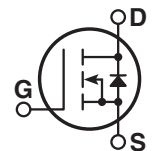
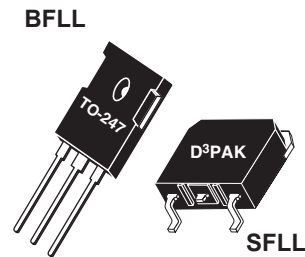


POWER MOS 7 FREDFET

Power MOS 7[®] is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7[®] by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7[®] combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package
- **FAST RECOVERY BODY DIODE**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT10090	UNIT
V_{DSS}	Drain-Source Voltage	1000	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	12	Amps
I_{DM}	Pulsed Drain Current ¹	48	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	298	Watts
	Linear Derating Factor	2.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ¹ (Repetitive and Non-Repetitive)	12	Amps
E_{AR}	Repetitive Avalanche Energy ¹	30	mJ
E_{AS}	Single Pulse Avalanche Energy ⁴	1210	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	1000			Volts
$I_{D(on)}$	On State Drain Current ² ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	12			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ² ($V_{GS} = 10V, 6A$)			0.95	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1000V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 800V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT10090BFLL - SFLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		1969		pF
C_{oss}	Output Capacitance			332		
C_{rss}	Reverse Transfer Capacitance			55		
Q_g	Total Gate Charge ³	$V_{GS} = 10V$ $V_{DD} = 500V$ $I_D = 12A @ 25^\circ C$		71		nC
Q_{gs}	Gate-Source Charge			12		
Q_{gd}	Gate-Drain ("Miller") Charge			47		
$t_{d(on)}$	Turn-on Delay Time	RESISTIVE SWITCHING $V_{GS} = 15V$ $V_{DD} = 500V$ $I_D = 12A @ 25^\circ C, R_G = 0.6\Omega$		9		ns
t_r	Rise Time			5		
$t_{d(off)}$	Turn-off Delay Time			23		
t_f	Fall Time			4		
E_{on}	Turn-on Switching Energy ⁶	INDUCTIVE SWITCHING @ 25°C $V_{DD} = 670V, V_{GS} = 15V$ $I_D = 12A, R_G = 5\Omega$		334		μJ
E_{off}	Turn-off Switching Energy			77		
E_{on}	Turn-on Switching Energy ⁶	INDUCTIVE SWITCHING @ 125°C $V_{DD} = 670V, V_{GS} = 15V$ $I_D = 12A, R_G = 5\Omega$		672		
E_{off}	Turn-off Switching Energy			100		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			12	Amps
I_{SM}	Pulsed Source Current ¹ (Body Diode)			48	
V_{SD}	Diode Forward Voltage ² ($V_{GS} = 0V, I_S = -I_D 12A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⁵			18	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D 12A, di/dt = 100A/\mu s$)	$T_J = 25^\circ C$		200	ns
		$T_J = 125^\circ C$		350	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D 12A, di/dt = 100A/\mu s$)	$T_J = 25^\circ C$		0.7	μC
		$T_J = 125^\circ C$		2.0	
I_{RRM}	Peak Recovery Current ($I_S = -I_D 12A, di/dt = 100A/\mu s$)	$T_J = 25^\circ C$		10	Amps
		$T_J = 125^\circ C$		15	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.42	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature
- ② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471

- ④ Starting $T_J = +25^\circ C, L = 16.8mH, R_G = 25\Omega, \text{Peak } I_L = 12A$
- ⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 12A, di/dt \leq 700A/\mu s, V_R \leq V_{DSS}, T_J \leq 150^\circ C$
- ⑥ E_{on} includes diode reverse recovery measured in accordance with JEDEC standard JESD24-1. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

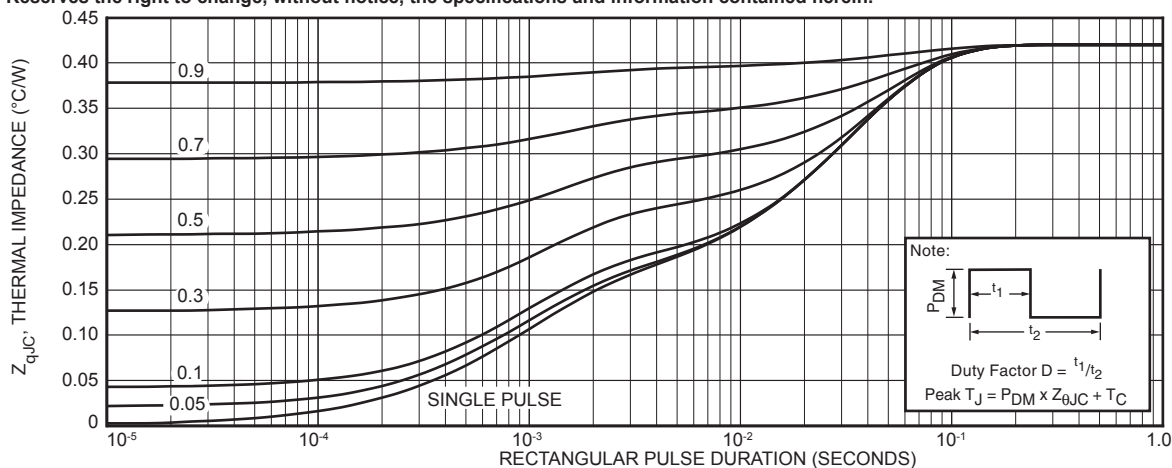


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT10090BFLL - SFLL

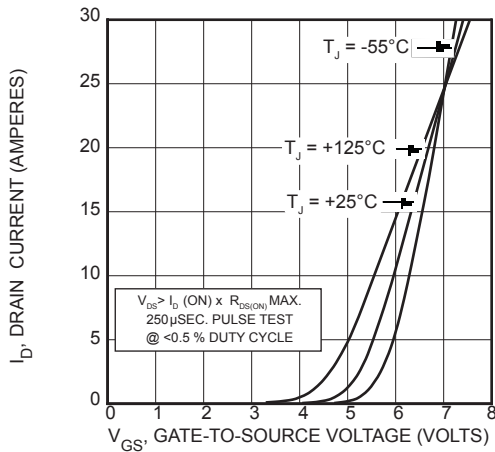


FIGURE 3, TRANSFER CHARACTERISTICS

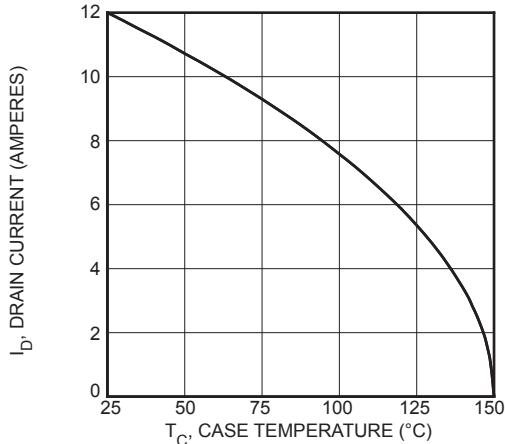


FIGURE 5, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

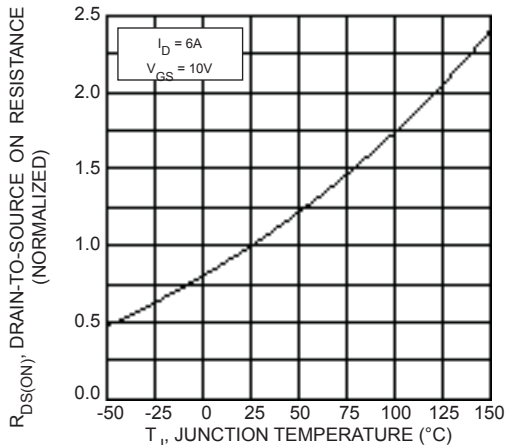


FIGURE 7, $R_{DS(\text{ON})}$ vs. TEMPERATURE

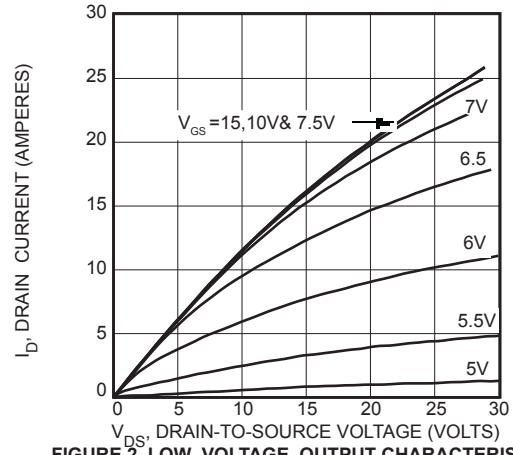


FIGURE 2, LOW VOLTAGE OUTPUT CHARACTERISTICS

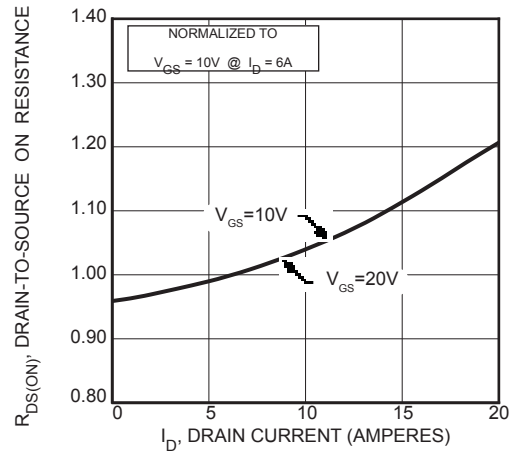


FIGURE 4, $R_{DS(\text{ON})}$ vs DRAIN CURRENT

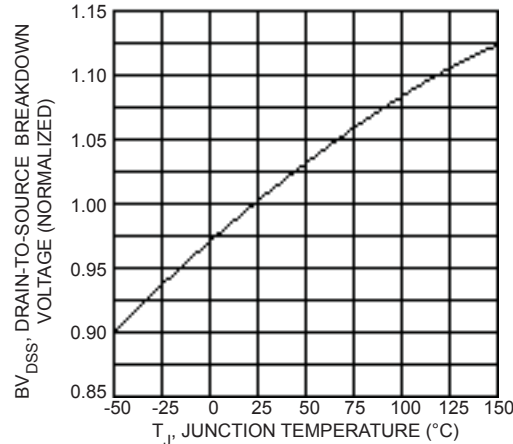


FIGURE 6, BREAKDOWN VOLTAGE vs TEMPERATURE

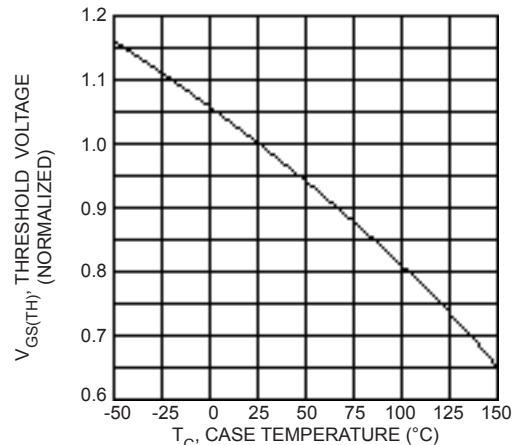


FIGURE 8, THRESHOLD VOLTAGE vs TEMPERATURE

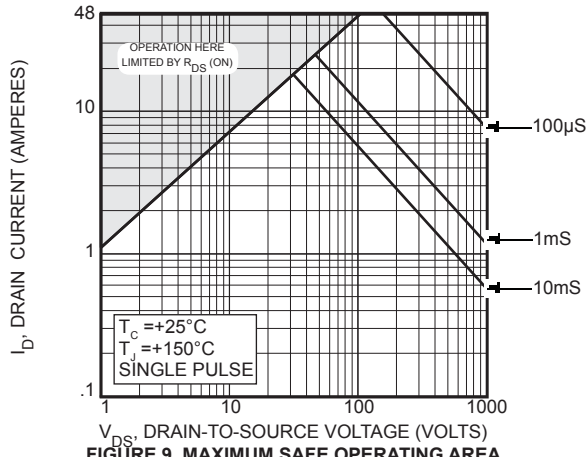


FIGURE 9, MAXIMUM SAFE OPERATING AREA

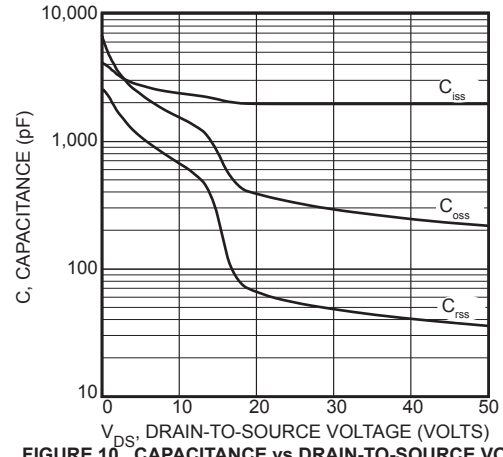


FIGURE 10, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

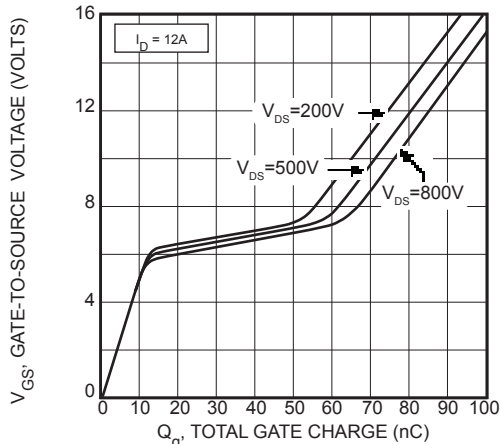


FIGURE 11, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

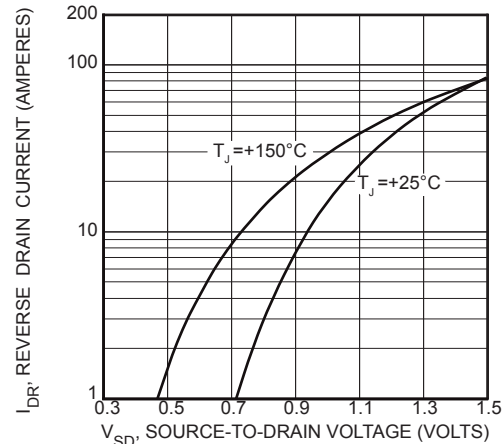


FIGURE 12, SOURCE-DRAIN DIODE FORWARD VOLTAGE

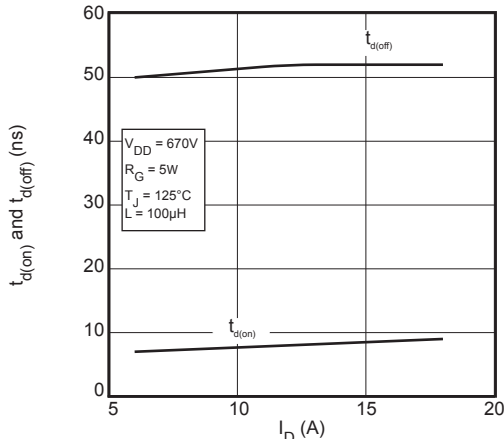


FIGURE 13, DELAY TIMES vs CURRENT

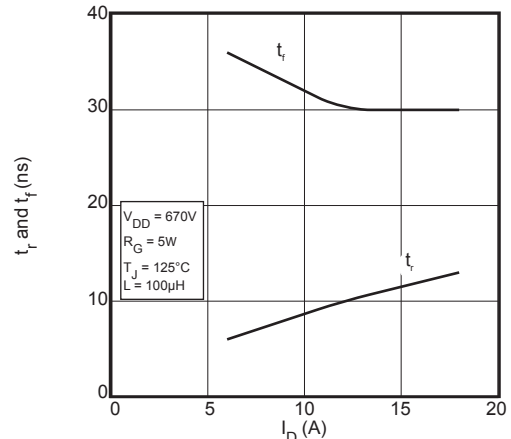


FIGURE 14, RISE AND FALL TIMES vs CURRENT

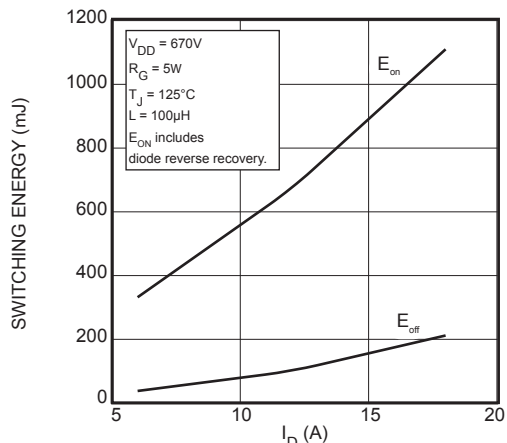


FIGURE 15, SWITCHING ENERGY vs CURRENT

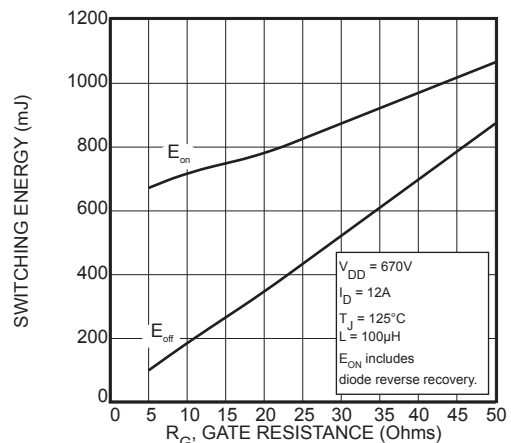


FIGURE 16, SWITCHING ENERGY vs. GATE RESISTANCE

Typical Performance Curves

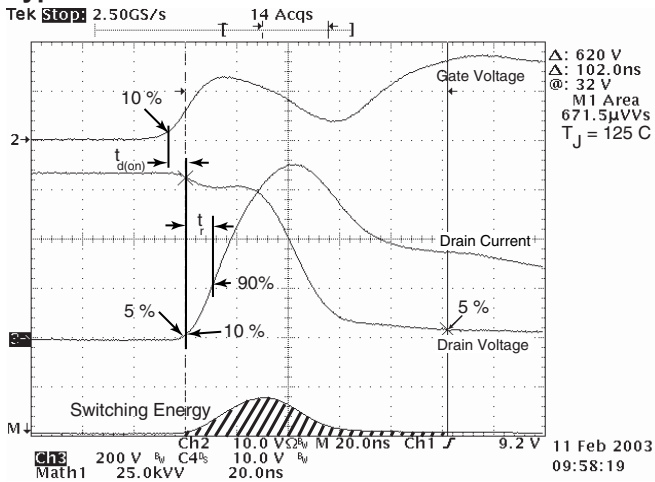


Figure 17, Turn-on Switching Waveforms and Definitions

APT10090BFL - SFLL

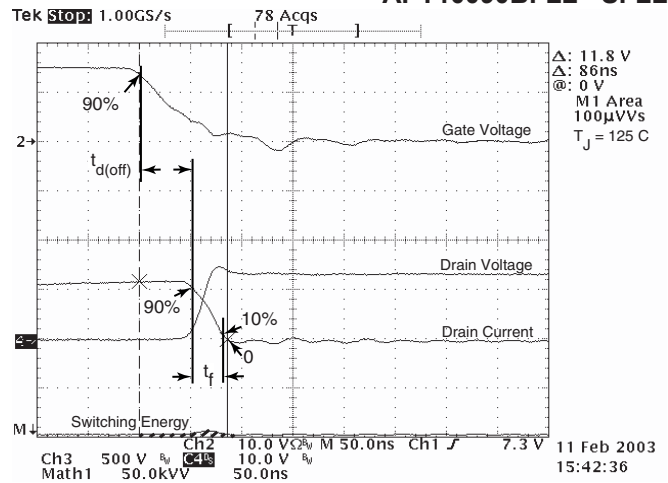


Figure 18, Turn-off Switching Waveforms and Definitions

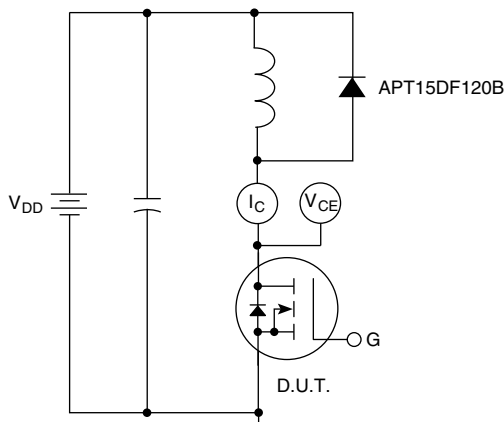
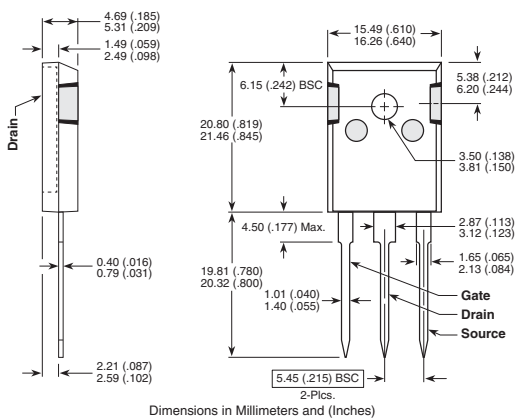
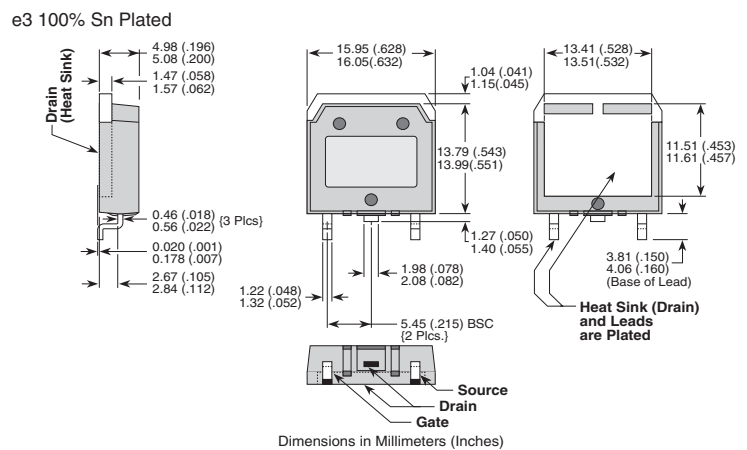


Figure 19, Inductive Switching Test Circuit

TO-247 (B) Package Outline



D³PAK Package Outline



Microsemi's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 6,939,743, 7,352,045 5,283,201 5,801,417 5,648,283 7,196,634 6,664,594 7,157,886 6,939,743 7,342,262 and foreign patents. US and Foreign patents pending. All Rights Reserved.