19-5881; Rev 2; 5/12

EVALUATION KIT AVAILABLE

Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

MAX17135

General Description

The MAX17135 is a complete power-management IC for E-paper displays that provides source- and gate-driver power supplies, a high-speed VCOM amplifier, and a temperature sensor.

The source-driver power supplies consist of a boost converter and an inverting buck-boost converter that generates +15V (up to +17V) and -15V (up to -17V), respectively. Both source-driver power supplies can deliver up to 200mA. The positive source-driver supply regulation voltage (V_{POS}) can be set either by using an I²C interface or by connecting an external resistor-divider. The negative source-driver supply voltage (V_{NEG}) is always tightly regulated to $-V_{POS}$ within ±50mV.

The gate-driver power supplies consist of regulated charge pumps that generate +22V (up to +40V) and -20V (up to -40V) and can deliver up to 20mA each.

The IC features a VCOM amplifier output whose output voltage is controlled by an internal 8-bit digital-to-analog converter (DAC). The DAC is programmable through an I²C interface and allows small-voltage-step sizes per DAC step.

The IC includes a temperature sensor that provides the ability to read the internal IC temperature and an external panel temperature with the use of an external temperature-sensing diode. Temperature output data is supplied through I²C.

The device is available in a space-saving, 32-pin TQFN package and is specified over the -40°C to +85°C extended temperature range.

Applications

E-Book Readers

Ordering Information

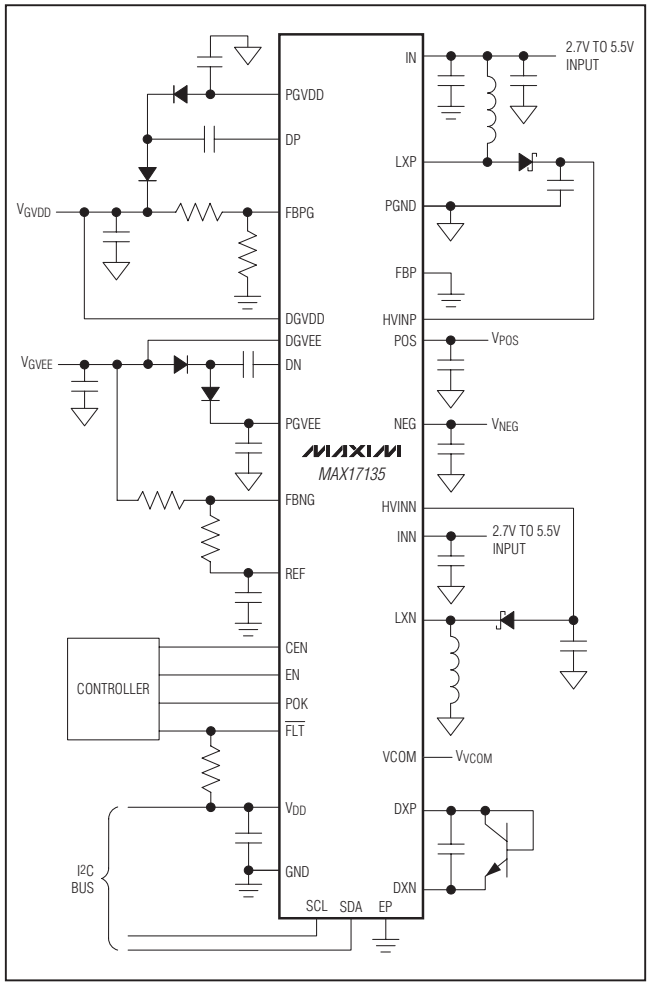
PART	TEMP RANGE	PIN-PACKAGE
MAX17135ETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Features

- **Four Regulated Output Voltages for Source- and Gate-Driver Power Supplies**
- **V_{POS} + V_{NEG} = ±50mV Tracking Accuracy**
- **Measures Internal and Remote Diode Temperature Sensors**
- **True Shutdown on All Outputs**
- **2.7V to 5.5V IN Supply Voltage Range**
- **Controlled Inrush Current During Soft-Start**
- **I²C Serial Interface for Temperature Read, Power Output Enable, POS Voltage Regulation Set-Point Adjustment, Power-Up/Power-Down Sequencing Adjustment, and Fault Monitoring**

Simplified Operating Circuit



Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

ABSOLUTE MAXIMUM RATINGS

IN, EN, CEN, VDD, SDA, SCL, INN, $\overline{FLT}$ to GND ... -0.3V to +6V
FBPG, FBNG, FBP, DXP, DXN, REF to GND ... -0.3V to (V_{IN} + 0.3V)
POK to GND ... -0.3V to (V_{VDD} + 0.3V)
LXP to PGND ... -0.3V to +20V
PGVDD, POS to GND ... -0.3V to (V_{HVINP} + 0.3V)
LXN to PGND ... (V_{HVINN} - 0.3V) to (V_{INN} + 0.3V)
PGVEE, NEG to GND ... (V_{HVINN} - 0.3V) to +0.3V
DP to PGND ... -0.3V to (V_{HVINP} + 0.3V)
DN to PGND ... (V_{HVINN} - 0.3V) to +0.3V
DGVDD to GND ... -0.3V to +42V
HVINN to PGND ... -20V to +0.3V
DGVEE to GND ... -42V to +0.3V
DGVDD to HVINN ... +60V
VCOM to GND ... (V_{HVINN} - 0.3V) to +0.3V
PGND to GND ... -0.3V to +0.3V
LXP, LXN, INN, PGND RMS Current Rating ... 1.6A
Continuous Power Dissipation (multilayer board)
TQFN (derate 24.9mW/°C above T_A = +70°C) ... 1990mW
Operating Temperature Range ... -40°C to +85°C
Junction Temperature ... +150°C
Storage Temperature Range ... -65°C to +150°C
Lead Temperature (soldering, 10s) ... +300°C
Soldering Temperature (reflow) ... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, *Typical Operating Circuit* of Figure 2, V_{HVINP} = 15V, V_{NEG} = -15V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES AND REFERENCE						
IN Voltage Range			2.7		5.5	V
IN UVLO Threshold		V_{IN} rising	2.45	2.55	2.65	V
IN UVLO Hysteresis				100		mV
IN Quiescent Current		EN = GND and the SHUTDOWN bit in the Configuration register = 1		4	10	µA
		EN = GND and the SHUTDOWN bit in the Configuration register = 0		0.8	1.5	mA
		V_{EN} = 3.6V, no switching, SHUTDOWN bit in the Configuration register = 0		2	3.5	
		V_{EN} = 3.6V, switching, SHUTDOWN bit in the Configuration register = 0		3		
V_{DD} Input Voltage			1.6		5.5	V
V_{DD} UVLO Threshold		V_{DD} rising, hysteresis = 150mV		1.2	1.5	V
V_{DD} Quiescent Current		EN = GND		4	10	µA
		Normal mode		4	10	
REF Output Voltage		No load	1.238	1.250	1.262	V
REF UVLO Threshold		REF rising		1.0	1.2	V
REF UVLO Hysteresis				100		mV
REF Load Regulation		0 < I_{REF} < 100µA		10		mV
REF Line Regulation		2.7V < V_{IN} < 5.5V		2		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, *Typical Operating Circuit* of Figure 2, V_{HVINP} = 15V, V_{NEG} = -15V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-UP REGULATOR						
Output Voltage Range	V_{HVINP}		V_{IN}		17	V
	V_{POS}	FBP = GND	5		17	
Operating Frequency			850	1000	1150	kHz
Oscillator Maximum Duty Cycle			91	95	98	%
Output Voltage Resolution		FBP = GND		4		Bits
POS Output Regulation Error		FBP = GND, V_{INN} = 2.7V to 5.5V, 1mA < I_{POS} < 200mA	-2		+2	%
FBP Regulation Voltage			1.238	1.250	1.262	V
FBP Load Regulation		1mA < I_{POS} < 200mA		-1		%
FBP Line Regulation		V_{IN} = 2.7V to 5.5V		-0.08		%/V
FBP Input Bias Current		V_{FBP} = 1.25V, T_A = +25°C	50	125	200	nA
FBP Internal Divider Enable Threshold		FBP rising, hysteresis = 10mV		25	50	mV
LXP On-Resistance		I_{LXP} = 0.2A		250	500	mΩ
LXP Leakage Current		EN = GND, V_{LXP} = 18V, T_A = +25°C			20	µA
LXP Current Limit		Duty cycle = 80%	1.5	1.8	2.1	A
Soft-Start Period				5		ms
INVERTING REGULATOR						
INN Input Voltage Range			2.7		5.5	V
INN Quiescent Current		EN = GND			10	µA
		No switching			10	
		Switching			3	mA
Output Voltage Range	V_{HVINN}		-17			V
Operating Frequency			850	1000	1150	kHz
Oscillator Maximum Duty Cycle			91	95	98	%
V_{POS} + V_{NEG} Regulation Voltage		V_{INN} = 2.7V to 5.5V, 1mA < I_{NEG} < 200mA, I_{POS} = no load	-100		+100	mV
LXN On-Resistance		INN to LXN, I_{LXN} = 0.2A		250	500	mΩ
LXN Leakage Current		V_{LXN} = V_{HVINN} = -18V, T_A = +25°C			20	µA
LXN Current Limit		Duty cycle = 85%	1.8	2.1	2.4	A
Soft-Start Period				5		ms
POSITIVE CHARGE-PUMP REGULATOR						
PGVDD Operating Voltage Range	V_{PGVDD}		7		V_{HVINP}	V
HVINP-DP Current Limit			150			mA
Oscillator Frequency			400	500	600	kHz

Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, *Typical Operating Circuit* of Figure 2, V_{HVINP} = 15V, V_{NEG} = -15V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBPG Regulation Voltage			1.238	1.250	1.262	V
FBPG Line Regulation		V_{HVINP} = 11V to 16V		0.05		%/V
FBPG Load Regulation		0mA < I_{GVDD} < 100mA		0.04		%
FBPG Input Bias Current		V_{FBPG} = 1.25V, T_A = +25°C	-50		+50	nA
DP On-Resistance High		I_{DP} = 100mA		3	6	Ω
DP On-Resistance Low		I_{DP} = -100mA		1.5	3	Ω
Soft-Start Period				10		ms
NEGATIVE CHARGE-PUMP REGULATOR						
PGVEE Operating Voltage Range	V_{PGVEE}		V_{HVINN}		-7	V
HVINN-DN Current Limit			150			mA
Oscillator Frequency			400	500	600	kHz
FBNG Regulation Voltage			-12	0	+12	mV
FBNG Line Regulation		V_{NEG} = -11V to -16V		0.05		%/V
FBNG Load Regulation		0mA < I_{GVEE} < 100mA		-0.03		%
FBNG Input Bias Current		V_{FBNG} = 0V, T_A = +25°C	-50		+50	nA
DN On-Resistance High		I_{DN} = 100mA		3	6	Ω
DN On-Resistance Low		I_{DN} = -100mA		1.5	3	Ω
Soft-Start Period				10		ms
VCOM						
Input Supply Range			V_{HVINN}		-5	V
HVINP Shutdown Current		V_{EN} = GND and the SHUTDOWN bit in the Configuration register = 1, V_{HVINP} = 3.6V		10	30	µA
HVINP Quiescent Current		V_{HVINP} = 15V, V_{EN} = 3.6V, Configuration register = 0		0.8		mA
HVINN Quiescent Current		V_{HVINN} = -15V, V_{EN} = 3.6V, Configuration register = 0		2.0		mA
VCOM Voltage High		I_{VCOM} = 5mA		-25	-50	mV
VCOM Voltage Low		I_{VCOM} = -5mA	V_{HVINN} + 50	V_{HVINN} + 25		mV
VCOM Load Regulation		0mA < I_{VCOM} < 30mA, sourcing, DVR register = 7Fh	-1.6	-0.6		%
		0mA < I_{VCOM} < 30mA, sinking, DVR register = 7Fh		0.3	1.3	
VCOM Output Current		Sourcing	70			mA
		Sinking	70			
VCOM High Impedance Leakage		CEN = GND, T_A = +25°C			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, *Typical Operating Circuit* of Figure 2, V_{HVINP} = 15V, V_{NEG} = -15V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEQUENCE SWITCHES						
POS Output Range	V_{POS}	Tracks HVINP	V_{IN}		17	V
POS On-Resistance		(HVINP - POS), I_{POS} = 100mA		0.9	1.3	Ω
POS Charge Current Limit			250			mA
POS Discharge Resistance			200	340	600	Ω
POS Soft-Start Charge Time				10		ms
NEG Output Range	V_{NEG}	Tracks HVINN	-17			V
NEG On-Resistance		(HVINN - NEG), I_{NEG} = 100mA		0.6	1	Ω
NEG Charge Current Limit			250			mA
NEG Discharge Resistance			200	340	600	Ω
NEG Soft-Start Charge Time				10		ms
PGVDD On-Resistance		(HVINP - PGVDD), I_{PGVDD} = 30mA		4	7	Ω
PGVEE On-Resistance		(HVINN - PGVEE), I_{PGVEE} = 30mA		1.5	3	Ω
DGVDD AND DGVEE						
DGVDD Input Voltage Range			7		40	V
DGVDD Discharge Resistance			800	1200	1600	Ω
DGVEE Input Voltage Range			-40		-7	V
DVGEE Discharge Resistance			800	1200	1600	Ω
VCOM Discharge Resistance			100	170	300	Ω
FAULT PROTECTION						
HVINP Fault Threshold		V_{HVINP} falling	75	80	85	%
FBP Fault Threshold		V_{FBP} falling	0.95	1.00	1.05	V
FBPG Fault Threshold		V_{FBPG} falling	0.95	1.00	1.05	V
HVINN Fault Threshold		V_{HVINN} rising	$-V_{HVINP}$ x 0.85	$-V_{HVINP}$ x 0.8	$-V_{HVINP}$ x 0.75	V
FBNG Fault Threshold		V_{FBNG} rising	200	250	300	mV
Feedback Fault Timer				50		ms
Thermal Shutdown		Hysteresis = 15°C		160		°C
TEMPERATURE SENSOR						
Temperature Resolution		Monotonicity guaranteed	8			Bits
		LSB		0.5		°C
External Diode Temperature Error		T_A = 0°C to +85°C	-4		+4	°C
		T_A = -40°C to +125°C	-8		+8	
External Conversion Time			60			ms
Conversion Rate		Register 0Fh = 100b		1		Conv/s
		Register 0Fh = 111b		8		
Diode Source Current		V_{DXP} = 1.5V - high level	90	100	110	µA
		V_{DXP} = 1.5V - low level	9.0	10	11.0	
Diode Source Current Ratio		V_{DXP} = 1.5V	9.5	10	10.5	A/A

Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, *Typical Operating Circuit* of Figure 2, V_{HVINP} = 15V, V_{NEG} = -15V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DXN Source Voltage			0.4	0.7	0.85	V
Diode Short-Circuit Threshold		V_{DXN} = 0.7V, V_{DXP} - V_{DXN}	20	65	110	mV
Diode Open-Circuit Threshold		V_{DXN} = 0.7V, V_{DXP} - V_{DXN}	1.6	1.9	2.2	V
PROGRAMMABLE VCOM CALIBRATOR						
VCOM-DAC Voltage Resolution			8			Bits
VCOM-DAC Differential Nonlinearity		Monotonic over temperature	-1		+1	LSB
VCOM-DAC Accuracy		VCOM_set = 0x7F. T_A = 0°C to +85°C	-1.5		+1.5	LSB
VCOM-DAC Accuracy		VCOM_set = 0x7F. T_A = -40°C to +85°C	-2.5		+2.5	LSB
VCOM-DAC Accuracy		Other setting	-4		+4	LSB
Memory Program Voltage		HVINP rising, hysteresis = 250mV	6.95	7.1	7.25	V
POS Settling Time		To ±0.5 LSB error band		20		µs
Memory Write Cycles			30			Times
Memory Write Time			110			ms
CONTROL LOGIC						
Input Low Voltage		EN, CEN			0.3 x V_{DD}	V
Input High Voltage		EN, CEN	0.7 x V_{DD}			V
Input Impedance		EN, CEN = 3.6V		1		MΩ
POK Logic-High Output Voltage		I_{POK} = 0.5mA	V_{DD} - 0.4			V
POK Logic-Low Output Voltage		I_{POK} = -0.5mA			0.4	V
$\overline{FLT}$ Leakage Current		$V_{\overline{FLT}}$ = 5.5V, T_A = +25°C			1	µA
$\overline{FLT}$ Output Low Voltage		$I_{\overline{FLT}}$ = 6mA			0.4	V
I²C INTERFACE						
Input Capacitance		SDA, SCL		5		pF
Input Low Voltage	V_{IL}	SDA, SCL			0.3 x V_{DD}	V
Input High Voltage	V_{IH}	SDA, SCL	0.7 x V_{DD}			V
SDA Sink Current		V_{SDA} = 0.4V	6			mA
SCL Frequency	f_{SCL}		DC		400	kHz
SCL High Time	t_{HIGH}		600			ns
SCL Low Time	t_{LOW}		1300			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, *Typical Operating Circuit* of Figure 2, V_{HVINP} = 15V, V_{NEG} = -15V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA, SCL Rise Time	t_R	C_{BUS} = total bus line capacitance (pF) (Note 2)	20 + 10 x C_{BUS}		300	ns
SDA, SCL Fall Time	t_F	C_{BUS} = total bus line capacitance (pF) (Note 2)	20 + 10 x C_{BUS}		300	ns
START Hold Time	$t_{HD;STA}$	10% of SDA to 90% of SCL	600			ns
START Setup Time	$t_{SU;STA}$		600			ns
Data Input Hold Time	$t_{HD;DAT}$		0			ns
Data Input Setup Time	$t_{SU;DAT}$		100			ns
STOP Setup Time	$t_{SU;STO}$		600			ns
Bus Free Time	t_{BUF}		1300			ns
Input Spike Suppression		SDA, SCL (Note 2)			250	ns
SDA Reset Low Time	$t_{TIMEOUT}$	(Notes 1, 2)			60	ms

Note 1: Holding the SDA line low for a time greater than $t_{TIMEOUT}$ causes the device to reset SDA to the IDLE state of the serial bus communication (SDA set high).

Note 2: Guaranteed by design, not production tested.

Note 3: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design.

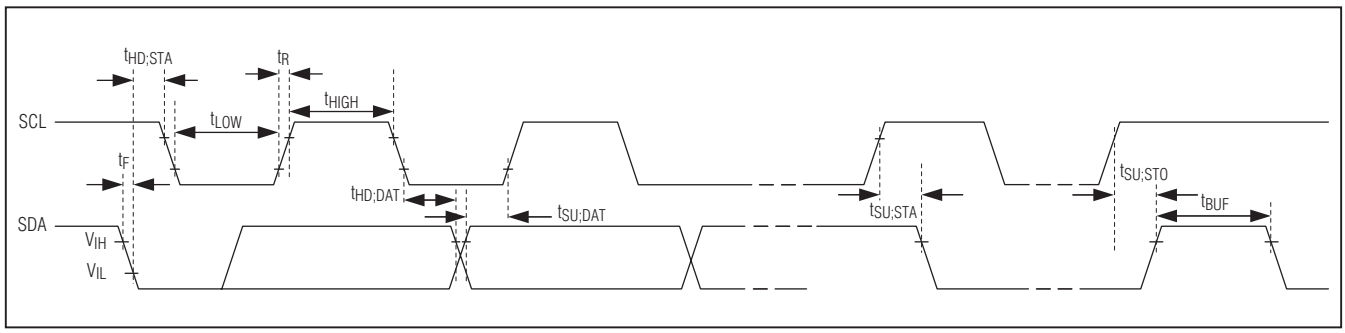


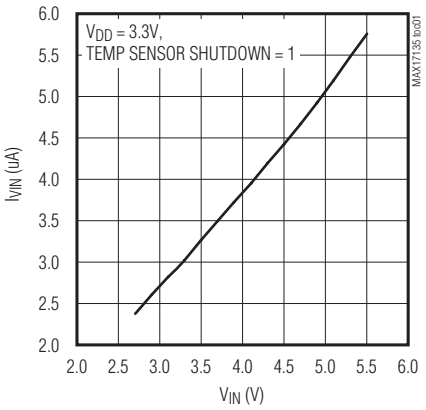
Figure 1. Timing Definitions Used in the Electrical Characteristics

Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

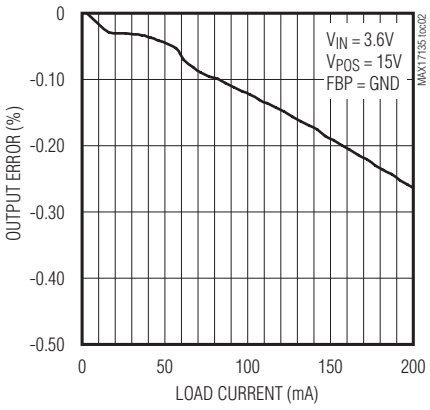
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

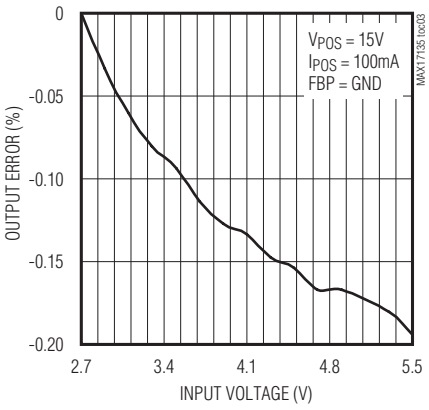
TOTAL INPUT SUPPLY STANDBY CURRENT vs. IN SUPPLY VOLTAGE



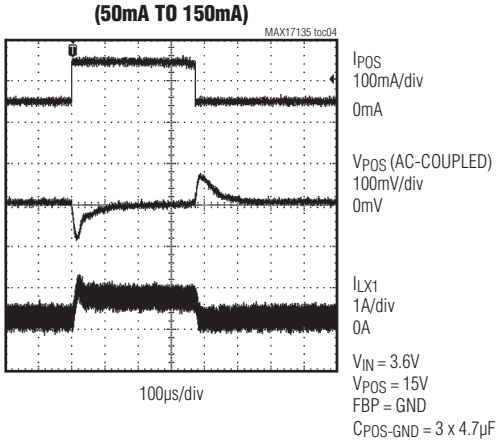
POS LOAD REGULATION



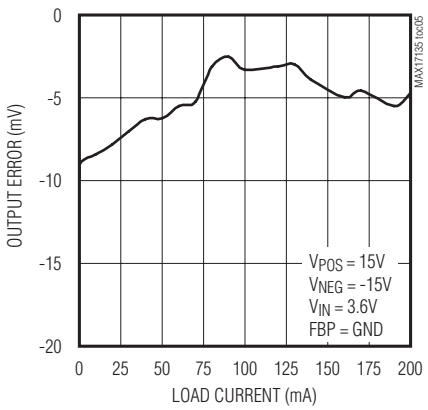
POS LINE REGULATION



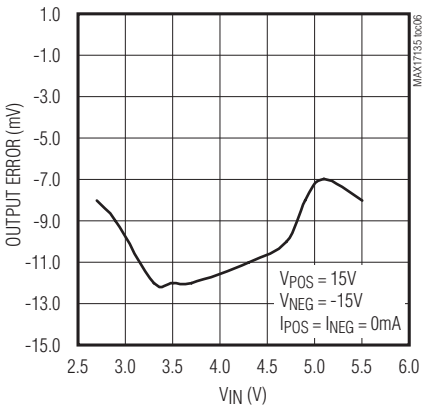
POS LOAD-TRANSIENT RESPONSE (50mA TO 150mA)



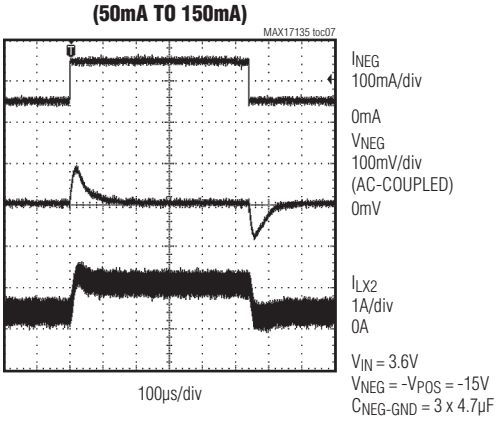
VPOS + VNEG LOAD REGULATION



VPOS + VNEG LINE REGULATION



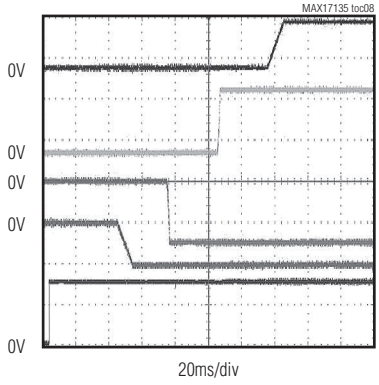
NEG LOAD-TRANSIENT RESPONSE (50mA TO 150mA)



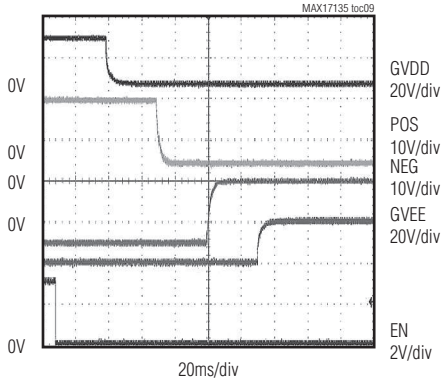
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

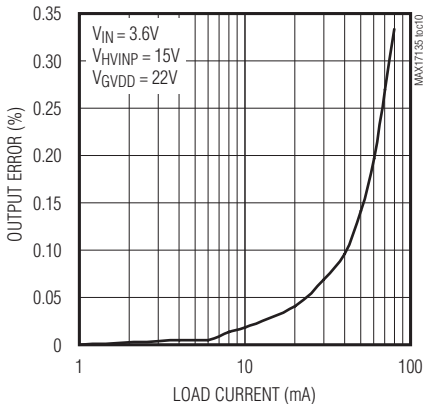
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



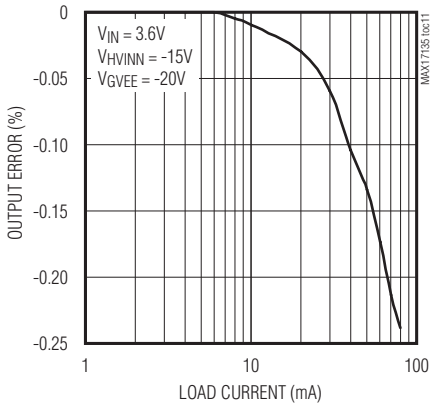
POWER-DOWN SEQUENCE OF ALL SUPPLY OUTPUTS



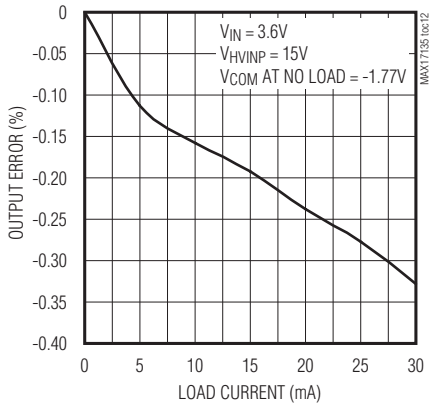
GVDD LOAD REGULATION



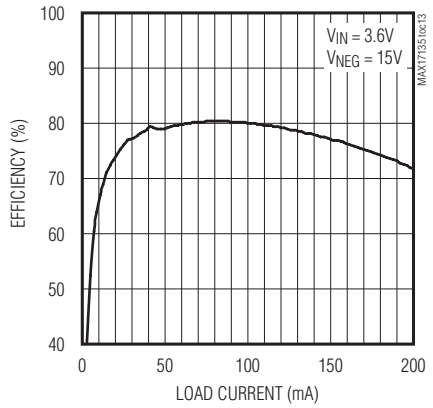
GVEE LOAD REGULATION



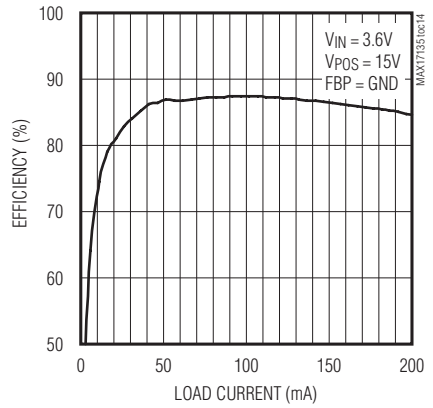
VCOM LOAD REGULATION



NEG EFFICIENCY vs. LOAD CURRENT

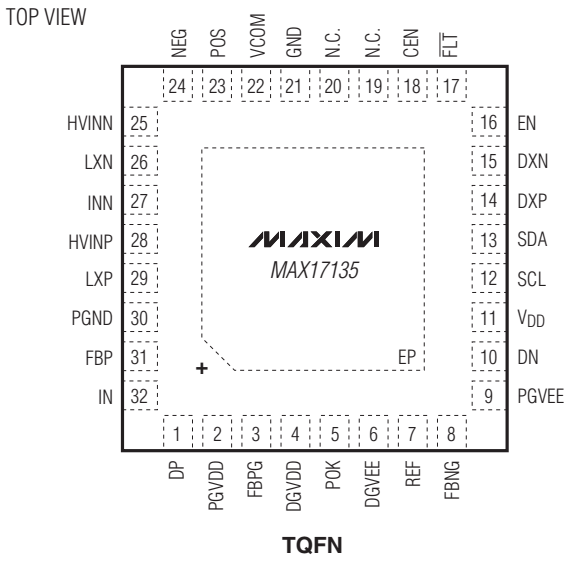


POS EFFICIENCY vs. LOAD CURRENT



Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1	DP	Regulated Charge-Pump Driver for GVDD. Connect to flying capacitor.
2	PGVDD	Supplies the HVINP Voltage for the Positive Charge Pump. Connect as shown in Figure 2.
3	FBPG	Feedback Input for GVDD
4	DGVDD	GVDD Discharge. Connect the output of the positive charge pump to DGVDD as shown in Figure 2.
5	POK	Power-OK. Driven high when the outputs of the gate- and source-driver power supplies are all in regulation.
6	DGVEE	GVEE Discharge. Connect the output of the negative charge pump to DGVEE as shown in Figure 2.
7	REF	Voltage Reference. Bypass to GND with a minimum 0.1µF ceramic capacitor.
8	FBNG	Feedback Input for GVEE
9	PGVEE	Supplies the HVINN Voltage to the Negative Charge Pump for the GVEE Output. Connect as shown in Figure 2.
10	DN	Regulated Charge-Pump Driver for GVEE. Connect to flying capacitor.
11	V_{DD}	Logic Supply Input for the I^2C. Bypass to GND through a minimum 0.1µF capacitor.
12	SCL	I^2C Serial Clock Input
13	SDA	I^2C Serial Data Input/Output
14	DXP	External Temperature-Sensing Diode Anode Connection. Bypass DXP to DXN with a 2200pF ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
15	DXN	External Temperature-Sensing Diode Cathode Connection
16	EN	Enable Pin. Logic-high initiates power-up sequencing. Logic-low initiates power-down sequencing.
17	$\overline{FLT}$	Fault Indicator. Open-drain output goes low during a fault condition.
18	CEN	VCOM Enable. Logic-high enables VCOM output. Logic-low causes the load on the VCOM output to be discharged.
19, 20	N.C.	No Connection
21	GND	Analog GND
22	VCOM	VCOM Output
23	POS	Positive Source-Driver Output Voltage
24	NEG	Negative Source-Driver Output Voltage
25	HVINN	Input Power for the NEG Voltage Rail. Connect the output of the inverting converter to this pin.
26	LXN	DC-DC Inverting Converter Inductor/Diode Connection
27	INN	Inverting Converter Power Input. 2.7V to 5.5V. Bypass to PGND with a minimum 10µF ceramic capacitor.
28	HVINP	Input Power for the POS Voltage Rail. Connect the output of the step-up converter to this pin.
29	LXP	Step-Up Converter Inductor/Diode Connection
30	PGND	Power Ground
31	FBP	Feedback Pin for HVINP Output. Connect FBP to GND to set the HVINP regulation voltage to +15V. With FBP connected to ground, V_{HVINP} can be changed through I^2C after power-up by changing the value stored in the HVINP register. Alternatively, connect an external resistor-divider midpoint to the FBP pin to set the HVINP regulation voltage.
32	IN	Power Input. Bypass to GND through a minimum 1µF capacitor.
—	EP	Exposed Pad. Connect exposed pad to ground.

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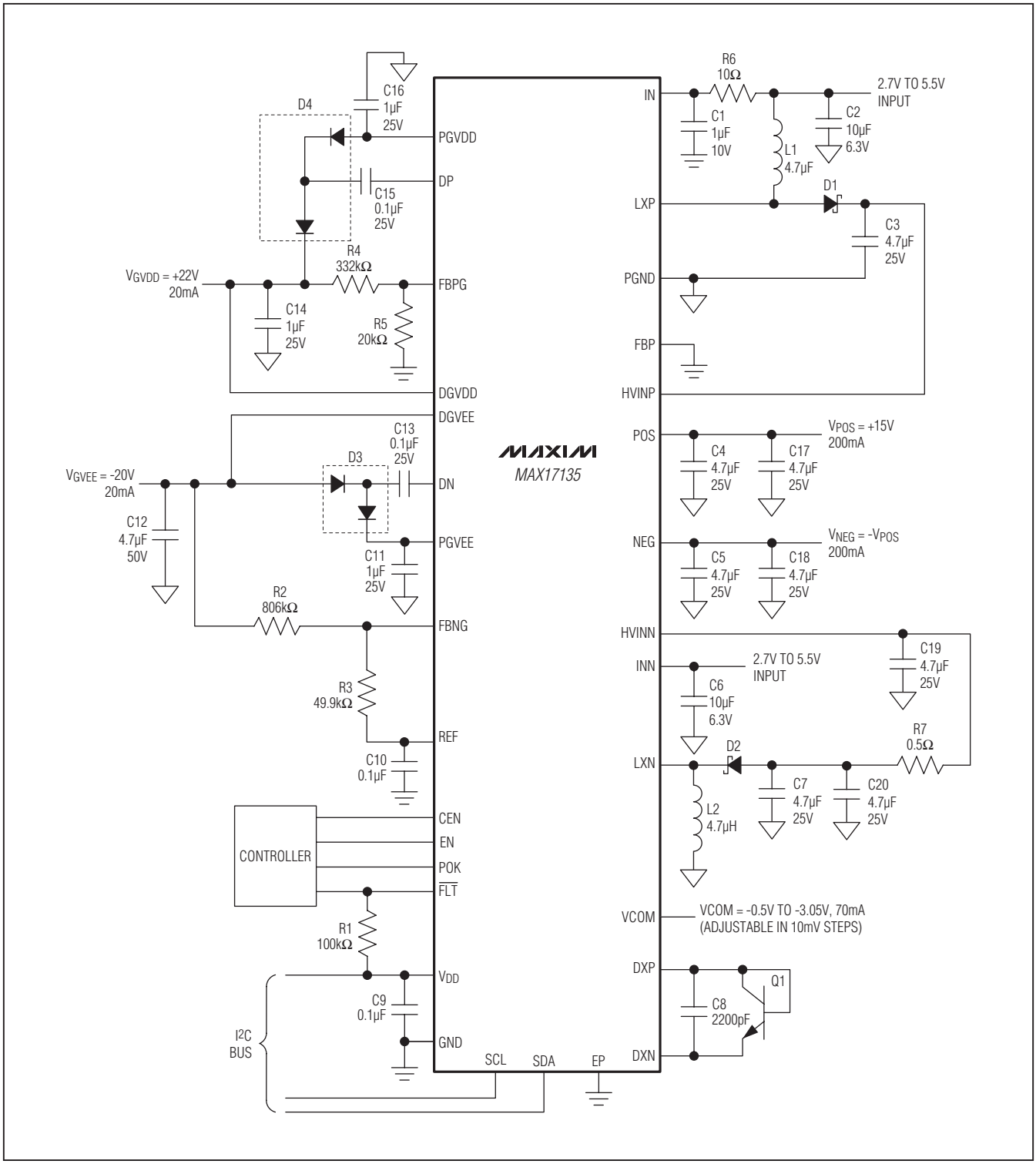

Figure 2. Typical Operating Circuit

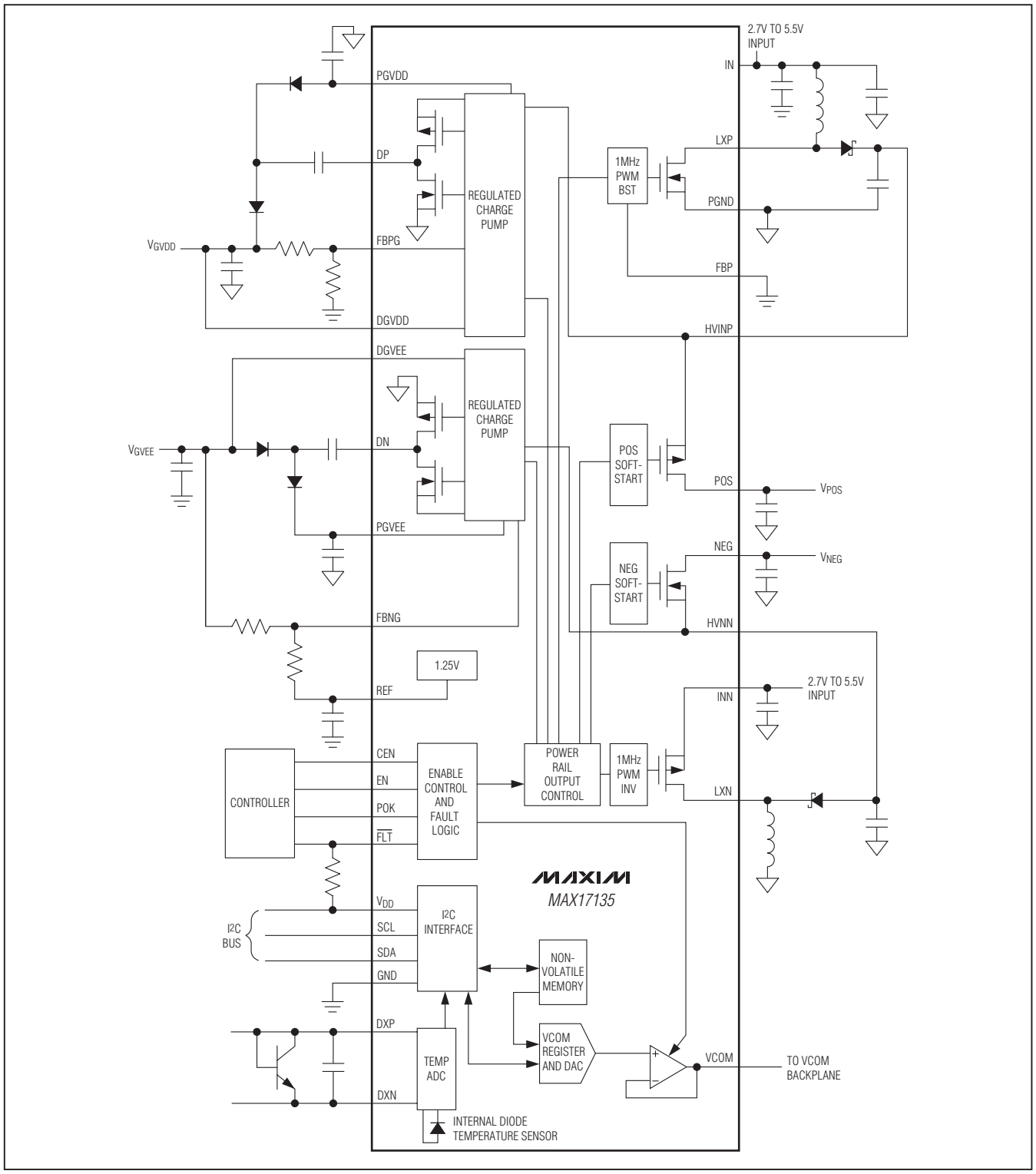

Figure 3. Functional Diagram

Multi-Output DC-DC Power Supply with VCOM Amplifier and Temperature Sensor for E-Paper Applications

Typical Operating Circuit

The IC's typical operating circuit (Figure 2) generates ±15V source-driver supplies and +22V and -20V gate-driver supplies for E-paper displays. The input voltage range for the IC is from 2.7V to 5.5V. Figure 3 shows the functional diagram. Table 1 lists recommended components and Table 2 lists contact information for component suppliers.

Detailed Description

Source-Driver Power Supplies

The source-driver power supplies consist of a boost converter and an inverting buck-boost converter that generate +15V (+17V max) and -15V (-17V max), respectively, and can deliver up to 200mA. The positive source-driver power supply's regulation voltage (V_{POS}) can be set using the external resistor-divider network shown in Figure 2, or can be programmed through the I^2C interface connecting FBP to GND before power-up.

Table 1. Component List

DESIGNATION	DESCRIPTION
C2, C6	10µF ±10%, 6.3V X7R ceramic capacitors (0805) TDK C2012X7R0J106K
C3, C4, C5, C7, C17–C20	4.7µF ±10%, 25V X7R ceramic capacitors (1206) Murata GRM31CR71E475KA88L
D1, D2	30V, 1A single Schottky diodes (SOD123) ON Semiconductor MBR130T1
D3, D4	Dual small-signal diodes (SOT23) Fairchild MMBD4148SE
L1, L2	4.7µH, 1.5A, 45mΩ inductors TOKO A915AY-4R7M
Q1	40V npn transistor (SOT23) Fairchild MMBT3904

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Fairchild Semiconductor	www.fairchildsemi.com
Murata Electronics North America, Inc.	www.murata-northamerica.com
ON Semiconductor	www.onsemi.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com

The negative source-driver supply voltage (V_{NEG}) is automatically tightly regulated to $-V_{POS}$ within ±50mV. V_{NEG} cannot be adjusted independently of V_{POS}.

Gate-Driver Power Supplies

The positive gate-driver power supply (GVDD) generates +22V (+40V max) and the negative gate-driver power supply (GVEE) generates -20V (-40V max). Both supplies can supply up to 20mA current. The GVDD and GVEE regulation voltages are both set by using the external resistor-divider networks shown in Figure 2.

VCOM Amplifier

The IC features a negative output VCOM amplifier whose voltage is programmed through an I^2C interface. An internal 8-bit digital-to-analog converter (DAC) allows for a wide VCOM output range of -0.5V to -3.05V and a 10mV change per DAC step. The user can store the DAC setting in nonvolatile memory. On power-up, the nonvolatile memory sets the DAC to the last stored setting.

Temperature Sensor

The IC includes a temperature sensor that reads the internal IC temperature and the external panel temperature with the use of an external temperature-sensing diode. Temperature output data is supplied through I^2C. An analog-to-digital converter (ADC) converts the temperature data to 9 bits, two's-complement format and stores the conversion results in separate temperature registers.

Fault Protection

The IC has robust fault and overload protection. If any of the GVEE, NEG, POS, or GVDD outputs fall more than 80% (typ) below their intended regulation voltage for more than 50ms (typ), or if a short-circuit condition occurs on any output for any duration, then all outputs latch off and $\overline{FLT}$ is asserted low. The fault condition is set in the Fault register, which can be read through the I^2C interface.

True Shutdown

The IC completely disconnects the loads from the input when in shutdown mode. In most boost converters, the external rectifying diode and inductor form a DC current path from the battery to the output. This can drain the battery even in shutdown if a load was connected at the boost-converter output. The device has an internal switch at POS. When this switch turns off during shutdown, there is no DC path from the input to POS.

Output Control

The IC's source-driver and gate-driver outputs (GVEE, NEG, POS, and GVDD) and VCOM amplifier output can be controlled by driving the IC's EN and CEN pins, respectively. Alternatively, the EN and CEN pins can be left unconnected or connected to GND such that their corresponding functions can be controlled by toggling the EN and CEN bits in the enable register. All outputs are brought up with soft-start control to limit the inrush current.

Power-On/Power-Off Sequencing and Timing

The IC allows for flexible power-up/power-down sequencing and timing of the source-driver and gate-driver power supplies (GVEE, NEG, POS, and GVDD). Toggling the EN pin from low to high or setting the EN bit in the enable register to 1 initiates an adjustable preset power-up sequence. Toggling the EN pin from high to low or setting the EN bit in the Enable register to 0 initiates an adjustable preset power-down sequence. The power-up/power-down sequence and timing between rails are determined by the user's values programmed into the Timing registers through I²C. The desired sequence and timing between rails contained in the Timing registers can also be stored in the nonvolatile memory, such that desired timing information is loaded into the Timing registers at power-up.

I²C Interface

The device supports an I²C-compatible, 2-wire digital interface. SDA is the bidirectional data line and SCL is the clock line of the 2-wire interface corresponding, respectively, to the SDA and SCL lines of the I²C bus. Write to a register by writing the device address byte, a data pointer byte, and a data byte. Read from the IC in one of two ways: if the location latched in the Pointer register is set from the previous read, the new read consists of a device address byte, followed by retrieving the corresponding number of data bytes. If the Pointer register needs to be set to a new address, perform a read operation by writing the device address byte, pointer byte, repeat start, and the device address byte again with the read bit. An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the device to stop in a state where the SDA line is held low. Ordinarily, this would prevent any further bus communication until the master sends nine additional clock cycles or SDA goes high. At that time, a STOP condition resets the device. If the additional clock cycles are not generated by the master, the IC bus resets and unlocks after the bus timeout period has elapsed.

The device uses the read and write protocols shown in Figure 4.

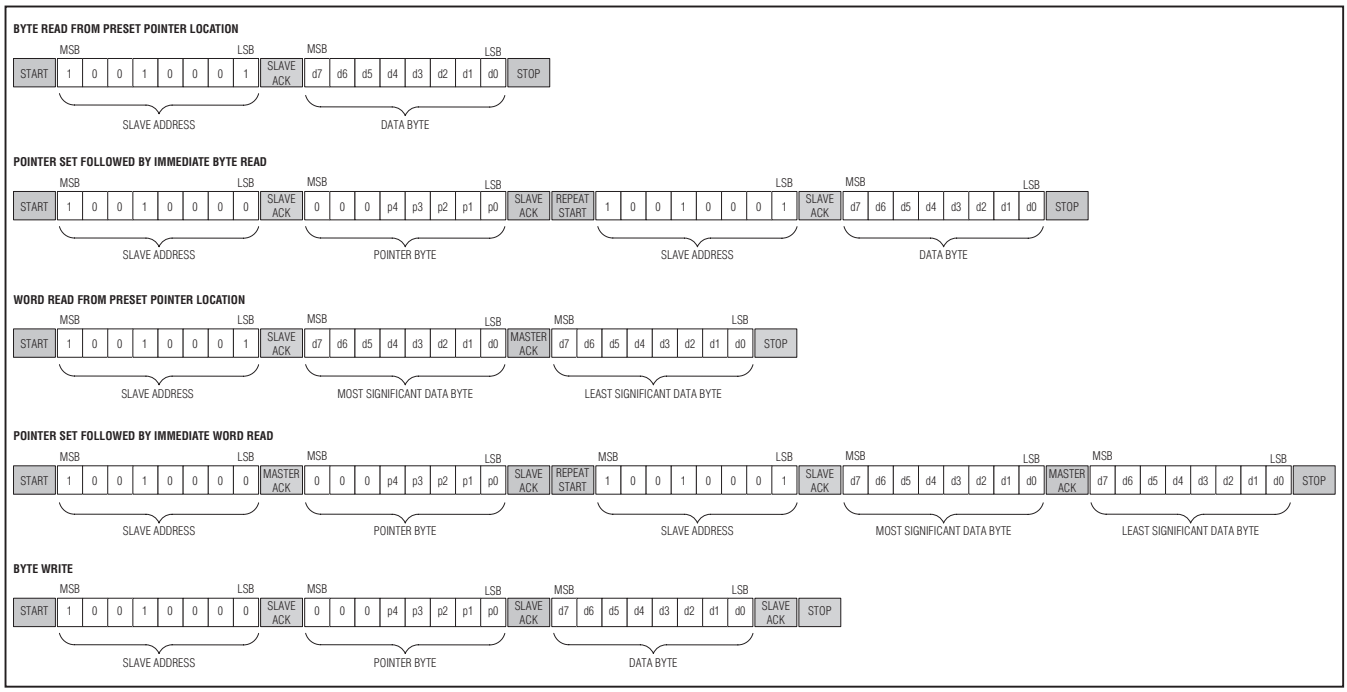

Figure 4. Read/Write Protocols

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I²C Address

The IC is a slave-only device and responds to the 7-bit address 90h. The read and write commands can be distinguished by adding 1 more bit (R/W bit) to the end of the 7-bit slave address, with 1 indicating read, and 0 indicating write.

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0	R-/W

I²C Registers

The device contains 20 data registers along with an additional Pointer register. The Pointer register selects which of the other 19 data registers to be read from or written to. At power-up, the Pointer is set to read the External Temperature register at address 0x00. The Pointer register latches the last location to which it was set.

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	Register Select				

P4–P0 Register Select

P4–P0 (HEX)	REGISTER	NO. OF BITS	POR STATE
00	External Temperature register (read only) (power-up default)	16	N/A
01	Configuration register (read/write)	8	00h
04	Internal Temperature register (read only)	16	N/A
05	Status register (read only)	8	N/A
06	Product Revision register (read only)	8	00h
07	Product ID Register (read only)	8	4Dh
08	DVR register (R/W)	8	FFh
09	Enable register (R/W)	8	00h
0A	Fault register (read only)	8	N/A
0B	HVINP register (R/W)	8	0Ah
0C	Programming Control register (write only)	8	N/A
0Fh	Temperature Conversion Rate register	8	04h
10	t1 Timing register (R/W)	8	1Eh (factory default)
11	t2 Timing register (R/W)	8	3Ch (factory default)
12	t3Timing register (R/W)	8	5Ah (factory default)
13	t4 Timing register (R/W)	8	78h (factory default)
14	t5 Timing register (R/W)	8	1Eh (factory default)
15	t6 Timing register (R/W)	8	3Ch (factory default)
16	t7 Timing register (R/W)	8	5Ah (factory default)
17	t8 Timing register (R/W)	8	78h (factory default)

External and Internal Temperature Registers (00h and 04h), Read Only

The temperature data format of the External Temperature register (00h) and the Internal Temperature register (04h) are both 9 bits, two's complement, and are read out in word format: an upper byte and a lower byte. Bits D15–D7 contain the temperature data, with the LSB representing +0.5°C and the MSB representing the sign bit. The last 7 bits of the lower byte, bits D6–D0, are don't care.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign Bit 1 = Negative 0 = Positive	+64°C	+32°C	+16°C	+8°C	+4°C	+2°C	+1°C	+0.5°C	X	X	X	X	X	X	X

X = Don't care.

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
+125	0111 1101 0XXX XXXX	7D0X
+25	0001 1001 0XXX XXXX	190X
+0.5	0000 0000 1XXX XXXX	008X
0	0000 0000 0XXX XXXX	000X
-0.5	1111 1111 1XXX XXXX	FF8X
-25	1110 0111 0XXX XXXX	E70X

X = Don't care.

Configuration Register (01h) (R/W)

After the IN and V_{DD} voltages have risen above their respective undervoltage-lockout thresholds, the Shutdown bit (D0) is set to 0 and temperature conversions begin immediately. Temperature conversions are continually performed every 1s unless the temperature sensor is put into shutdown mode. Set D0 to 1 to put the temperature sensor in shutdown mode to reduce supply current.

D0: SHUTDOWN: When set to 1, the temperature sensor is shut down.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Shutdown

Status Register (05h), Read Only

The Status register indicates whether the IC's ADC is in the process of performing a temperature conversion and whether there are any fault conditions with the remote temperature-sensing diode. Any fault condition with the external temperature-sensing diode causes the external temperature register to return 7FC0h.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	SHORT	OPEN	BUSY

D0: BUSY: Is set to 1 when the ADC is in the process of performing a temperature conversion.

D1: OPEN: Is set to 1 when any connections from DXN and DXP to the temperature-sensing diode are open.

D2: SHORT: Is set to 1 when there is a short-circuit condition between DXP and DXN.

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Product Revision Register (06h), Read Only

This register contains the product revision 0x00h.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Product Identification Register (07h), Read Only

Maxim is indicated by 0x4Dh.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	0	1

DVR Register (08h) R/W

The VCOM voltage can be set anywhere between -0.5V and -3.050V with 10mV per LSB by programming the DVR register with a corresponding value as shown in the table below. During power-up, once IN and V_{DD} exceed their undervoltage-lockout thresholds, the DVR register is programmed with a value stored in the nonvolatile memory to set the VCOM voltage. The factory-default DVR value stored in the nonvolatile memory is 7F. See the *Programming Control Register (0Ch)*, *Write Only* section for details regarding changing the preset DVR value.

D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB

DVR REGISTER	VCOM OUTPUT VOLTAGE (V)
00h	-0.50
01h	-0.51
…	…
7Fh	-1.77
…	…
FEh	-3.04
FFh	-3.05

Enable Register (09h) R/W

The output enable functions performed by the EN and CEN pins can also be performed through I^2C commands by setting the function's corresponding enable bit in the Enable register.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CEN	EN

Each function's enable bit is ORed with the status of its corresponding enable pin to determine whether the function is to be performed. If I^2C control over the EN and CEN functions is desired, leave the EN and CEN pins unconnected or connect them to GND such that when:

- The EN bit is set to 1; the GVEE, NEG, POS, and GVDD power rails begin a power-up sequence. The sequence order and timing between the startup of each power rail is determined by the information stored in the t1–t4 Timing registers at the time the EN bit is set to 1.
- The EN bit is set to 0; the GVEE, NEG, POS, and GVDD begin a power-down/discharge sequence based on the information stored in the Timing registers. The sequence order and timing between the power-down of each power rail is determined by the information stored in the t5–t8 Timing registers at the time the EN bit is set to 0.
  - The CEN bit is set to 1; the VCOM output is enabled.
  - The CEN bit is set to 0; the VCOM output is discharged to ground.

During a fault condition, all bits in the Enable register are cleared (EN = CEN = 0). Driving the EN or CEN pins high or low has no effect on the EN or CEN settings in the Enable register.

Fault Register (0Ah) Read Only

During a fault condition, all outputs of the device are latched off, all bits in the Enable register are set to 0, and the corresponding bit of the fault condition is set in the Fault register (see the table below). After the fault condition is removed, the Fault register is cleared by cycling the V_{DD} supply.

The POK bit in the Fault register is not a fault indicator, but rather a status indicator that is asserted to 1 after FBNG, NEG, POS, and FBPG have all exceeded 80% of their regulation voltages and all soft-start periods have completed. The POK bit is set to 0 once the power-down sequence has been initiated by setting the EN bit to 0 or once a fault condition has occurred. The status of POK itself does not directly affect the status of EN or CEN bits.

Note: The temperature sensor DXN/DXP short-circuit and open-circuit "faults" are not latching faults that cause the IC to shut down and do not set the CEN or EN bits' status.

D7	D6	D5	D4	D3	D2	D1	D0
POK	OT	HVINNSC	HVINPSC	FBNG	HVINN	HVINP	FBPG

FBPG = GVDD undervoltage fault

HVINP = HVINP undervoltage fault

HVINN = HVINN undervoltage fault

FBNG = GVEE undervoltage fault

HVINPSC = HVINP short-circuit fault

HVINNSC = HVINN short-circuit fault

OT = Thermal shutdown

POK = Power-OK

HVINP Register (0Bh) R/W

The POS regulation voltage is determined by the boost converter's output regulation voltage (V_{HVINP}). The HVINP regulation voltage is set by using a resistor-divider network or by programming the corresponding value of the desired HVINP regulation voltage into the HVINP register through I^2C (see the table below). Programming the HVINP register to set the HVINP regulation voltage gives the flexibility to change the HVINP regulation voltage between each power-up sequence of the GVEE, NEG, POS, and GVDD rails and removes external components.

To set the HVINP regulation voltage through I^2C, connect the FBP pin to GND. With FBP connected to GND, the HVINP register is automatically loaded with 0Ah and the HVINP regulation voltage is set to +15V after IN and V_{DD} have exceeded their undervoltage-lockout thresholds. If another HVINP regulation voltage other than +15V is desired, write a new value to the HVINP register that corresponds to the desired HVINP regulation voltage after IN and V_{DD} have exceeded their undervoltage-lockout thresholds, but before EN is asserted high. The new HVINP regulation voltage is maintained until a new value is written to the HVINP register or the V_{DD} input power is cycled. After cycling V_{DD}, the HVINP register is again reloaded with 0Ah such that it is necessary to rewrite the HVINP register to change the HVINP regulation voltage to another voltage other than V_{HVINP} = 15V.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	MSB	Bit2	Bit1	LSB

The HVINP register can be programmed to provide a POS regulation voltage from 00h (V_{POS} = 5V) to 0Ch (V_{POS} = 17V) adjustable in 1V steps.

HVINP REGISTER	HVINP OUTPUT VOLTAGE (V)
00h	5
01h	6
...	...
0Ah	15
0Bh	16
0Ch	17

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Conversion Rate Control Byte (0Fh) R/W

The Conversion Rate register (0Fh) programs the time interval between conversions in the free-running auto-convert mode of the temperature sensors. This variable-rate control reduces the supply current in portable-equipment applications. The conversion rate control byte's POR state is 04h. The control mechanism looks only at the 3 LSBs of this register, so the upper 5 bits are "don't care" bits, which should be set to zero. The conversion rate tolerance is ±25% at any rate setting.

DATA	CONVERSION RATE (Hz)	AVERAGE SUPPLY CURRENT OF TEMP-SENSOR BLOCK (µA)
00h	0.0625	14
01h	0.125	18
02h	0.25	26
03h	0.5	41
04h	**1**	**72**
05h	2	133
06h	4	255
07h	8	500
08h to FFh	Depends on the 3 LSB	Depends on the 3 LSB

Valid A/D conversion results are available one total conversion time after the initiating conversion, whether the conversion is initiated through the Shutdown bit in the Configuration Register or initial power-up. Changing the conversion rate can also affect the delay until new results are available.

t1–t8 Timing Registers (10h–17h) R/W

Figure 5 shows the start-up and shutdown sequence of the power rails:

- The HVINP power rail begins its soft-start sequence once EN is driven high or the EN bit in the Enable register is set to 1.
- The HVINN power rail begins its soft-start sequence once the HVINP soft-start period has expired.
- The GVEE, NEG, POS, and GVDD power rails start up t1–t4ms after the expiration of the HVINN soft-start period.
- POK is asserted high after FBNG, NEG, POS, and FBPG have all exceeded 80% of their regulation voltages and all the corresponding power rails' soft-start periods have expired.
- Once EN is driven low or the EN bit in the Enable register is set to 0 (while the EN is disconnected or is connected to GND), POK is asserted low and each power rail is discharged at a time depending on the values stored in the timing registers (t5–t8). Approximately 512ms after EN is driven low, HVINP and HVINN are powered down but not discharged.

The power-up/power-down sequence and timing between the GVEE, NEG, POS, and GVDD power rails can be set by programming the t1–t8 registers with corresponding values according to the table below.

D7	D6	D5	D4	D3	D2	D1	D0
128ms	64ms	32ms	16ms	8ms	4ms	2ms	1ms

The binary value stored in a register directly corresponds to the time in ms.

VALUE STORED IN A TIMING REGISTER (t1–t8)	TIME (ms)
00h	0
01h	1
...	...
FEh	254
FFh	255

During power-up of the device, once IN and V_{DD} exceed their undervoltage-lockout thresholds, the t1–t8 registers are loaded with values stored in the nonvolatile memory to preset the t1–t8 timing. The factory-default timing settings in the nonvolatile memory are:

- t1 = t5 = 30ms
- t2 = t6 = 60ms
- t3 = t7 = 90ms
- t4 = t8 = 120ms

To change the preset t1–t8 timing, see the *Programming Control Register (0Ch), Write Only* section.

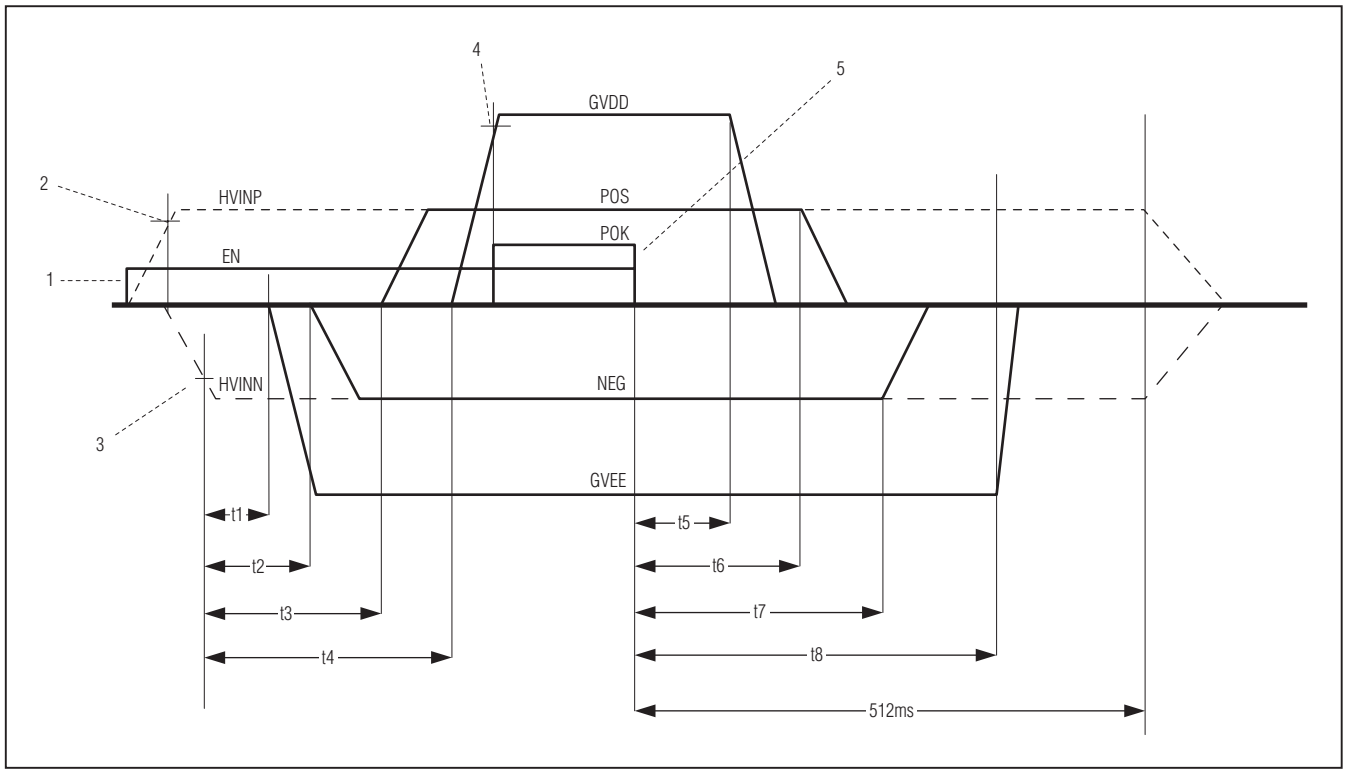

Figure 5. Adjustable Power-Up and Power-Down Sequencing

Programming Control Register (0Ch), Write Only

The Programming Control register (PCR) allows the user to update the nonvolatile memory containing the values used to set the DVR and Timing registers after initial power-up of the IC (after V_{DD} and IN both exceed their undervoltage-lockout thresholds).

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	Timing	DVR

To change the nonvolatile memory values that preset the VCOM voltage, set EN to high to bring up the power rails. After POK is asserted high, write the value corresponding to the desired VCOM voltage setting into the DVR register. After the DVR register has been updated, write 1 to D0 of the PCR to update the nonvolatile memory with the current value stored in the DVR register. The nonvolatile memory containing the power-up DVR setting can be changed up to 30 times. The I^2C bus returns NACK if the DVR nonvolatile memory is attempted to be programmed more than 30 times.

To change the nonvolatile memory values that preset the power-up and power-down timing between the power rails, set EN to high to bring up the power rails. After POK is asserted high, write to all t1–t8 registers with the values corresponding to the desired t1–t8 timing between power rails. The t1–t8 values cannot be stored to the nonvolatile memory independently and all eight Timing registers must be written to at least once before attempting to update the nonvolatile memory with any new values, even if not all values need to be changed from the current values stored in the nonvolatile memory. Once all the Timing registers have been written to at least once, write 1 to D1 of the PCR to update the nonvolatile memory with the current values stored in all t1–t8 Timing registers. The nonvolatile memory containing the power-up and power-down timing settings can be changed up to three times. The I^2C bus returns NACK if the t1–t8 nonvolatile memory is attempted to be programmed more than three times.

Note: V_{POS} needs to be greater than 7.3V in order to successfully program the nonvolatile memory.

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PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the inner loop area created by the boost converter high-switching current connections. Place D1 and C3 close to the IC such that the traces connecting the LXP pin to the anode of D1, the cathode of D1 to C3, and C3 to the PGND pin are kept as short as possible to minimize the loop area contained within these connections. Make these connections with short, wide traces.
- Minimize the inner loop area created by the buck-boost converter high-switching current connections. Place C6, C7, and D2 close to the IC such that the traces connecting C6 to the INN pin, the LXN pin to the cathode of D2, the anode of D2 to C7, and C6 ground connection to C7 are kept as short as possible to minimize the loop area contained within these connections. Make these connections with short, wide traces.
- Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power ground island (PGND) consisting of the PGND pin, the input and output capacitor ground connections, the charge-pump capacitor ground connections, and the buck-boost inductor ground connection. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground plane (GND) consisting of the GND pin, all the feedback-divider ground connections, the IN, V_{DD}, and REF bypass capacitor ground connections, and the device's exposed backside paddle.
- Connect the GND and PGND islands by connecting the PGND pin directly to the exposed backside paddle. Make no other connections between these separate ground planes.
- Place the feedback-voltage-divider resistors as close as possible to their respective feedback pins. Keep the traces connecting the feedback resistors to their respective feedback pins as short as possible. Placing the resistors far away causes the feedback trace to become an antenna that can pick up switching noise. Care should be taken to avoid running any feedback trace near the LXP, LXN, DP, or DN switching nodes.
- Place the IN, V_{DD}, and REF bypass capacitors as close as possible to the IC. The ground connections of the IN, V_{DD}, and REF bypass capacitors should be connected directly to the analog ground plane or directly to the GND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Keep sensitive signals away from the LXP, LXN, DP, and DN switching nodes. Use DC traces as a shield if necessary.

Refer to the MAX17135 evaluation kit for an example of proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255N+1	21-0140	90-0015

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/11	Initial release	—
1	12/11	*Typical Operating Circuit* values updated	12
2	5/12	*Inverting Regulator* section in EC table changed to meet QA standard	3