Data Sheet May 1999 File Number 2758.4

Digital Filter

The HSP43881 is a video speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 8 x 8-bit multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8 bits. The HSP43881 has a maximum sample rate of 30MHz. The effective multiply accumulate (mac) rate is 240MHz.

The HSP43881 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 30MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of $^1/_2$, $^1/_3$ or $^1/_4$ the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and N x N spatial correlations/convolutions for image processing applications.

Features

- Eight Filter Cells
- 0MHz to 30MHz Sample Rate
- 8-Bit Coefficients and Signal Data
- 26-Bit Accumulator Per Stage
- Filter Lengths Over 1000 Taps
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

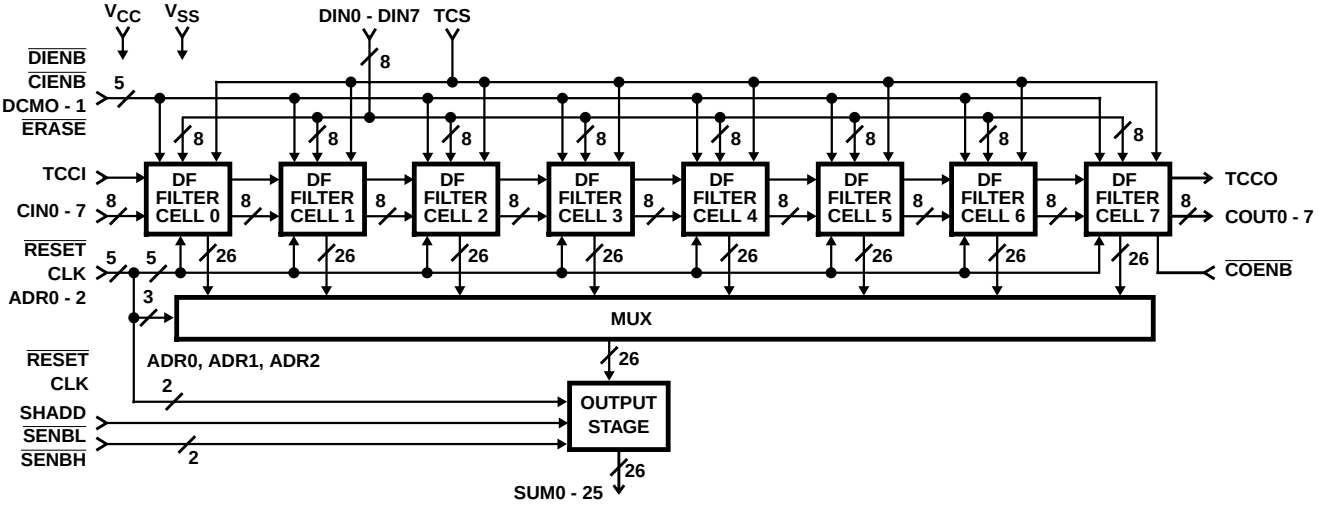
Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP43881JC-20	0 to 70	84 Ld PLCC	N84.1.15
HSP43881JC-25	0 to 70	84 Ld PLCC	N84.1.15
HSP43881JC-30	0 to 70	84 Ld PLCC	N84.1.15
HSP43881GC-20	0 to 70	85 Ld PGA	G85.A
HSP43881GC-25	0 to 70	85 Ld PGA	G85.A
HSP43881GC-30	0 to 70	85 Ld PGA	G85.A

Block Diagram



Pinouts

85 PIN GRID ARRAY (PGA)
TOP VIEW, PINS DOWN

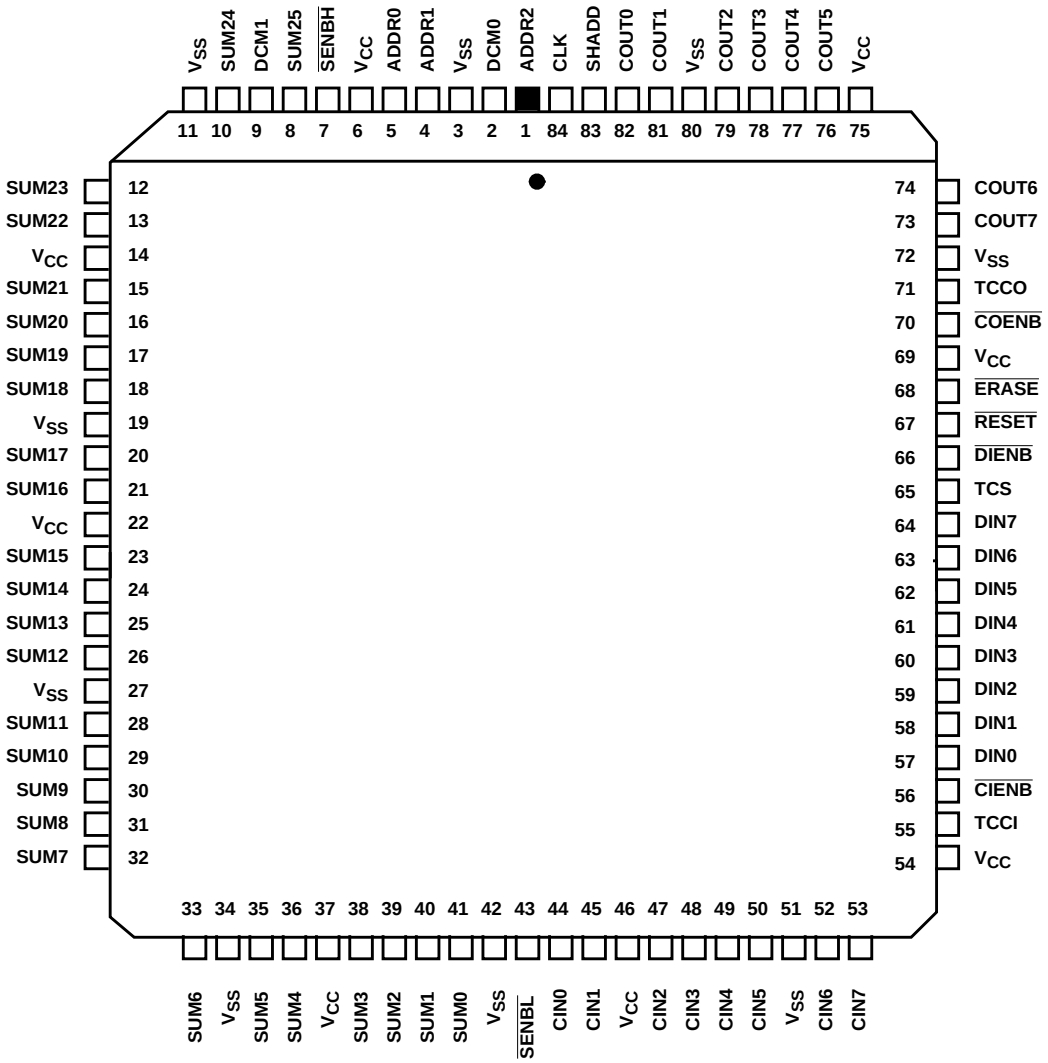
	1	2	3	4	5	6	7	8	9	10	11
A	V_{SS}	$\overline{COENB}$	V_{CC}	$\overline{RESET}$	DIN7	DIN6	DIN3	DIN0	TCCI	V_{CC}	V_{SS}
B	V_{CC}	COUT7	TCCO	$\overline{ERASE}$	TCS	DIN1	DIN2	$\overline{CIENB}$	CIN7	CIN6	CIN4
C	COUT5	COUT6	ALIGN PIN		$\overline{DIENB}$	DIN5	DIN4			CIN5	CIN3
D	COUT3	COUT4								CIN2	V_{CC}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{SENBL}$
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
K	$\overline{SENBH}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9

HSP43881
TOP VIEW, PINS UP

	1	2	3	4	5	6	7	8	9	10	11
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V_{CC}	SUM13	V_{SS}	SUM11	SUM9
K	$\overline{SENBH}$	SUM24	V_{SS}	V_{CC}	SUM19	V_{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
J	V_{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V_{SS}
H	ADR1	ADR0								SUM5	SUM4
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
F	V_{SS}	COUT0	SHADD						SUM0	V_{CC}	V_{SS}
E	COUT1	V_{SS}	COUT2						CIN1	CIN0	$\overline{SENBL}$
D	COUT3	COUT4								CIN2	V_{CC}
C	COUT5	COUT6	ALIGN PIN		$\overline{DIENB}$	DIN5	DIN4			CIN5	CIN3
B	V_{CC}	COUT7	COUT8	$\overline{ERASE}$	DIN8	DIN1	DIN2	$\overline{CIENB}$	CIN7	CIN6	CIN4
A	V_{SS}	$\overline{COENB}$	V_{CC}	$\overline{RESET}$	DIN7	DIN6	DIN3	DIN0	CIN8	V_{CC}	V_{SS}

Pinouts (Continued)

84 LEAD PLCC PACKAGE
BOTTOM VIEW



NOTE: An overbar on a signal name represents an active LOW signal.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	A3, A10, B1, D11, F10, J1, K4, L7		+5V Power Supply Input.
V_{SS}	A1, A11, E2, F1, E11, H11, K3, K6, L9		Power Supply Ground Input.
CLK	G3	I	The CLK input provides the DF system sample clock. The maximum clock frequency is 30MHz.
DIN0-7	A58, B67, C67	I	These eight inputs are the data sample input bus. Eight bit data samples are synchronously loaded through these pins to the X register of each filter cell simultaneously. The $\overline{\text{DIENB}}$ signal enables loading, which is synchronous on the rising edge of the clock signal.
TCS	B5	I	The TCS input determines the number system interpretation of the data input samples on pins DIN0-7 as follows: TCS = Low $\rightarrow$ Unsigned Arithmetic. TCS = High $\rightarrow$ Two's Complement Arithmetic. The TCS signal is synchronously loaded into the X register in the same way as the DIN0-7 inputs.
$\overline{\text{DIENB}}$	C5	I	A low on this enables the data sample input bus (DIN0-7) to all the filter cells. A rising edge of the CLK signal occurring while $\overline{\text{DIENB}}$ is low will load the X register of every filter cell with the 8-bit value present on DIN0-7. A high on this input forces all the bits of the data sample input bus to zero; a rising CLK edge when $\overline{\text{DIENB}}$ is high will load the X register of every filter cell with all zeros. This signal is latched inside the DF, delaying its effect by one clock internal to the DF. Therefore, it must be low during the clock cycle immediately preceding presentation of the desired data on the DIN0-7 inputs. Detailed operation is shown in later timing diagrams.
CIN0-7	B9-11, C10-11, D10, E9-10	I	These eight inputs are used to input the 8-bit coefficients. The coefficients are synchronously loaded into the C register of filter CELL 0 if a rising edge of CLK occurs while $\overline{\text{CIENB}}$ is low. The $\overline{\text{CIENB}}$ signal is delayed by one clock as discussed below.
TCCI	A9	I	The TCCI input determines the number system interpretation of the coefficient inputs on pins CIN07 as follows: TCCI = LOW E Unsigned Arithmetic. TCCI = HIGH E Two's Complement Arithmetic. The TCCI signal is synchronously loaded into the C register in the same way as the CIN0-7 inputs.
$\overline{\text{CIENB}}$	B8	I	A low on this input enable the C register of every filter cell and the D registers (decimation) of every filter cell according to the state of the DCM0-1 inputs. A rising edge of the CLK signal occurring while $\overline{\text{CIENB}}$ is low will load the C register and appropriate D registers with the coefficient data present at their inputs. This provides the mechanism for shifting the coefficients from cell to cell through the device. A high on this input freezes the contents of the C register and the D registers ignoring the CLK signal. This signal is latched and delayed by one clock internal to the DF. Therefore, it must be low during the clock cycle immediately preceding presentation of the desired coefficient of the CIN0-7 inputs. Detailed operation is shown in the Timing Diagrams Section.
COUT0-7	B2, C1-2, D1-2, E1, E3, F2	O	These eight three-state outputs are used to output the 8-bit coefficients from filter cell 7. These outputs are enabled by the $\overline{\text{COENB}}$ signal low. These outputs may be tied to the CIN0-7 inputs of the same DF to recirculate the coefficients, or they may be tied to the CIN0-7 inputs of another DF to cascade DFs for longer filter lengths.
TCCO	B3	O	The TCCO three-state output determines the number system representation of the coefficients output on COUTO-7. It tracks the TCCI signal to this same DF. It should be tied to the TCCI input of the next DF in a cascade of DFs for increased filter lengths. This signal is enabled by $\overline{\text{COENB}}$ low.
$\overline{\text{COENB}}$	A2	I	A low on the $\overline{\text{COENB}}$ input enables the COUT0-7 and the TCCO output. A high on this input places all these outputs in their high impedance state.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
DCM0-1	G2, L1		These two inputs determine the use of the internal decimation registers as follows: DCM1 DCM0 Decimation Function 0 0 Decimation Registers not used. 0 1 One Decimation Register is used. 1 0 Two Decimation Registers are used. 1 1 Three Decimation Registers are used. The coefficients pass from cell to cell at a rate determined by the number of decimation registers used. When no decimation registers are used, coefficients move from cell to cell on each clock. When one decimation register is used, coefficients move from cell to cell on every other clock, etc. These signals are latched and delayed by one clock internal to the DF.
SUM0-25	J2, J5-8, J10, K2, K5-11, L-26, L8, L10-11	O	These 26 three-state outputs are used to output the results of the internal filter cell computations. Individual filter cell results or the result of the shift and add output stage can be output. If an individual filter cell result is to be output, the ADR0-2 signals select the filter cell result. The SHADD signal determines whether the selected filter cell result or the output stage adder result is output. The signals $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ enable the most significant and least significant bits of the SUM0-25 result, respectively. Both $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ may be enabled simultaneously if the system has a 26-bit or larger bus. However, individual enables are provided to facilitate use with a 16-bit bus.
$\overline{\text{SENBH}}$	K1	I	A low on this input enables result bits SUM16-25. A high on this input places these bits in their high impedance state.
$\overline{\text{SENBL}}$	E11	I	A low on this input enables result bits SUM0-15. A high on this input places these bits in their high impedance state.
ADR0-2	G1, H1-2	I	These inputs select the one cell whose accumulator will be read through the output bus (SUM0-25) or added to the output stage accumulator. They also determine which accumulator will be cleared when $\overline{\text{ERASE}}$ is low. For selection of which accumulator to read through the output bus (SUM0-25) or which to add to the output stage accumulator, these inputs are latched in the DF and delayed by one clock internal to the device. If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock, when ADR0-1 selects the cell, will be output. This does not hinder normal operation since the ADR0-1 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.
SHADD	F3	I	The SHADD input controls the activation of the shift-and-add operation in the output stage. This signal is latched in the DF and delayed by one clock internal to the device. A detailed explanation is given in the DF Output Stage Section.
$\overline{\text{RESET}}$	A4	I	A low on this input synchronously clears all the internal registers, except the cell accumulators. It can be used with $\overline{\text{ERASE}}$ to also clear all the accumulators simultaneously. This signal is latched in the DF and delayed by one clock internal to the DF.
$\overline{\text{ERASE}}$	B4	I	A low on this input synchronously clears the cell accumulator selected by the ADR0-1 signals. If $\overline{\text{RESET}}$ is also low simultaneously, all cell accumulators are cleared.
ALIGN PIN	C3		Used for aligning chip in socket or printed circuit board. Must be left as a no connect in circuit.

Functional Description

The Digital Filter Processor (DF) is composed of eight filter cells cascaded together and an output stage for combining or selecting filte5r cell outputs (See Block Diagram). Each filter cell contains a multiplier accumulator and several registers (Figure 1). Each 8-bit coefficient is multiplied by an 8-bit data sample, with the result added to the 26-bit accumulator contents. The coefficient output of each cell is cascaded to the coefficient input of the next cell to its right.

DF Filter Cell

An 8-bit coefficient (CIN0-7) enters each cell through the C register on the left and exits the cell on the right as signals COUT0-7. With no decimation, the coefficient moves directly from the C register to the output, and is valid on the clock following its entrance. When decimation is selected the coefficient exit is delayed by 1, 2 or 3 clocks by passing through one or more decimation registers (D1, D2 or D3).

The combination of D registers through which the coefficient passes is determined by the state of DCM0 and DCM1. The output signals (COUT0-7) are connected to the CIN0-7 inputs of the next cell to its right. The COENB input signal enables the COUT0-7 outputs of the right most cell to the COUT-07 pins of the device.

The C and D registers are enabled for loading by CIENB. Loading is synchronous with CLK when CIENB is low. Note that

CIENB is latched internally. It enables the register for loading after the next CLK following the onset of CIENB low. Actual loading occurs on the second CLK following the onset of CIENB low. Therefore, CIENB must be low during the clock cycle immediately preceding presentation of the coefficient on the CIN0-7 inputs. In most basic FIR operations, CIENB will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When CIENB is high, the coefficients are frozen.

These registers are cleared synchronously under control of RESET, which is latched and delayed exactly like CIENB. The output of the C register (C0-8) is one input to 8 x 8 multiplier.

The other input to the 8 x 8 multiplier comes from the output of the X register. This register is loaded with a data sample from the device input signals DIN0-7 discussed above. The X register is enabled for loading by DIENB. Loading is synchronous with CLK when DIENB is low. Note that DIENB is latched internally. It enables the register for loading after the next CLK following the onset of DIENB low. Actual loading occurs on the second CLK following the onset of DIENB low; therefore, DIENB must be low during the clock cycle immediately preceding presentation of the data sample on the DIN0-7 inputs. In most basic FIR operations, DIENB will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When DIENB is high, the X register is loaded with all zeros.

The multiplier is pipelined and is modeled as a multiplier core followed by two pipeline registers, MREG0 and MREG1 (Figure 1). The multiplier output is sign extended and input as one operand of the 26-bit adder. The other adder operand is the output of the 26-bit accumulator. The adder output is loaded synchronously into both the accumulator and the TREG.

The TREG loading is disabled by the cell select signal, CELLn, where n is the cell number. The cell select is decoded from the ADR0-2 signals to generate the TREG load enable. The cell select is inverted and applied as the load enable to the TREG. Operation is such that the TREG is loaded whenever the cell is not selected. Therefore, TREG is loaded every clock except the clock following cell selection. The purpose of the TREG is to hold the result of a sum of products calculation during the clock when the accumulator is cleared to prepare for the next sum of products calculation. This allows continuous accumulation without wasting clocks.

The accumulator is loaded with the adder output every clock unless it is cleared. It is cleared synchronously in two ways. When $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are both low, the accumulator is cleared along with all other registers on the device. Since $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ are latched and delayed one clock internally, clearing occurs on the second CLK following the onset of both $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ low.

The second accumulator clearing mechanism clears a single accumulator in a selected cell. The cell select signal, CELLn, decoded from ADR0-2 and the $\overline{\text{ERASE}}$ signal enable clearing of the accumulator on the next CLK.

The $\overline{\text{ERASE}}$ and $\overline{\text{RESET}}$ signals clear the DF internal registers and states as follows:

$\overline{\text{ERASE}}$	$\overline{\text{RESET}}$	CLEARING EFFECT
1	1	No clearing occurs, internal state remains same.
1	0	$\overline{\text{RESET}}$ only active, all registers except accumulators are cleared, including the internal pipeline registers.
0	1	$\overline{\text{ERASE}}$ only active, the accumulator whose address is given by the ADR0-2 inputs is cleared.
0	0	Both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ active, all accumulators, as well as all other registers are cleared.

The DF Output Stage

The output stage consists of a 26-bit adder, 26-bit register, feedback multiplexer from the register to the adder, an output multiplexer and a 26-bit three-state driver stage (Figure 2).

The 26-bit output adder can add any filter cell accumulator result to the 18 most significant bits of the output buffer. This result is stored back in the output buffer. This operation takes place in one clock period. The eight LSBs of the output buffer are lost. The filter cell accumulator is selected by the ADR0-2 inputs.

The 18 MSBs of the output buffer actually pass through the zero mux on their way to the output adder input. The zero mux is controlled by the SHADD input signal and selects either the output buffer 18 MSBs or all zeros for the adder input. A low on the SHADD input selects zero. A high on the SHADD input selects the output buffer MSBs, thus, activating the shift and add operation. The SHADD signal is latched and delayed by one clock internally.

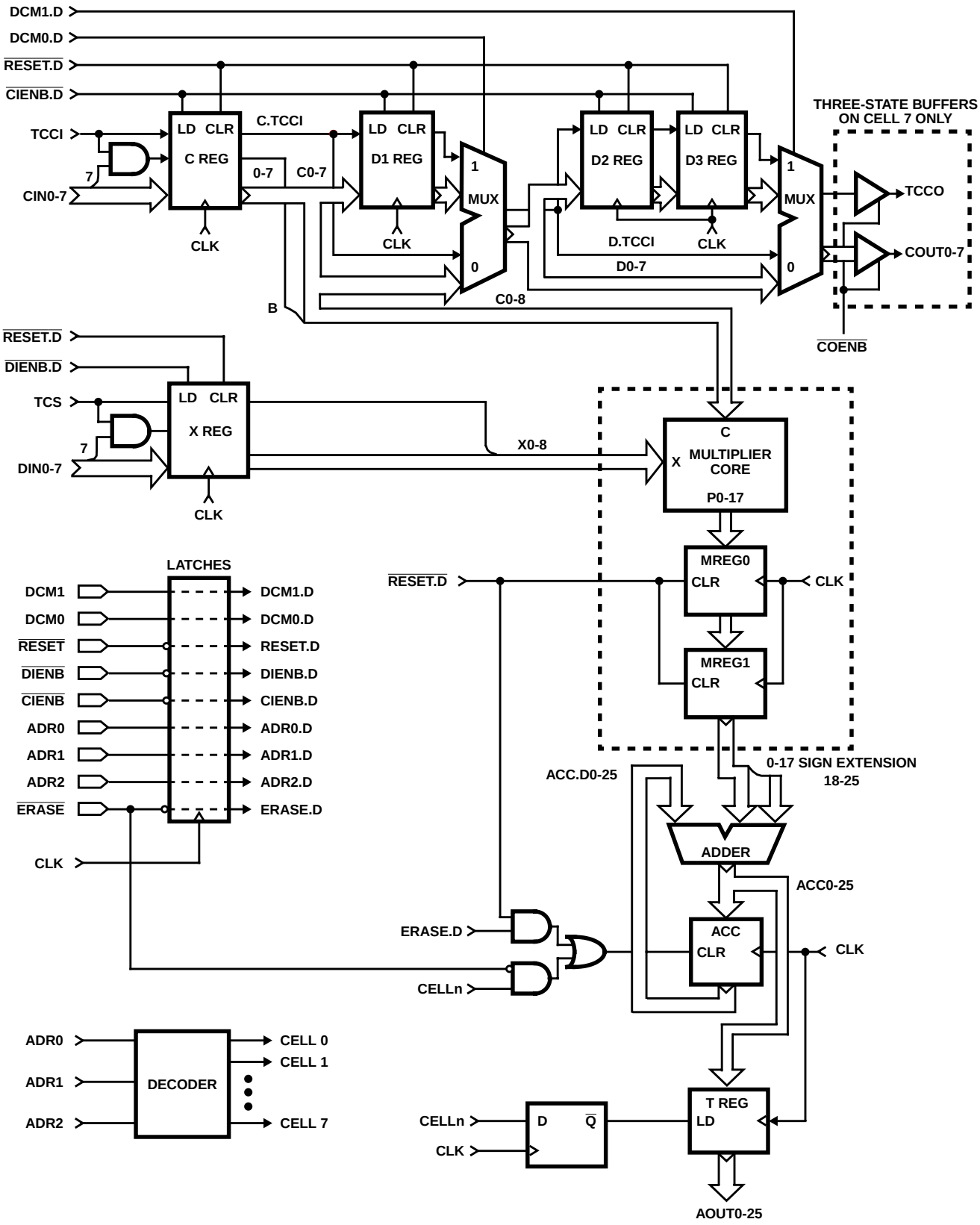


FIGURE 1. FILTER CELL

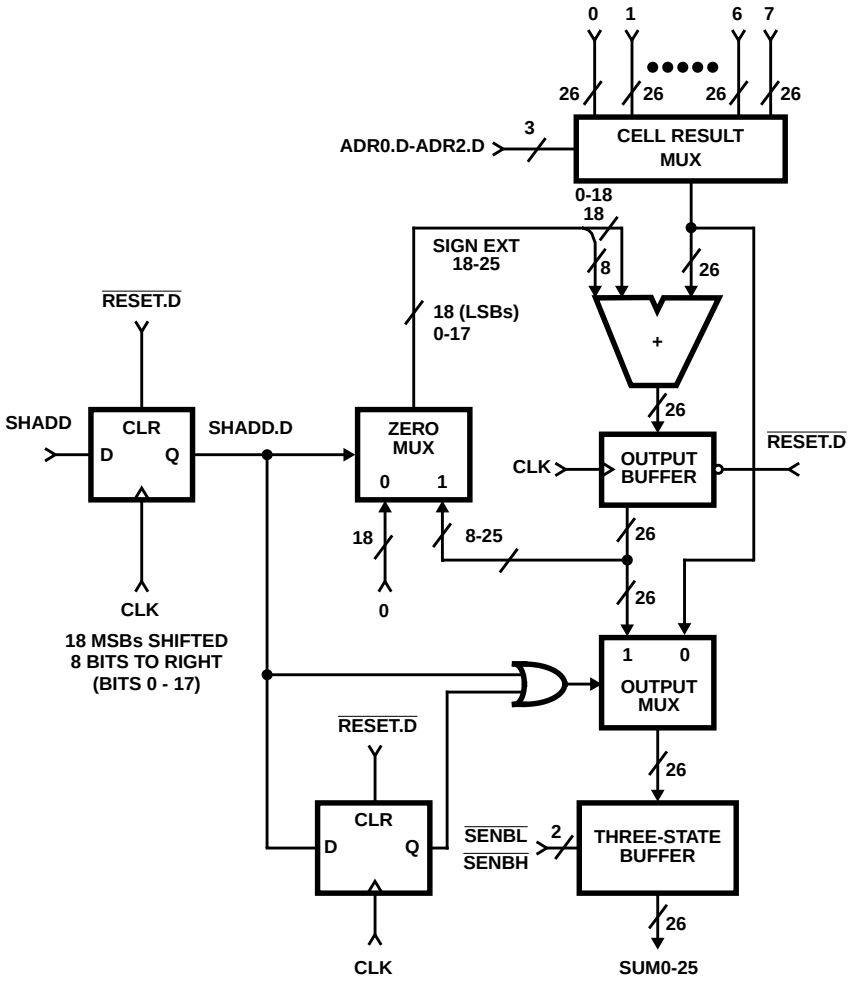


FIGURE 2. DF OUTPUT STAGE

The 26 least significant bits (LSBs) from either a cell accumulator or the output buffer are output on the SUM0-25 bus. The output mux determines whether the cell accumulator selected by ADR0-2 or the output buffer is output to the bus. This mux is controlled by the SHADD input signal. Control is based on the state of the SHADD during two successive clocks; in other words, the output mux selection contains memory. If SHADD is low during a clock cycle and was low during the previous clock, the output mux selects the contents of the filter cell accumulator addressed by ADR0-2. Otherwise the output mux selects the contents of the output buffer.

If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock when ADR0-2 selects the cell will be output. This does not hinder normal FIR operation since the ADR0-2 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

The SUM0-25 output bus is controlled by the SENBH and SENBL signals. A low on SENBL enables bits SUM0-15. A low on SENBH enables bits SUM16-25. Thus, all 26 bits can be output simultaneously if the external system has a 26-bit or larger bus. If the external system bus is only 16 bits, the bits can be enabled in two groups of 16 and 10 bits (sign extended).

DF Arithmetic

Both data samples and coefficients can be represented as either unsigned or two's complement numbers. The TCS and TCCI inputs determine the type of arithmetic representation. Internally all values are represented by a 9-bit two's complement number. The value of the additional ninth bit depends on the arithmetic representation selected. For two's complement arithmetic, the sign is extended into the ninth bit. For unsigned arithmetic, bit-9 is 0.

The multiplier output is 18 bits and the accumulator is 26 bits. The accumulator width determines the maximum possible number of terms in the sum of products without

overflow. The maximum number of terms depends also on the number system and the distribution of the coefficient and data values. Then maximum numbers of terms in the sum products are:

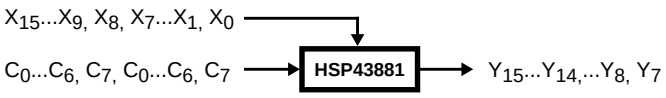
NUMBER SYSTEM	MAX # OF TERMS
Two Unsigned Vectors	1032
Two Two's Complement: • Two Positive Vectors • Negative Vectors • One Positive and One Negative Vector	 2080 2047 2064
One Unsigned and One Two's Complement Vector: • Positive Two's Complement Vector • Negative Two's Complement Vector	 1036 1028

For practical FIR filters, the coefficients are never all near maximum value, so even larger vectors are possible in practice.

Basic FIR Operation

A simple, 30MHz 8-tap filter example serves to illustrate more clearly the operation of the DF. The sequence table (Table 1) shows the results of the multiply accumulate in each cell after each clock. The coefficient sequence, Cn, enters the DF on the left and moves from left to right through the cells. The data sample sequence, Xn, enters the DF from the top, with each cell receiving the same sample simultaneously. Each cell accumulates the sum of products for one output point. Eight sums of products are calculated simultaneously, but staggered in time so that a new output is available every system clock.

TABLE 1. 30MHz, 8-TAP FIR FILTER SEQUENCE



CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
0	$C_7 \times X_0$	0	0	0					-
1	$+C_6 \times X_1$	$C_7 \times X_1$	0	0					-
2	$+C_5 \times X_2$	$+C_6 \times X_2$	$C_7 \times X_2$	0					-
3	$+C_4 \times X_3$	$+C_5 \times X_3$	$+C_6 \times X_3$	$C_7 \times X_3$					-
4	$+C_3 \times X_4$	$+C_4 \times X_4$	$+C_5 \times X_4$	$+C_6 \times X_4$	$C_7 \times X_4$				-
5	$+C_2 \times X_5$	$C_3 \times X_5$	$+C_4 \times X_5$	$+C_5 \times X_5$	$+C_6 \times X_5$	$C_7 \times X_5$			-
6	$+C_1 \times X_6$	$+C_2 \times X_6$	$+C_3 \times X_6$	$+C_4 \times X_6$	$+C_5 \times X_6$	$+C_6 \times X_6$	$C_7 \times X_6$		-
7	$+C_0 \times X_7$	$+C_1 \times X_7$	$+C_2 \times X_7$	$+C_3 \times X_7$	$+C_4 \times X_7$	$+C_5 \times X_7$	$+C_6 \times X_7$	$C_7 \times X_7$	Cell 0 (Y7)
8	$C_7 \times X_8$	$+C_0 \times X_8$	$+C_1 \times X_8$	$+C_2 \times X_8$	$+C_3 \times X_8$	$+C_4 \times X_8$	$+C_5 \times X_8$	$+C_6 \times X_8$	Cell 1 (Y8)
9	$+C_6 \times X_9$	$C_7 \times X_9$	$+C_0 \times X_9$	$+C_1 \times X_9$	$+C_2 \times X_9$	$+C_3 \times X_9$	$+C_4 \times X_9$	$+C_5 \times X_9$	Cell 2 (Y9)
10	$+C_5 \times X_{10}$	$+C_6 \times X_{10}$	$C_7 \times X_{10}$	$+C_0 \times X_{10}$	$+C_1 \times X_{10}$	$+C_2 \times X_{10}$	$+C_3 \times X_{10}$	$+C_4 \times X_{10}$	Cell 3 (Y10)
11	$+C_4 \times X_{11}$	$+C_5 \times X_{11}$	$+C_6 \times X_{11}$	$C_7 \times X_{11}$	$+C_0 \times X_{11}$	$+C_1 \times X_{11}$	$+C_2 \times X_{11}$	$+C_3 \times X_{11}$	Cell 4 (Y11)
12	$+C_3 \times X_{12}$	$+C_4 \times X_{12}$	$+C_5 \times X_{12}$	$+C_6 \times X_{12}$	$C_7 \times X_{12}$	$+C_0 \times X_{12}$	$+C_1 \times X_{12}$	$+C_2 \times X_{12}$	Cell 5 (Y12)
13	$+C_2 \times X_{13}$	$+C_3 \times X_{13}$	$+C_4 \times X_{13}$	$+C_5 \times X_{13}$	$+C_6 \times X_{13}$	$C_7 \times X_{13}$	$+C_0 \times X_{13}$	$+C_1 \times X_{13}$	Cell 6 (Y13)
14	$+C_1 \times X_{14}$	$+C_2 \times X_{14}$	$+C_3 \times X_{14}$	$+C_4 \times X_{14}$	$+C_5 \times X_{14}$	$+C_6 \times X_{14}$	$+C_7 \times X_{14}$	$+C_0 \times X_{14}$	Cell 7 (Y14)
15	$+C_0 \times X_{15}$	$+C_1 \times X_{15}$	$+C_2 \times X_{15}$	$+C_3 \times X_{15}$	$+C_4 \times X_{15}$	$+C_5 \times X_{15}$	$+C_6 \times X_{15}$	$C_7 \times X_{15}$	Cell 0 (Y15)

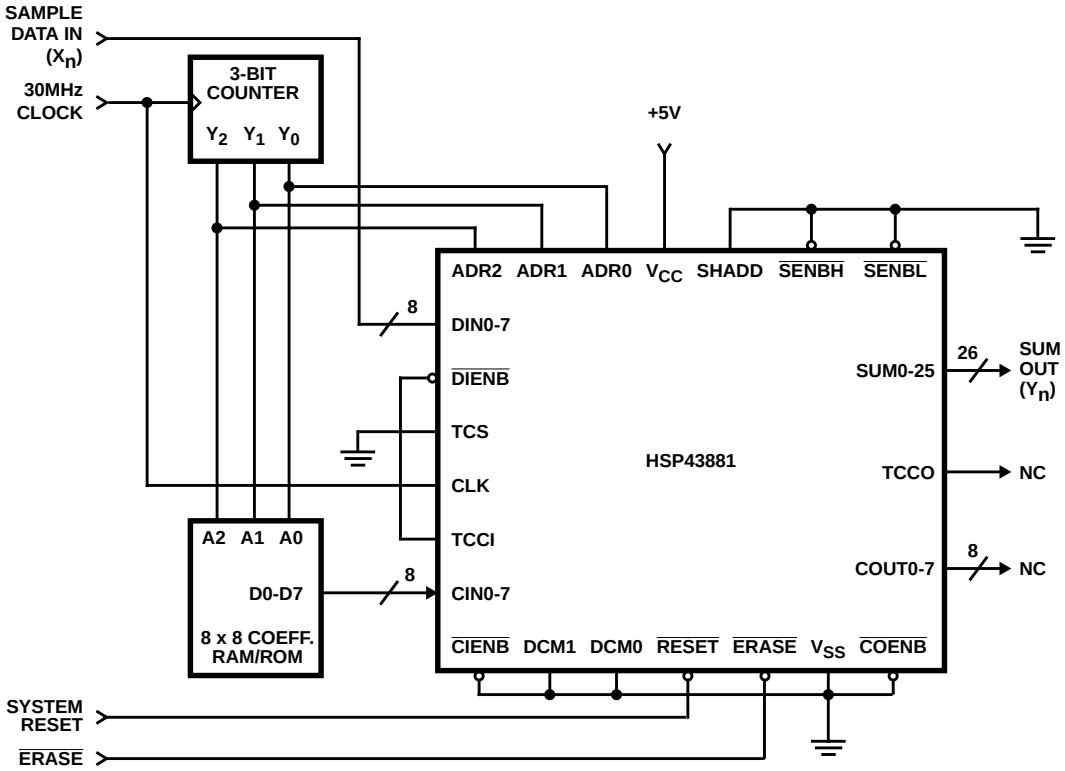


FIGURE 3. 30MHZ, 8 TAP FIR FILTER APPLICATION SCHEMATIC

Detailed operation of the DF to perform a basic 8-tap, 8-bit coefficient, 8-bit data, 30MHz FIR filter is best understood by observing the schematic (Figure 3) and timing diagram (Figure 4). The internal pipeline length of the DF is four (4) clock cycles, corresponding to the register levels CREG (or XREG), MREG0, MREG1, and TREG (Figures 1 and 2). Therefore, the delay from presentation of data and coefficients at the DIN0-7 and CIN0-7 inputs to a sum appearing at the SUM0-25 output is:

k + Td

Where:

k = filter length

Td = 4, the internal pipeline delay of DF

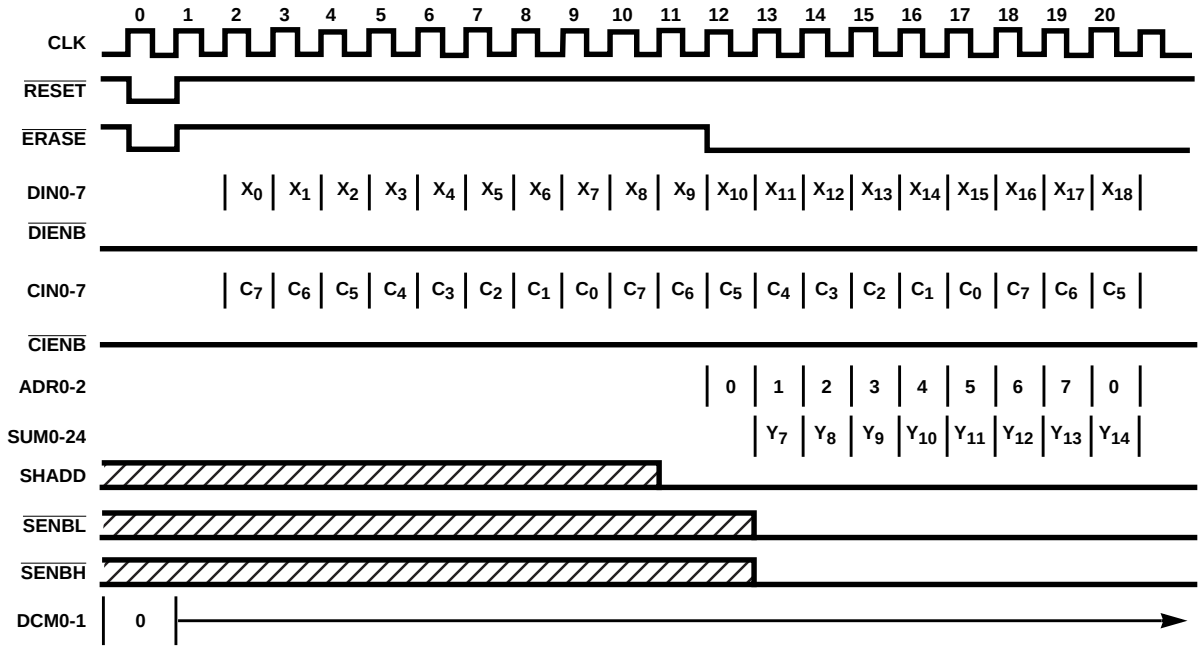
After the pipeline has filled, a new output sample is available every clock. The delay to last sample output from last sample input is Td.

The output sums, Yn, shown in the Timing Diagram are derived from the sum of products equation:

Y(n) = C(0) x X(n) + C(1) x X(n1) + C(2) x X(n -2) + C(3) x X(n -3) + C(4) x X(n -4) + C(5) x X(n -5) + C(6) x X(n -6) + C(7) x X(n -7)

Extended FIR Filter Length

Filter lengths greater that eight taps can be created by either cascading together multiple DF devices or “reusing” a single device. Using multiple devices, an FIR filter of over 1000-taps can be constructed to operate at a 30MHz sample rate. Using a single device clocked at 30MHz, a FIR filter of over 1000 taps can be constructed to operate at less than a 30MHz sample rate. Combinations of these two techniques are also possible.



$$Y_N = \sum_{K=0}^{7} C_K \times X_{N-K}$$

FIGURE 4. 30MHz, 8-TAP FIR FILTER TIMING

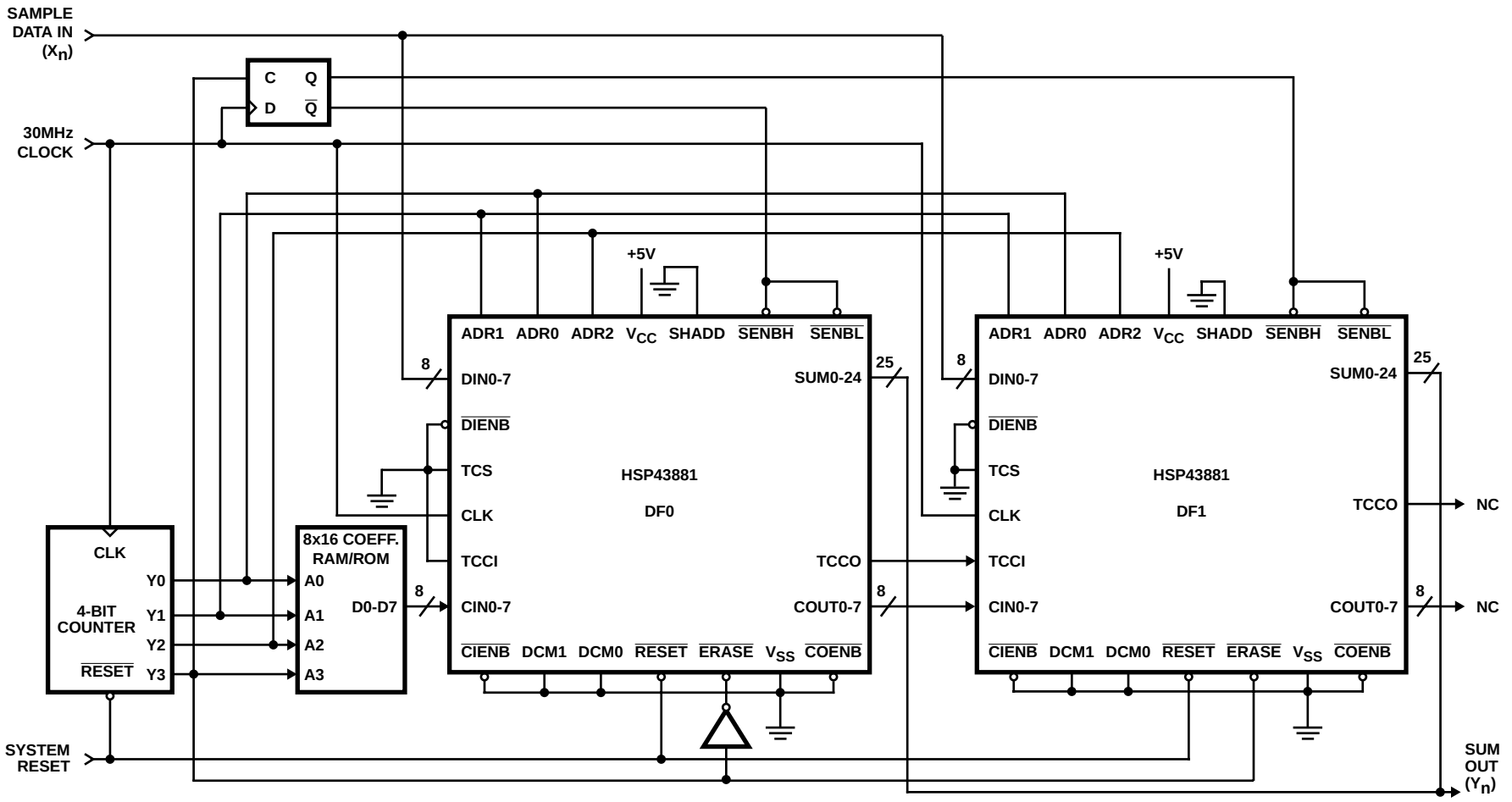


FIGURE 5. 30MHz, 16-TAP FIR FILTER CASCADE APPLICATION SCHEMATIC

Cascade Configuration

To design a filter length L>8, L/8 DFs are cascaded by connecting the COUT0-7 outputs of the (i)th DF to the CIN0-7 inputs of the (i+1)th DF. The DIN0-7 inputs and SUM0-25 outputs of all the DFs are also tied together. A specific example of two cascaded DFs illustrates the technique (Figure 5). Timing (Figure 6) is similar to the simple 8-tap FIR, except the $\overline{\text{ERASE}}$ and $\overline{\text{SENBL}}$/$\overline{\text{SENBH}}$ signals must be enabled independently for the two DFs in order to clear the correct accumulators and enable the SUM0-25 output signals at the proper times.

Single DF Configuration

Using a single DF, a filter of length L>8 can be constructed by processing in L/8 passes as illustrated in the following table (Table 2) for a 16-tap FIR. Each pass is composed of Tp = 7 + L cycles and computes eight output samples. In pass i, the sample with indices i*8 to i*8 +(L1) enter the DIN0-7 inputs. The coefficients C_0 -C_{L-1} enter the CIN0-7 inputs, followed by seven zeros. As these zeros are entered, the result samples are output and the accumulators reset. Initial filing of the pipeline is not shown in this sequence table. Filter outputs can be put through a FIFO to even out the sample rate.

Extended Coefficient and Data Sample Word Size

The sample and coefficient word size can be extended by utilizing several DFs in parallel to get the maximum sample rate or a single DF with resulting lower sample rates. The technique is to compute partial products of 8 x 8 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders (at full speed) or with the DF's shift and add mechanism contained in its output stage (at reduced speed).

Decimation/Resampling

The HSP43881 DF provides a mechanism for decimating by factors of 2, 3, or 4. From the DF filter cell block diagram (Figure 1), note the three D registers and two multiplexers in the coefficient path through the cell. These allow the coefficients to be delayed by 1, 2, or 3 clocks through the cell. The sequence table (Table 3) for a decimate by two filter illustrates the technique (internal cell pipelining ignored for simplicity).

Detailed timing for a 30MHz input sample rate, 15MHz output sample rate (i.e., decimate by two), 16-tap FIR filter, including pipelining, is shown in Figure 7. This filter requires only a single HSP43881 DF.

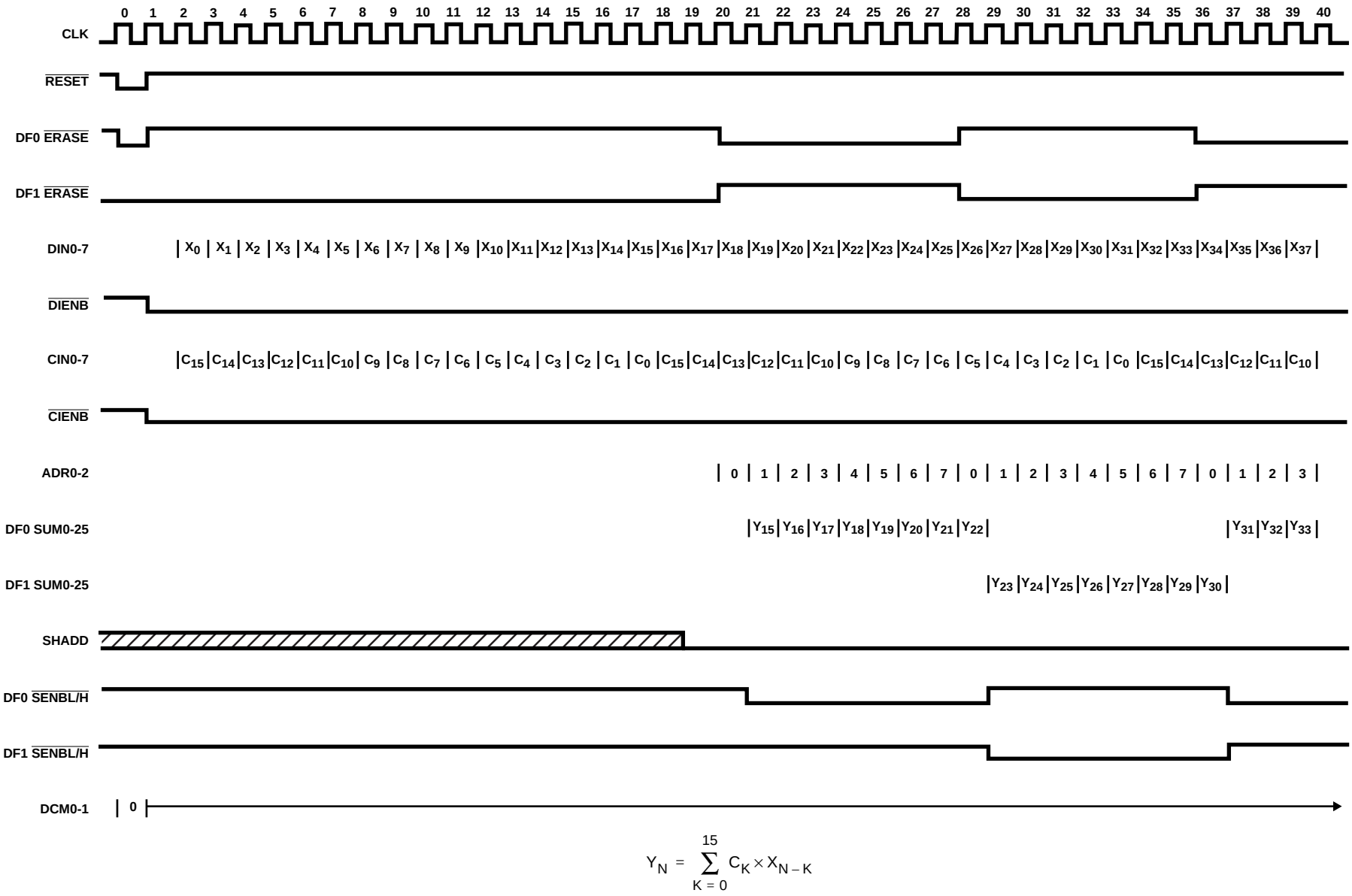
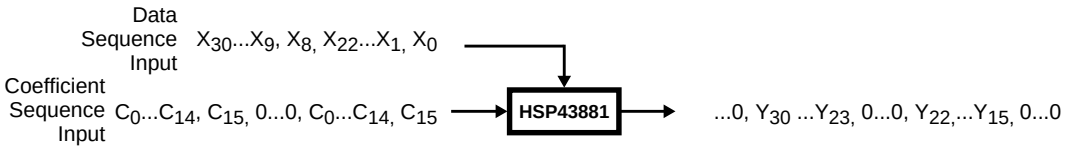


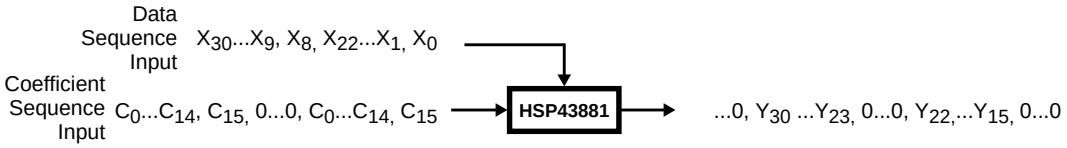
FIGURE 6. 16-TAP 30MHz FIR FILTER TIMING USING TWO CASCADED HSP43881s

TABLE 2. 16-TAP FIR FILTER SEQUENCE USING A SINGLE DF



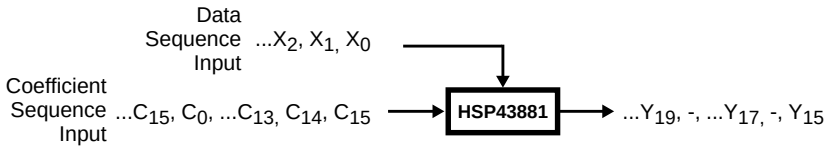
CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
6	$C_{15} \times X_0$	0	0	0					-
7	$+C_{14} \times X_1$	$C_{15} \times X_1$	0	0					-
8	$+C_{13} \times X_2$		$C_{15} \times X_2$	0					-
9	$+C_{12} \times X_3$			$C_{15} \times X_3$					-
10	$+C_{11} \times X_4$			$+C_{14} \times X_4$	$C_{15} \times X_4$				-
11	$+C_{10} \times X_5$			$+C_{13} \times X_5$		$C_{15} \times X_5$			-
12	$+C_9 \times X_6$			$+C_{12} \times X_6$			$C_{15} \times X_6$		-
13	$+C_8 \times X_7$			$+C_{11} \times X_7$				$C_{15} \times X_7$	-
14	$+C_7 \times X_8$			$+C_{10} \times X_8$				$C_{14} \times X_8$	-
15	$+C_6 \times X_9$			$+C9 \times X_9$				$C_{13} \times X_9$	-
16	$+C_5 \times X_{10}$			$+C_8 \times X_{10}$				$C_{12} \times X_{10}$	-
17	$+C_4 \times X_{11}$			$+C_7 \times X_{11}$				$C_{11} \times X_{11}$	-
18	$+C_3 \times X_{12}$			$+C_6 \times X_{12}$				$C_{10} \times X_{12}$	-
19	$+C_2 \times X_{13}$			$+C_5 \times X_{13}$				$C_9 \times X_{13}$	-
20	$+C_1 \times X_{14}$			$+C_4 \times X_{14}$				$C_8 \times X_{14}$	-
21	$+C_0 \times X_{15}$			$+C_3 \times X_{15}$				$C_7 \times X_{15}$	CELL 0 (Y15)
22	0	$+C_0 \times X_{16}$		$+C_2 \times X_{16}$				$C_6 \times X_{16}$	CELL 1 (Y16)
23	0	0	$C_0 \times X_{17}$	$+C_1 \times X_{17}$				$C_5 \times X_{17}$	CELL 2 (Y17)
24	0	0	0	$+C_0 \times X_{18}$				$C_4 \times X_{18}$	CELL 3 (Y18)
25	0	0	0	0	$C_0 \times X_{19}$			$C_3 \times X_{19}$	CELL 4 (Y19)
26	0	0	0	0	0	$C_0 \times X_{20}$		$C_2 \times X_{20}$	CELL 5 (Y20)
27	0	0	0	0	0	0	$C_0 \times X_{21}$	$C_1 \times X_{21}$	CELL 6 (Y21)
28	0	0	0	0	0	0	0	$C_0 \times X_{22}$	CELL 7 (Y22)

TABLE 2. 16-TAP FIR FILTER SEQUENCE USING A SINGLE DF (Continued)



CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
29	$C_{15} \times X_8$	0	0	0	0	0	0	0	-
30	$+C_{14} \times X_9$	$C_{15} \times X_9$	0	0	0	0	0	0	-
31	$+C_{13} \times X_{10}$		$+C_{15} \times X_{10}$	0	0	0	0	0	-
32	$+C_{12} \times X_{11}$				0	0	0	0	-
33	$+C_{11} \times X_{12}$				$C_{15} \times X_{12}$	0	0	0	-
34	$+C_{10} \times X_{13}$					$C_{15} \times X_{13}$	0	0	-
35	$+C_9 \times X_{14}$						$C_{15} \times X_{14}$	0	-
36	$+C_8 \times X_{15}$							$C_{15} \times X_{15}$	-
37	$+C_7 \times X_{16}$							$C_{14} \times X_{16}$	-
38	$+C_6 \times X_{17}$							$C_{13} \times X_{17}$	-
39	$+C_5 \times X_{18}$							$C_{12} \times X_{18}$	-
40	$+C_4 \times X_{19}$							$C_{11} \times X_{19}$	-
41	$+C_3 \times X_{20}$							$C_{10} \times X_{20}$	-
42	$+C_2 \times X_{21}$							$C_9 \times X_{21}$	-
43	$+C_1 \times X_{22}$							$C_8 \times X_{22}$	-
44	$+C_0 \times X_{23}$							$C_7 \times X_{23}$	CELL 0 (Y23)
45	0	$C_0 \times X_{24}$						$C_6 \times X_{24}$	CELL 1 (Y24)
46	0	0	$C_0 \times X_{25}$	$C_0 \times X_{26}$				$C_5 \times X_{25}$	CELL 2 (Y25)
47	0	0	0					$C_4 \times X_{26}$	CELL 3 (Y26)
48	0	0	0		$C_0 \times X_{27}$			$C_3 \times X_{27}$	CELL 4 (Y27)

TABLE 3. 16-TAP DECIMATE BY TWO FIR FILTER SEQUENCE; 30MHz IN, 15MHz OUT



CLK	CELL 0	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	SUM/CLR
6	$C_{15} \times X_0$	0	0	0	0	0	0	0	-
7	$+C_{14} \times X_1$	0	0	0	0	0	0	0	-
8	$+C_{13} \times X_2$	$C_{15} \times X_2$	0	0	0	0	0	0	-
9	$+C_{12} \times X_3$		0	0	0	0	0	0	-
10	$+C_{11} \times X_4$		$C_{15} \times X_4$	0	0	0	0	0	-
11	$+C_{10} \times X_5$			0	0	0	0	0	-
12	$+C_9 \times X_6$			$C_{15} \times X_6$	0	0	0	0	-
13	$+C_8 \times X_7$				0	0	0	0	-
14	$+C_7 \times X_8$				$C_{15} \times X_8$	0	0	0	-
15	$+C_6 \times X_9$					0	0	0	-
16	$+C_5 \times X_{10}$					$C_{15} \times X_{10}$	0	0	-
17	$+C_4 \times X_{11}$						0	0	-
18	$+C_3 \times X_{12}$						$C_{15} \times X_{12}$	0	-
19	$+C_2 \times X_{13}$							0	-
20	$+C_1 \times X_{14}$							$C_{15} \times X_{14}$	-
21	$+C_0 \times X_{15}$							$+C_{14} \times X_{15}$	CELL 0 (Y15)
22	$C_{15} \times X_{16}$							$+C_{13} \times X_{16}$	-
23	$+C_{14} \times X_{17}$							$+C_{12} \times X_{17}$	CELL 1 (Y17)
24	$+C_{13} \times X_{18}$							$+C_{11} \times X_{18}$	-
25	$+C_{12} \times X_{19}$							$+C_{10} \times X_{19}$	CELL 2 (Y19)
26	$+C_{11} \times X_{20}$							$+C_9 \times X_{20}$	-
27	$+C_{10} \times X_{21}$							$+C_8 \times X_{21}$	CELL 3 (Y21)
28	$+C_9 \times X_{22}$							$+C_7 \times X_{22}$	-
29	$+C_8 \times X_{23}$							$+C_6 \times X_{23}$	CELL 4 (Y23)
30	$+C_7 \times X_{24}$							$+C_5 \times X_{24}$	-
31	$+C_6 \times X_{25}$							$+C_4 \times X_{25}$	CELL 5 (Y25)
32	$+C_5 \times X_{26}$							$+C_3 \times X_{26}$	-
33	$+C_4 \times X_{27}$							$+C_2 \times X_{27}$	CELL 6 (Y27)
34	$+C_3 \times X_{28}$							$+C_1 \times X_{28}$	-
35	$+C_2 \times X_{29}$							$+C_0 \times X_{29}$	CELL 7 (Y29)
36	$+C_1 \times X_{30}$							$C_{15} \times X_{30}$	-
37	$+C_0 \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	$+C_{14} \times X_{31}$	CELL 8 (Y31)

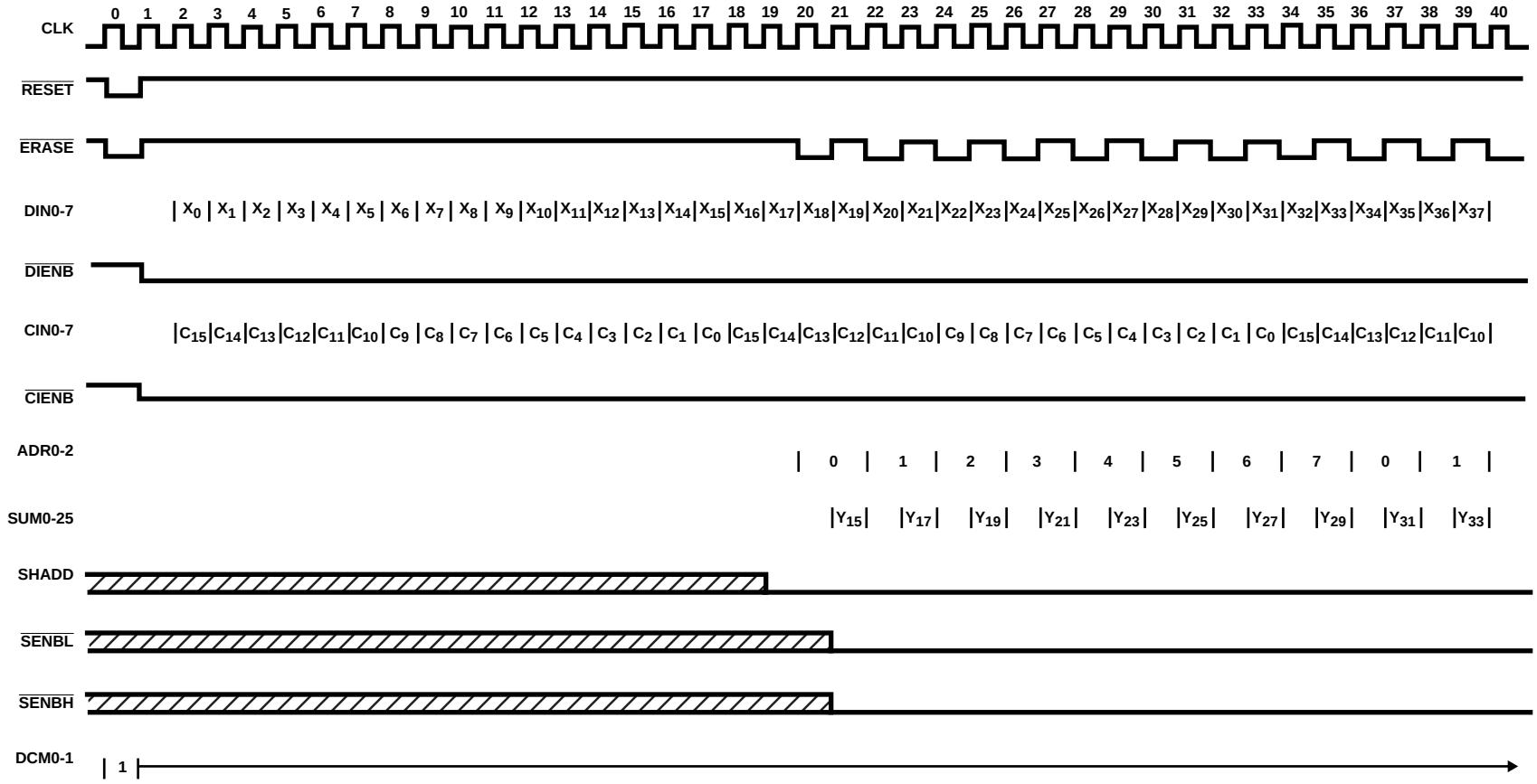


FIGURE 7. 16-TAP DECIMATE-BY-TWO FIR FILTER TIMING; 30MHz, 15MHz OUT

Absolute Maximum Ratings

Supply Voltage 8.0V
Input, Output Voltage . . . . . GND -0.5 to V_{CC} 0.5V
ESD Rating . . . . . Class 1

Operating Conditions

Voltage Range . . . . . 5V ±5%
Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PLCC Package	34	N/A
PGA Package	36	7

Maximum Junction Temperature
PLCC Package . . . . . 150^oC
PGA Package . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 17,763 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	NOTES	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	Notes 2, 4	V_{CC} = Max CLK Frequency 20MHz	-	140	mA
Standby Power Supply Current	I_{CCSB}	Note 4	V_{CC} = Max	-	500	µA
Input Leakage Current	I_I		V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Output Leakage Current	I_O		V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Logical One Input Voltage	V_{IH}		V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}		V_{CC} = Min	-	0.8	V
Logical One Output Voltage	V_{OH}		I_{OH} = 400µA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}		I_{OL} = 2mA, V_{CC} = Min	-	0.4	V
Clock Input High	V_{IHC}		V_{CC} = Max	3.0	-	V
Clock Input Low	V_{ILC}		V_{CC} = Min	-	0.8	V
Input Capacitance PLCC PGA	C_{IN}	Note 3	CLK Frequency 1MHz All measurements referenced to GND $T_A = 25^oC$	-	10 15	pF pF
Output Capacitance PLCC PGA	C_{OUT}			-	10 15	pF pF

NOTES:

2. Operating supply current is proportional to frequency. Typical rating is 7mA/MHz.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
4. Output load per test load circuit and C_L = 40pF.

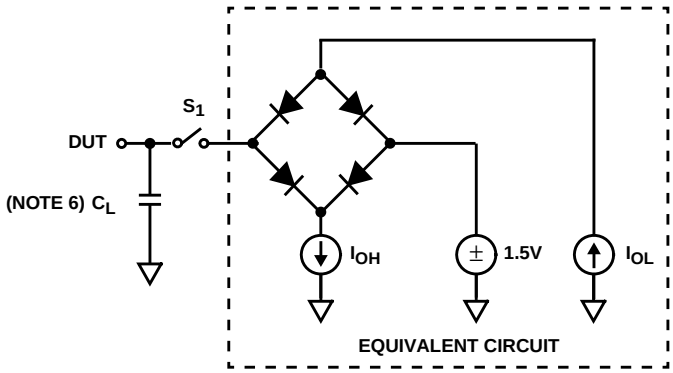
AC Electrical Specifications V_{CC} = 5V ±5%, T_A = 0°C to + 70°C

PARAMETER TEST CONDITIONS	SYMBOL	NOTES	-20 (20MHz)		-25 (25.6MHz)		-30 (30MHz)		
			MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Clock Period	t_{CP}		50	-	39	-	33	-	ns
Clock Low	t_{CL}		20	-	16	-	13	-	ns
Clock High	t_{CH}		20	-	16	-	13	-	ns
Input Setup	t_{IS}		16	-	14	-	13	-	ns
Input Hold	t_{IH}		0	-	0	-	0	-	ns
CLK to Coefficient Output Delay	t_{ODC}		-	24	-	20	-	18	ns
Output Enable Delay	t_{OED}		-	20	-	15	-	15	ns
Output Disable Delay	t_{ODD}	Note 5	-	20	-	15	-	15	ns
CLK to SUM Output Delay	t_{ODS}		-	27	-	25	-	21	ns
Output Rise	t_{OR}	Note 5	-	6	-	6	-	6	ns
Output Fall	t_{OF}	Note 5	-	6	-	6	-	6	ns

NOTE:

5. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

Test Load Circuit



NOTES:

6. Includes stray and jig capacitance.
7. Switch S_1 Open for I_{CCSB} and I_{CCOP} Tests.

Waveforms

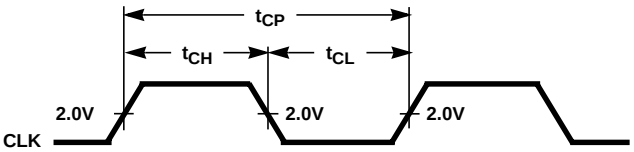
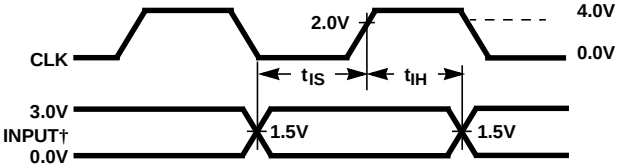
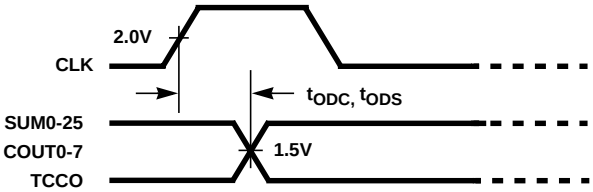


FIGURE 8. CLOCK AC PARAMETERS



† Input includes: DIN0-7, CIN0-7, DIENB, CIENB, ERASE, RESET,DCM0-1, ADRO-2, TCS, TCCI, SHADD

FIGURE 9. INPUT SETUP AND HOLD



† SUM-25, COUTO-7, TCCO are assumed not to be in high-impedance state.

FIGURE 10. SUM0-25, COUT0-7, TCCO OUTPUT DELAYS

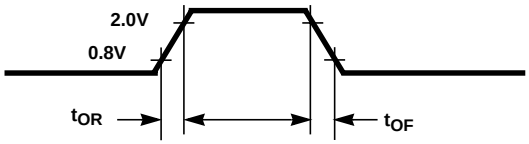


FIGURE 11. OUTPUT RISE AND FALL TIMES

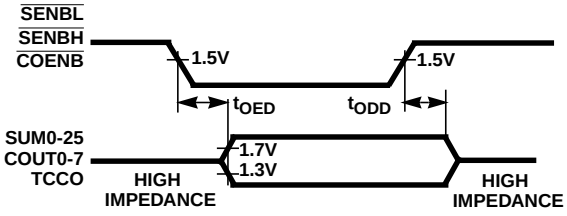
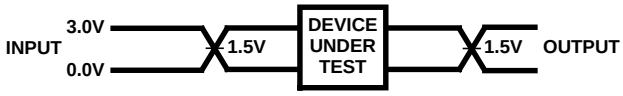


FIGURE 12. OUTPUT ENABLE, DISABLE TIMING



NOTE: AC Testing: Inputs are driven at 3.0V for Logic and “1” and 0.0V for Logic “0”. Input and output timing measurements are made at 1.5 for both a Logic “1” and “0”. CLK is driven at 4.0 and 0V and measured at 2.0V.

FIGURE 13. AC TESTING INPUT, OUTPUT WAVEFORM

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