Digital Controlled Variable Gain Amplifier DVGA2-33APP+

50Ω 0.05 to 3 GHz
31.5 dB, 0.5 dB Step, 6 Bit Parallel Control

The Big Deal

- Integrated Amplifier and Digital Attenuator
- 19 dB Gain / 31.5 dB Gain Control
- Flat frequency response, ±0.7 dB (700-2100 MHz)

CASE STYLE: DG1677

Product Overview

The DVGA2-33APP+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit Parallel interface attenuator and 19dB gain using a InGap HBT amplifier. Step attenuator used in DVGA2-33APP+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Key Features

Feature	Advantages
31.5 dB attenuation in 0.5 dB step size	Combining medium gain and a wide range of gain control makes the DVGA2-33APP+ an ideal building block for any RF chain where level setting control is required in a fast speed of parallel control interface.
Flat frequency response, ±0.7 over 700-2100 MHz	No need for external components to flatten gain.
Medium Gain, 19 dB	Incorporating multiple stages of amplification, the DVGA2-33APP+ provides medium gain over a wideband reducing cost and PCB board space.
Good IP3, +30.7 dBm at 1.0 GHz	Use in receivers and transmitters giving the users advantage in instantenous spur free dynamic range over wide bandwidths.
Output Power, +16.8 dBm at 1.0 GHz	The DVGA2-33APP+ maintains consistent output power capability over the full attenuation range and operating temperature range making it ideal to be used in remote applications such as LNB's as the L Band driver stage.
Attenuation Step size, 0.5 dB, accuracy 0.1 to 0.5 dB typ. Total attenuation, 31.5 dB	Enables precise control of gain in 0.5 dB steps up to 31.5 dB.
MCLP Package	Low Inductance, repeatable transitions, excellent thermal pad.
PCB area reduction	The DVGA2-33APP+ combines multiple functions common to TX/RX architectures into a single 5x5mm package
Flexibility in the application block diagram	The DVGA2-33APP+ provides access to the internal circuit through external jumper (see simplified schematic) enables designers flexibility to incorporate a wide range of additional circuits.

Digital Controlled Variable Gain Amplifier 50Ω 50 - 3000 MHz

19 dB Gain, 0.5 dB Step, 31.5 dB Attenuation,
6 Bit Parallel Control

Product Features

- 31.5 dB Gain control 0.5dB step size
- Gain, 19 dB nominal at 0dB attenuation and 1 GHz
- Useable to 4 GHz
- Parallel control interface
- Small size 5.0 x 5.0 mm

DVGA2-33APP+

CASE STYLE: DG1677

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Typical Applications

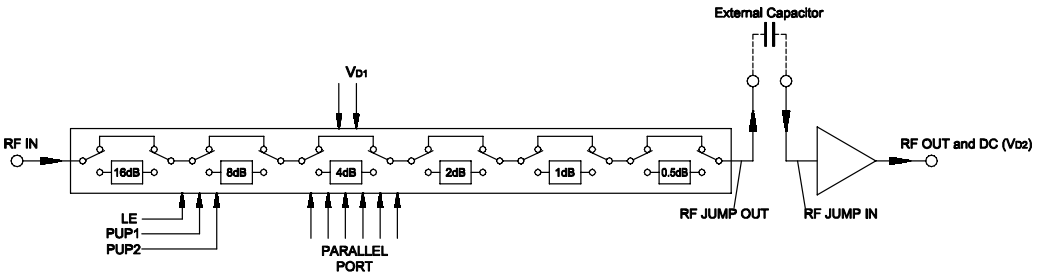
- Base Station Infrastructure
- GPS
- LTE
- WCDMA

General Description

The DVGA2-33APP+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit Parallel interface attenuator and 19dB gain using a InGap HBT amplifier. Step attenuator used in DVGA2-33APP+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic

(Refer to Table 1 for Pad description)



RF Electrical Specifications[1] at 25°C, 50Ω With V_{D1}=+3.0V, V_{D2}=+5V

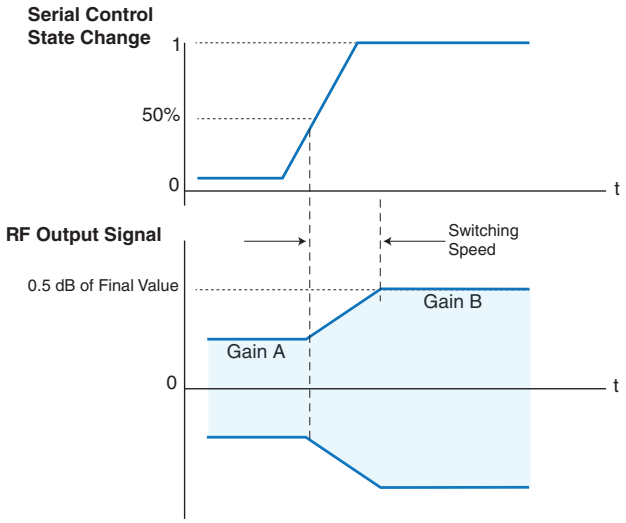
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.05		3.0	GHz
Gain (at 0 dB attenuation)	0.05	—	20.6	—	dB
	1.0	—	19.4	—	
	2.0	16.3	17.9	20.0	
	3.0	—	15.7	—	
Input Return Loss (all states)	0.05	—	13.2	—	dB
	1.0	—	13.6	—	
	2.0	—	10.8	—	
	3.0	—	10.8	—	
Output Return Loss (all states)	0.05	—	17.1	—	dB
	1.0	—	15.8	—	
	2.0	—	11.2	—	
	3.0	—	8.0	—	
Output Power @ 1 dB compression (all states)	0.05	—	16.5	—	dBm
	1.0	—	16.8	—	
	2.0	—	18.1	—	
	3.0	—	16.2	—	
Output IP3 (all states)	0.05	—	31.9	—	dBm
	1.0	—	30.7	—	
	2.0	—	31.5	—	
	3.0	—	29.1	—	
Noise Figure (at 0 dB attenuation)	0.05	—	4.7	—	dB
	1.0	—	4.9	—	
	2.0	—	5.3	—	
	3.0	—	5.2	—	
Accuracy @ **0.5 dB** Attenuation Setting	0.05 - 1.0	—	0.02	0.12	dB
	1.0 - 3.0	—	0.13	0.23	
Accuracy @ **1 dB** Attenuation Setting	0.05 - 1.0	—	0.02	0.13	dB
	1.0 - 3.0	—	0.22	0.3	
Accuracy @ **2 dB** Attenuation Setting	0.05 - 1.0	—	0.02	0.16	dB
	1.0 - 3.0	—	0.41	0.6	
Accuracy @ **4 dB** Attenuation Setting	0.05 - 1.0	—	0.03	0.3	dB
	1.0 - 3.0	—	0.58	0.7	
Accuracy @ **8 dB** Attenuation Setting	0.05 - 1.0	—	0.05	0.4	dB
	1.0 - 3.0	—	0.97	1.1	
Accuracy @ **16 dB** Attenuation Setting	0.05 - 1.0	—	0.13	0.6	dB
	1.0 - 3.0	—	1.21	1.4	
Thermal Resistance (Amplifier)[2]		—	91	—	°C/W

1. Measured in Mini-Circuits characterization test board TB-694A+. See characterization Test Circuit (Fig. 2)
2. Junction to ground paddle

Attenuation Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	µSec
Switching Rep Rate	—	—	25	KHz

Figure 1. Switching Speed



DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{D1}	2.7	3.0	3.3	V
V_{D2}	4.75	5.0	5.25	V
Supply Current, I_{D1}	—	—	200	µA
I_{D2}	—	69	78	mA
Control Input Low	-0.3	—	0.6	V
Control Input High	1.17	—	3.6	V
Control Current*	—	—	1	µA

*Except 30 µA typ. for C0.5, C16 and 2 µA typ. for LE.

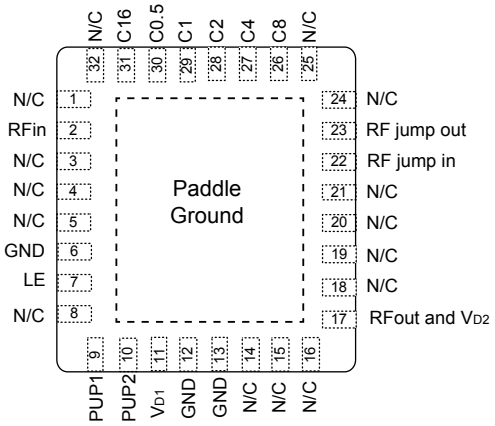
Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature (ground pad)	-40°C to 85°C
Storage Temperature	-65°C to 150°C
V_{D1}	-0.3V Min., 5.5V Max.
V_{D2}	5.7V
Voltage on any control input	-0.3V Min., V_{D1}+0.3V Max.
Input Power	+13dBm

Permanent damage may occur if any of these limits are exceeded.

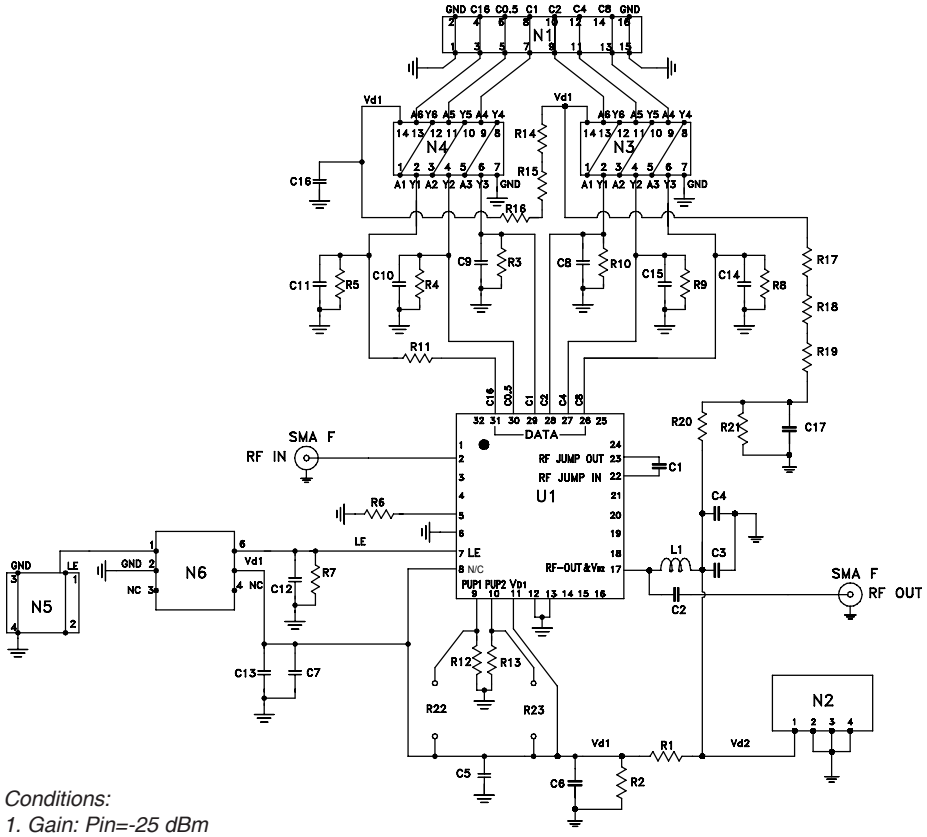
Table 1. Pad Description

Pin Number	Function	Description
1	N/C	Not Connected
2	RF IN	RF Input Port (Note 1)
3	N/C	Not Connected
4	N/C	Not Connected
5	N/C	Not Connected (Note 4)
6	GND	Ground
7	LE	Latch Enable Input (Note 2)
8	N/C	No Connection
9	PUP1	Power-Up Selection
10	PUP2	Power-Up Selection
11	V_{D1}	V_{D1} Power Supply Input
12	GND	Ground
13	GND	Ground
14	N/C	Not Connected
15	N/C	Not Connected
16	N/C	Not Connected
17	RF OUT &V_{D2}	RF output and V_{D2} on same pad (external Bias Tee) (Note1,6)
18	N/C	Not Connected
19	N/C	Not Connected
20	N/C	Not Connected
21	N/C	Not Connected
22	RF JUMP IN	Interstage RF Jumper Input (Note 1)
23	RF JUMP OUT	Interstage RF Jumper Output (Note 1)
24	N/C	Not Connected
25	N/C	Not Connected
26	C8	Power Up Control for 8dB Att. Bit (Note 4)
27	C4	Power Up Control for 4dB Att. Bit (Note 4)
28	C2	Power Up Control for 2dB Att. Bit (Note 4)
29	C1	Power Up Control for 1dB Att. Bit (Note 4)
30	C0.5	Power Up Control for 0.5dB Att. Bit (Note 4)
31	C16	Power Up Control for 16dB Att. Bit (Note 3,4)
32	N/C	Not Connected
PADDLE	GND	Ground (Note5)



Notes:
1. All RF input and output ports shall be AC coupled with external blocking capacitor.
2. Latch Enable (LE) has an internal 2MΩ pull-up resistor to V_{D1}
3. Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance (see layout drawing PL-383).
4. Place a 10KΩ resistor to ground.
5. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation
6. See application and characterization test circuit and layout drawing PL-383.

Application and Characterization Test Circuit



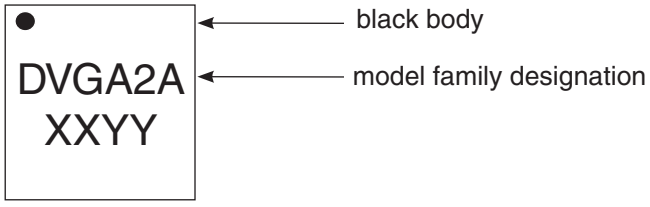
Conditions:
1. Gain: Pin=-25 dBm
2. Output IP3 (OIP3): two tones, spaced 1 MHz apart +5 dBm/ tone at output.
3. Schmitt trigger used in characterization circuit. Not required when application circuit includes recommended level settings.

Figure 2. Schematic of Test Circuit used for Characterization. (DUT soldered on Mini-Circuits Characterization Test Board TB-694A+). Gain, output power at 1 dB compression (P1dB) Output IP3 (OIP3), Noise Figure are measured using Agilent's N5242A PNA-X Microwave Network Analyzer.

Bill of Materials

Ref. Des.	Value / Description	Case Style, Size
U1	DVGA2-33APP+	
N1	CONN VERT HDR 2-ROW 16 POS	
N2	CONN VERT HDR 4POS 1.25MM	
N3,N4	HEX INVERT TRIGGER Fairchild P/N MM74HC14M	
N5	CONN VERT HDR 2-ROW 4 POS	
N6	SCHMITT TRIGGER BUFFER TI P/N SN74LVC2G17DCKR	
C1	1000 pF	0402
C2	1000 pF	0805
C3	1 uF	0805
C4	100 pF	0402
C5	100 pF	0603
C6,C17	0.47 uF	0805
C7	0.1 uF	0805
C8-C16	100 pF	0603
R1,R20	475 OHM	0603
R2,R21	681 OHM	0603
R3-R10	10 KOHM	0603
R11	10 KOHM	0402
R12,R13	475 OHM	0603
R14-R19	0 OHM	0603
R22-R23	OPTIONAL PULL UP RESISTORS FOR PUP1 AND PUP2	0603
L1	390 NH	0603

Product Marking



Simplified Schematic

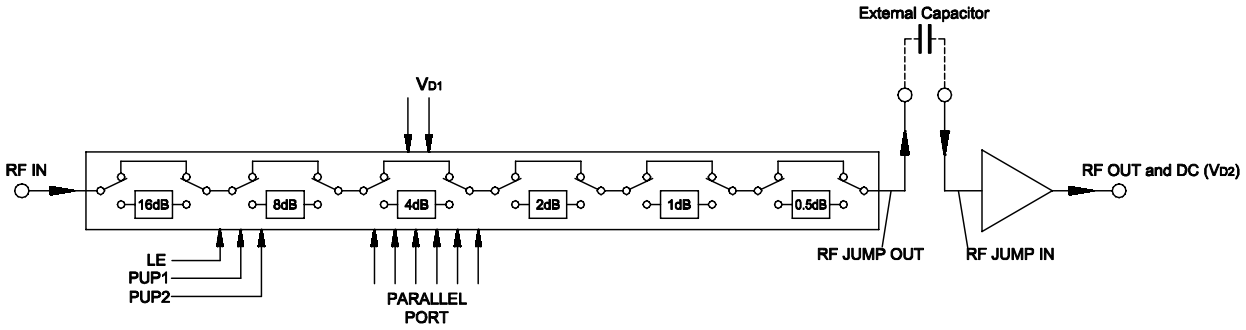


Figure 3. The DVGA2-33APP+ Parallel interface consists of 6 control bits that select the desired attenuation state, as shown in Table 2 Truth Table.

Table 2. Truth Table

Attenuation State	C16	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0	0
0.5 (dB)	0	0	0	0	0	1
1 (dB)	0	0	0	0	1	0
2 (dB)	0	0	0	1	0	0
4 (dB)	0	0	1	0	0	0
8 (dB)	0	1	0	0	0	0
16 (dB)	1	0	0	0	0	0
31.5 (dB)	1	1	1	1	1	1
Note: Not all 64 possible combinations of C0.5 - C16 are shown in table						

The parallel interface timing requirements are defined by Figure 4 (Parallel Interface Timing Diagram) and Table 3 (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

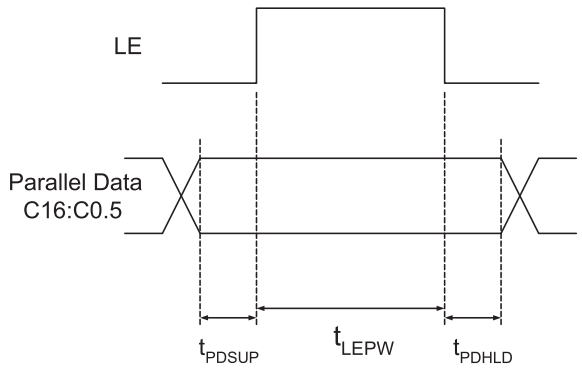


Figure 4. Parallel Interface Timing Diagram

Table 3. Parallel Interface AC Characteristics (V_{D1}=3V)

Symbol	Parameter	Min.	Max.	Units
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Parallel data set-up time before clock rising edge of LE	10		ns
t_{PDHLD}	Parallel data hold time after clock falling edge of LE	10		ns

Power-up Control Settings

The DVGA2-33APP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided. When the attenuator powers up with LE=0, the six parallel control bits are set to one of four possible values. These values are selected by the two power up control bits; PUP1 and PUP2, as shown in Table 4 (Power-Up Truth table, Parallel Mode)

Table 4 **Power-Up Truth Table, Parallel Mode**

Attenuation State	PUP1	PUP2	LE
Reference	0	0	0
8 (dB)	0	1	0
16 (dB)	1	0	0
31 (dB)	1	1	0
Defined by C0.5-C16 (See Table 1-Truth Table)	X (Note 1)	X (Note 1)	1

Note 1: PUP1 and PUP2 Connection may be 0, 1, GROUND, or not connect, without effect on attenuation state.

Power-Up LE=1 provides normal parallel operation with c0.5-c16, and PUP1 and PUP2 are not active.

Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG1677 *Plastic package, exposed paddle, lead finish: Ni/Pd/Au*
Tape & Reel **Standard quantities available on reel**	F68 *7" reels with 20,50,100,200, 500 or 1K devices*
Suggested Layout for PCB Design	PL-383
Evaluation Board	TB-694A+
Environmental Ratings	ENV66

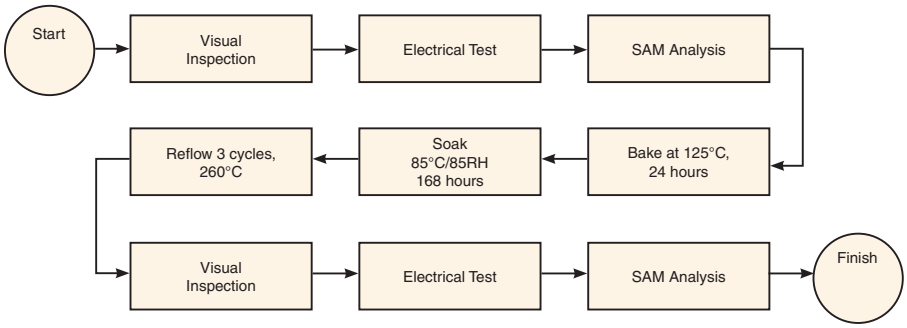
ESD Rating

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

Machine Model (MM): Class M1 (100V) in accordance with ANSI/ESD STM5.2-1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D



Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp