



STG8820

SamHop Microelectronics Corp.

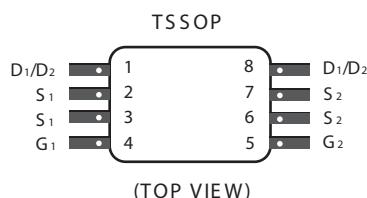
Ver 1.1

Dual N-Channel Enhancement Mode Field Effect Transistor

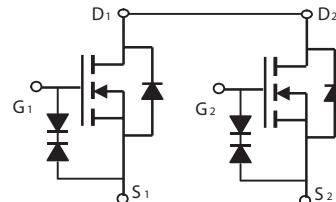
PRODUCT SUMMARY		
VDSS	ID	RDS(ON) (mΩ) Max
20V	7A	20 @ VGS=4.0V
		27 @ VGS=2.5V

FEATURES

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Limit	Units
V_{DS}	Drain-Source Voltage		20	V
V_{GS}	Gate-Source Voltage		± 12	V
I_D	Drain Current-Continuous ^a	$T_A=25^\circ\text{C}$	7	A
		$T_A=70^\circ\text{C}$	5.6	A
I_{DM}	-Pulsed ^b		28	A
P_D	Maximum Power Dissipation ^a	$T_A=25^\circ\text{C}$	1.5	W
		$T_A=70^\circ\text{C}$	1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ^a	85	$^\circ\text{C}/\text{W}$
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ELECTRICAL CHARACTERISTICS ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
I_{DSs}	Zero Gate Voltage Drain Current	$V_{DS}=16V, V_{GS}=0V$			1	μA
I_{GSs}	Gate-Body Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$			± 10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.8	1.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=4V, I_D=7A$		17	20	m ohm
		$V_{GS}=2.5V, I_D=6A$		20	27	m ohm
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=7A$		23		S
DYNAMIC CHARACTERISTICS ^c						
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V$ $f=1.0MHz$		470		pF
C_{oss}	Output Capacitance			164		pF
C_{rss}	Reverse Transfer Capacitance			142		pF
SWITCHING CHARACTERISTICS ^c						
$t_{D(ON)}$	Turn-On Delay Time	$V_{DD}=10V$ $I_D=1A$ $V_{GS}=4V$ $R_{GEN}=10\text{ ohm}$		17		ns
t_r	Rise Time			54		ns
$t_{D(OFF)}$	Turn-Off Delay Time			63		ns
t_f	Fall Time			45		ns
Q_g	Total Gate Charge	$V_{DS}=10V, I_D=7A,$ $V_{GS}=4V$		10		nC
Q_{gs}	Gate-Source Charge			2.1		nC
Q_{gd}	Gate-Drain Charge			4.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_s	Maximum Continuous Drain-Source Diode Forward Current			2.0	A	
V_{SD}	Diode Forward Voltage ^b	$V_{GS}=0V, I_s=2.0A$		0.79	1.2	V
Notes						
a.Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.						
b.Pulse Test:Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.						
c.Guaranteed by design, not subject to production testing.						

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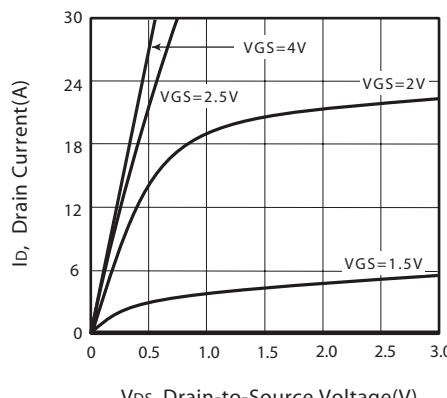


Figure 1. Output Characteristics

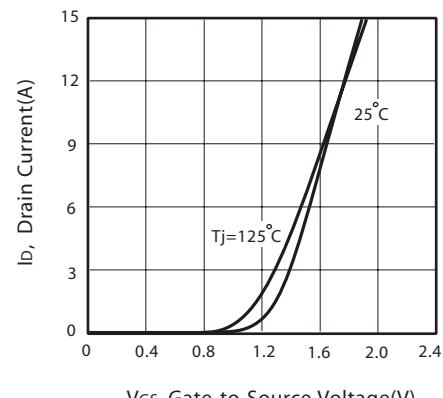


Figure 2. Transfer Characteristics

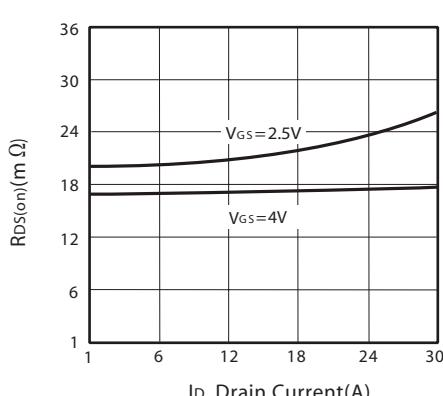


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

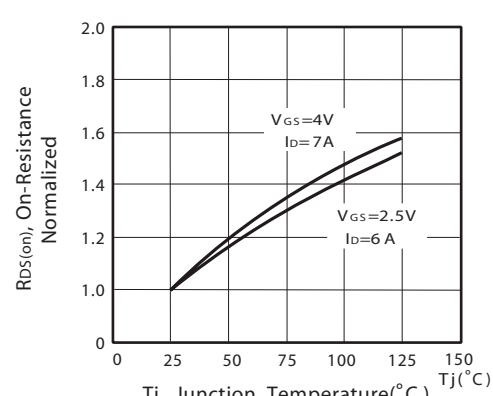


Figure 4. On-Resistance Variation with Drain Current and Temperature

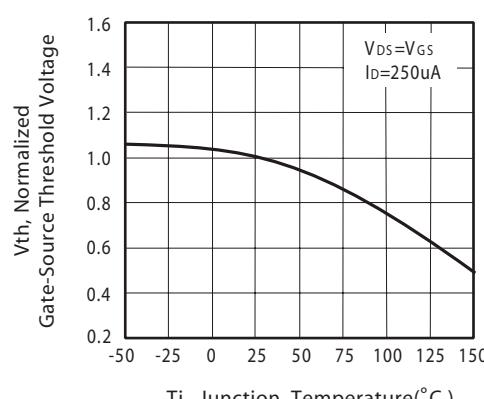


Figure 5. Gate Threshold Variation with Temperature

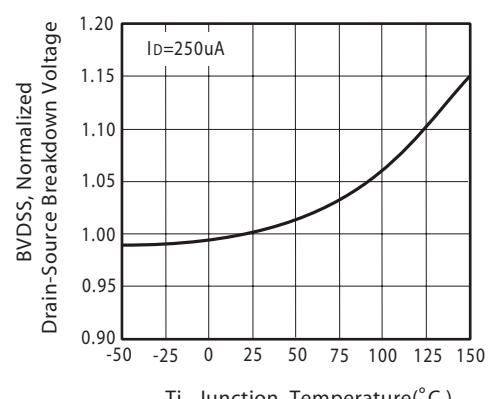
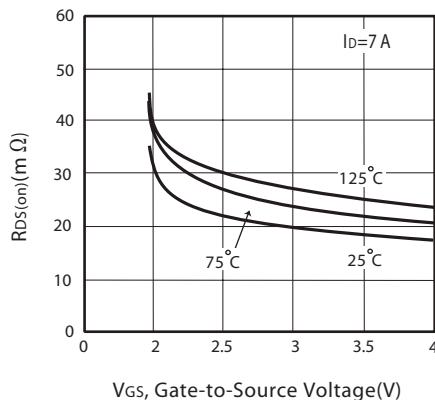


Figure 6. Breakdown Voltage Variation with Temperature

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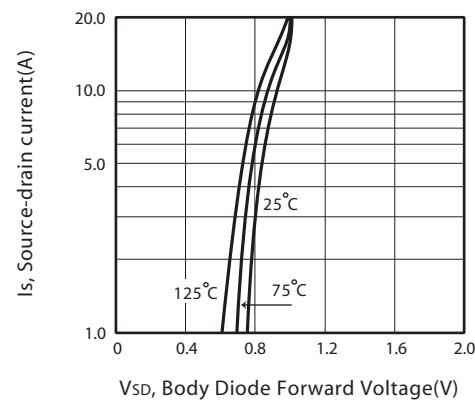
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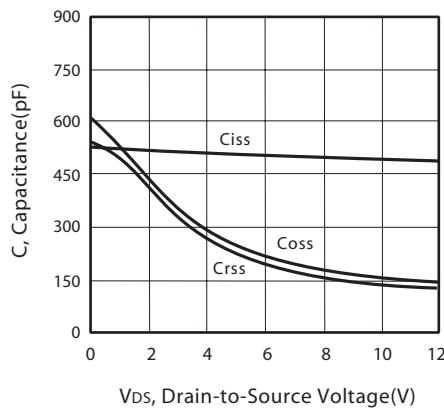
V_{GS}, Gate-to-Source Voltage(V)

Figure 7. On-Resistance vs. Gate-Source Voltage



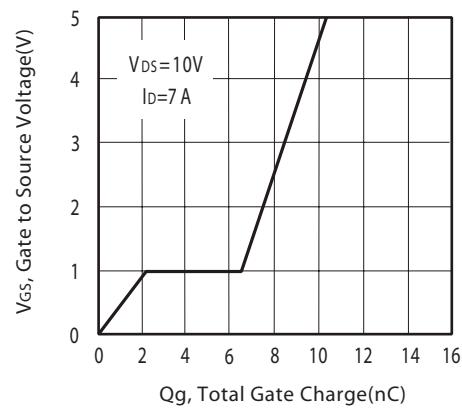
V_{SD}, Body Diode Forward Voltage(V)

Figure 8. Body Diode Forward Voltage Variation with Source Current



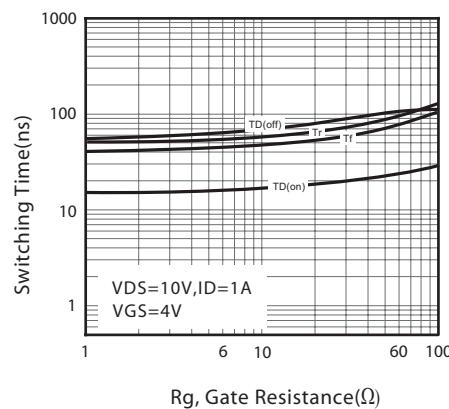
V_{DS}, Drain-to-Source Voltage(V)

Figure 9. Capacitance



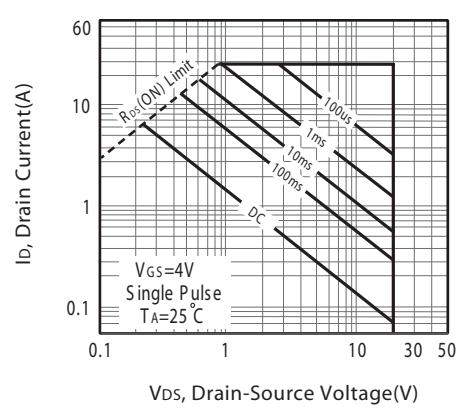
Q_g, Total Gate Charge(nC)

Figure 10. Gate Charge



R_g, Gate Resistance(Ω)

Figure 11. switching characteristics



V_{DS}, Drain-Source Voltage(V)

Figure 12. Maximum Safe Operating Area

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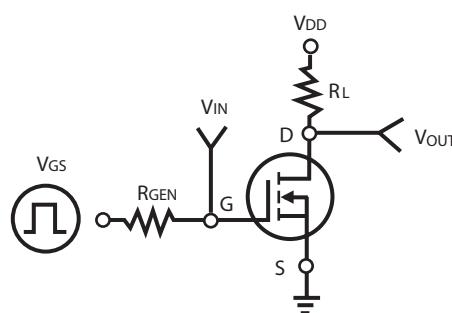


Figure 13. Switching Test Circuit

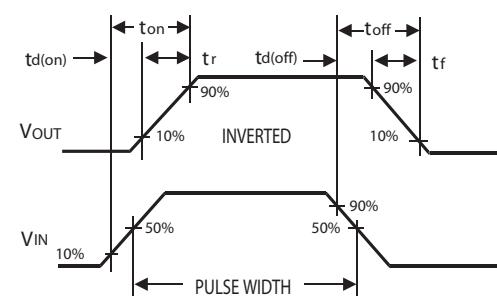
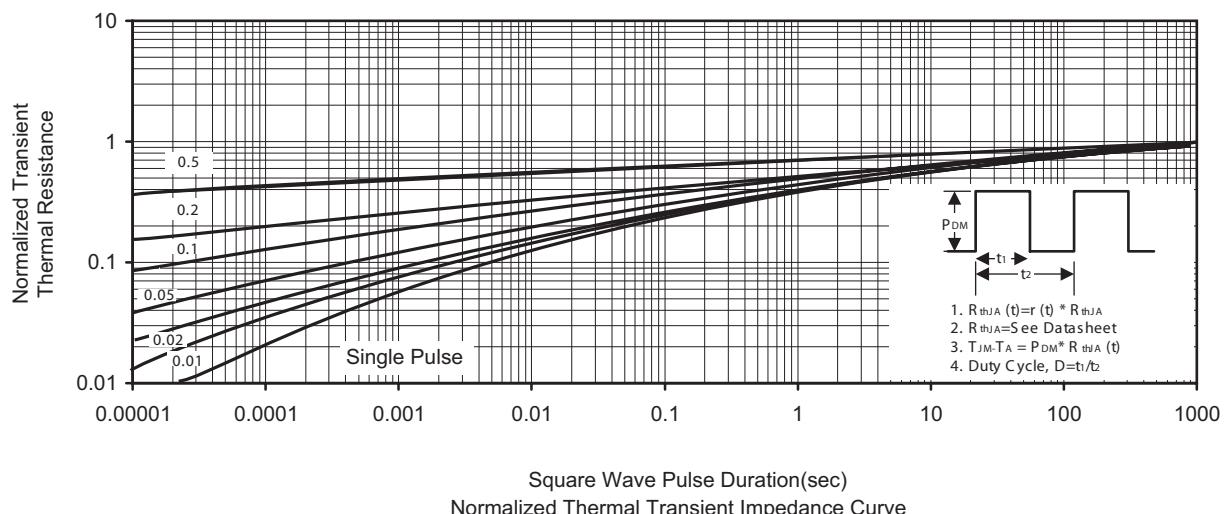


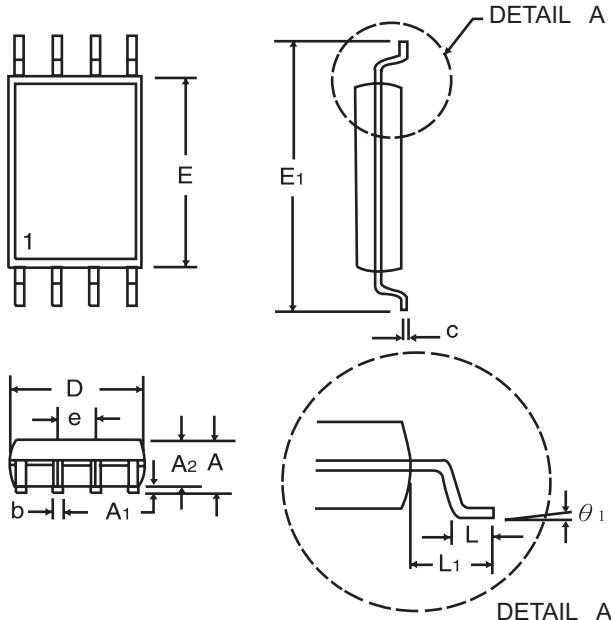
Figure 14. Switching Waveforms



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PACKAGE OUTLINE DIMENSIONS

TSSOP-8

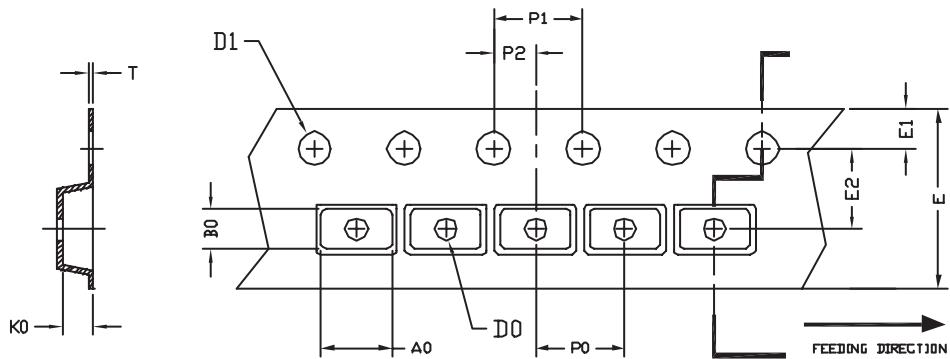


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.20	0.033	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.127		0.005	
D	2.90	3.10 ^②	0.114	0.122 ^②
E	4.30	4.50 ^③	0.169	0.177 ^③
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
θ ₁	0°	8°	0°	8°

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E to be determined at Datum Plane H.

TSSOP-8 Tape and Reel Data

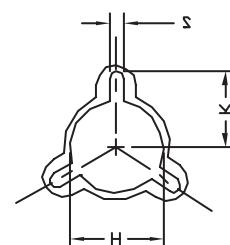
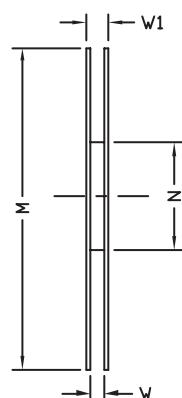
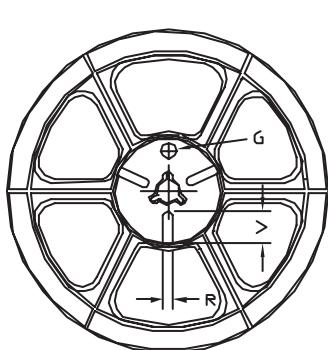
TSSOP-8 Carrier Tape



UNIT : mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSSOP 8	6.08	4.40	1.60	$\phi 1.50$ + 0.1 - 0.0	$\phi 1.50$ + 0.1 - 0.0	12.00 ± 0.3	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

TSSOP-8 Reel



UNIT : mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\phi 330$	330	100	12.5	16.0	$\phi 13.0$ + 0.5 - 0.2	10.6	2.0 ± 0.5	---	---	---