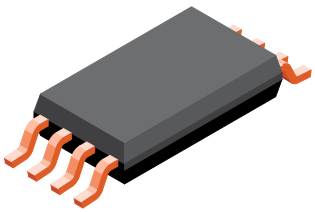
3V Hall Effect Linear Sensor with I²C Output

FEATURES AND BENEFITS

- 1 mm thin (TSSOP-08) package
- 2 factory programmed sensitivity options: 2 LSB/G (for fields up to ±1000 G) and 4 LSB/G (±500 G)
- Temperature-stable sensitivity for NdFeB and ferrite magnets
- I²C interface for easy integration with support for up to 127 unique addresses
- EEPROM stores factory programmed settings and up to 16 bytes of user information (programmable through the I²C interface)
- Micro-power sleep mode through I²C command for minimizing power in battery-operated applications
- Precise recoverability after temperature cycling
- Wide ambient temperature range: –40°C to 125°C
- 12-bit ADC with 10-bit ENOB (Effective Number of Bits)

Package: 8-Pin TSSOP (suffix LE)



Not to scale

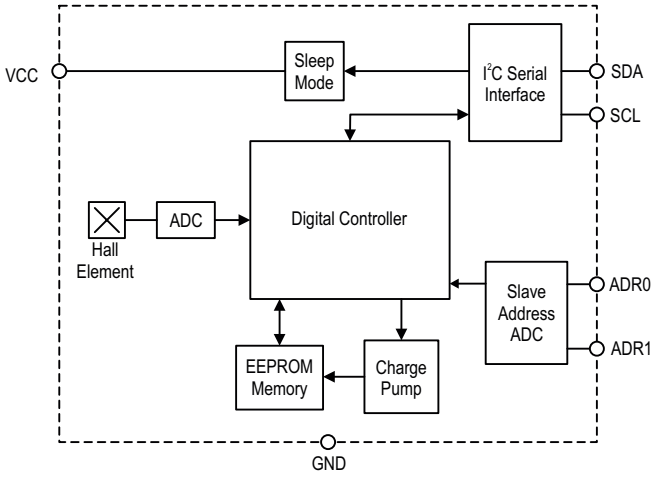
DESCRIPTION

The A1454 linear Hall effect sensor IC provides a 12-bit digital output word that is proportional to the strength of the magnetic field that is present. Its quiescent output value is at mid-scale, and it comes in 2 different factory programmed sensitivity ranges: 2LSB/G & 4LSB/G. The sensitivity temperature coefficient is also factory programmed to support either Neodymium or Ferrite magnets. The A1454 incorporates an I²C interface for easy integration into a wide variety of applications. The I²C address can either be set by external resistors or programmed via EEPROM, to support up to 127 unique I²C addresses, allowing for multiple ICs on the same bus. It also includes 16 bytes of user programmable EEPROM.

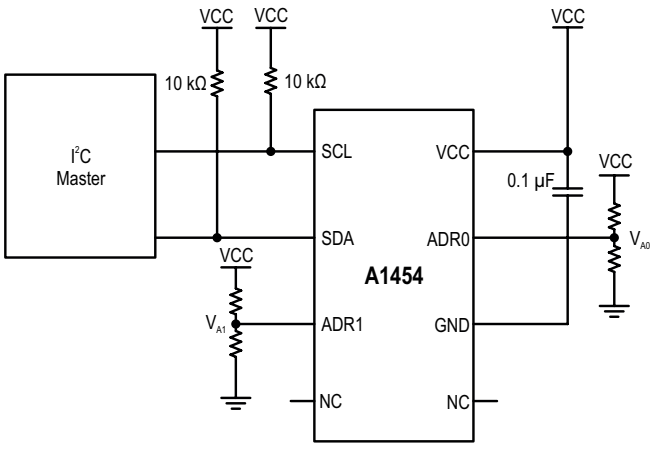
The A1454 I²C interface provides a user-controlled sleep input command that puts the device in micro-power mode, which reduces the current consumption of the A1454. This low power feature makes the A1454 perfect for portable, battery-operated applications.

The BiCMOS monolithic process allows the integration of both high precision analog and high-density digital circuitry. The A1454 integrates the Hall element, a 12-bit ADC, gain & offset compensation circuitry, EEPROM memory and the I²C interface on a single monolithic IC that is packaged in a space saving surface mount package.

Engineering samples are available on a limited basis. Contact your sales or applications support office for additional information.



Functional Block Diagram



Typical Application Circuit

SPECIFICATIONS

Selection Guide

Part Number	Sensitivity	Target Magnet	Packing	Package
A1454KLETR-2F-T	2 LSB/G	Ferrite	4000 pieces per reel	8-Pin TSSOP Package
A1454KLETR-4F-T	4 LSB/G	Ferrite		
A1454KLETR-2N-T	2 LSB/G	Neodymium		
A1454KLETR-4N-T	4 LSB/G	Neodymium		

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		5.0	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward SCL Pin Voltage	$V_{I2C(SCL)}$		5.5	V
Forward SDA Pin Voltage	$V_{I2C(SDA)}$		5.5	V
Reverse SCL and SDA Voltage	V_{RI2C}		–0.1	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature[1]	T_{stg}		–65 to 170	ºC

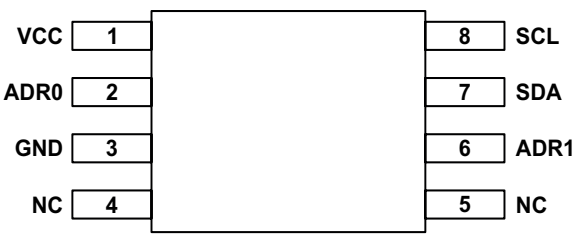
[1]Stresses Beyond the Absolute Maximum Ratings may result in permanent device damage. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On single-layer PCB with copper limited to solder pads	137	ºC/W

*Additional thermal information available on the Allegro website.

Pin-out Diagram and Terminal List Table



Package LE, 8-Pin TSSOP Pin-out Diagram

Terminal List Table

Number	Name	Function
1	VCC	Device Supply Voltage Pin
2	ADR0	Address Select Pin 0
3	GND	Device Ground Pin
4	NC	No Connection
5	NC	No Connection
6	ADR1	Address Select Pin1
7	SDA	I²C interface SDA Pin
8	SCL	I²C interface SCL Pin

OPERATING CHARACTERISTICS: valid at T_A = 25°C, V_{CC} = 3.0 V, and C_{BYPASS} = 0.1 µF; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Electrical Characteristics						
Supply Voltage	V_{CC}	Normal Operation	2.65	3.0	3.5	V
		EEPROM programming	2.8 [3]	–	3.5	V
Turn On Delay[1]	t_{don}	After $V_{CC(min)}$ is reached	–	30	–	ms
Supply Current	I_{CC}	V_{CC} = $V_{CC(max)}$, Active mode	–	2	5	mA
		V_{CC} = $V_{CC(max)}$, Sleep mode	–	0.2	1	µA
		V_{CC} = $V_{CC(max)}$, EEPROM programming occurring	–	2	5	mA
Internal Bandwidth[2]	BW_i	Small signal –3 dB	–	2	–	kHz
Output Refresh Rate[3]	f_{out}		–	32	–	kHz
POR V_{CC} Low Time[4]	t_{POR}	V_{CC} goes below $V_{CC(min)}$	–	100	–	ms
Number of EEPROM Writes	–	Number of times the EEPROM can be written	–	–	1000	writes
Address Pin Characteristics						
Address Value 0 Reference [5]	V_{ADDR0}	ADR0, ADR1 Pins	–	0	0.1	x VCC
Address Value 1 Reference [5]	V_{ADDR1}	ADR0, ADR1 Pins	0.23	0.33	0.43	x VCC
Address Value 2 Reference [5]	V_{ADDR2}	ADR0, ADR1 Pins	0.57	0.67	0.77	x VCC
Address Value 3 Reference [5]	V_{ADDR3}	ADR0, ADR1 Pins	0.90	0.100	–	x VCC
Address Pin Input Resistance	R_{in}	ADR0, ADR1 Pins	0.8	1	1.2	MΩ

[1] The device will not respond to I²C inputs until after the turn-on delay.
[2] Determined by design and characterization, not evaluated at final test.
[3] The rate at which a new output value is available to be read by the I²C interface.
[4] If V_{CC} is below $V_{CC(min)}$ for this amount of time, the device will reset when V_{CC} goes above $V_{CC(min)}$. If the device is in Sleep mode when V_{CC} goes below $V_{CC(min)}$, this time will be much longer due to the slow discharge of internal capacitors while in Sleep mode.
[5] Based on design simulation and device characterization. Not verified for each part at final test.

MAGNETIC CALIBRATION CHARACTERISTICS: valid at T_A = 25°C and C_{BYPASS} = 0.1 µF; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
Factory Programmed Quiescent Voltage Output	QVO	A1454KLETR-4N,T_A = 25°C	–	±10	–	LSB
		A1454KLETR-4F,T_A = 25°C	–	±10	–	LSB
		A1454KLETR-2N,T_A = 25°C	–	±10	–	LSB
		A1454KLETR-2F,T_A = 25°C	–	±10	–	LSB
Factory Programmed Sensitivity	Sens	A1454KLETR-4N,T_A = 25°C FSI = +/- 500 G	–	4.0	–	LSB/G
		A1454KLETR-4F,T_A = 25°C FSI = +/- 500 G	–	4.0	–	LSB/G
		A1454KLETR-2N,T_A = 25°C FSI = +/- 1000 G	–	2.0	–	LSB/G
		A1454KLETR-2F,T_A = 25°C FSI = +/- 1000 G	–	2.0	–	LSB/G
Sensitivity Temperature Coefficient	TC_{sens}	NdFeB compensated[2] applies to part numbers with suffix 'N'	–	0.12	–	%/ºC
		Ferrite compensated[3] applies to part numbers with suffix 'F'	–	0.21	–	%/ºC
Linearity sensitivity error[4]	Lin_{ERR}		–	<±1	–	%
Effective Number of Bits		Field = 1000 G, Temp = 25ºC, BW = 2 kHz.	–	~10	–	Bits
Effective Number of Bits		Field = 500 G, Temp = 25–C, BW = 2 kHz.	–	~9	–	Bits
Sensitivity Error vs. Temp	$Sens_{Err}$	–40ºC ~ +85ºC	–	<±3	–	%
		–40ºC ~ +125ºC	–	<±6	–	%

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] The slope of the Hall gain function with temperature change is meant to compensate for the variation of a Neodymium magnet with temperature.
[3] The slope of the Hall gain function with temperature change is meant to compensate for the variation of a ferrite magnet with temperature.
[4] See Characteristic Definitions section.

I²C INTERFACE CHARACTERISTICS*: valid at T_A = 25°C, V_{CC} = 3.0 V, and REXT = 10 kΩ; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Bus Free Time Between Stop and Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	t_{ndSTA}		0.6	–	–	µs
Setup Time for Repeated Start Condition	t_{suSTA}		0.6	–	–	µs
SCL Low Time	t_{low}		1.3	–	–	µs
SCL High Time	t_{high}		0.6	–	–	µs
Data Setup Time	t_{suDAT}		100	–	–	ns
Data Hold Time	t_{hdDAT}		0	–	900	ns
Setup Time for Stop Condition	t_{suSTO}		0.6	–	–	µs
Logic Input Low Level (SDA, SCL pins)	V_{IL}		–	–	30	$\%V_{CC}$
Logic Input High Level (SDA, SCL pins)	V_{IH}		70	–	–	$\%V_{CC}$
Logic Input Current	I_{IN}	V_{IN} = 0 V to V_{CC}	–1	0	1	µA
Output Voltage (SDA pin)	V_{OL}	I_{LOAD} = 1.5 mA	–	–	0.36	V
Clock Frequency (SCL pin)	f_{CLK}		–	–	400	kHz
Output Fall Time (SDA pin)	t_f	R_{PU} = 2.4 kΩ, C_B = 100 pF	–	–	250	ns
I²C Pull-Up Resistance	R_{EXT}		2.4	10	–	kΩ
Total Capacitive Load for Each of SDA and SCL Buses	C_B		–	–	100	pF

*These values are ratiometric to the supply voltage. I²C Interface Characteristics are ensured by design and not factory tested.
*Contact Allegro for 1.8V I²C Bus support.

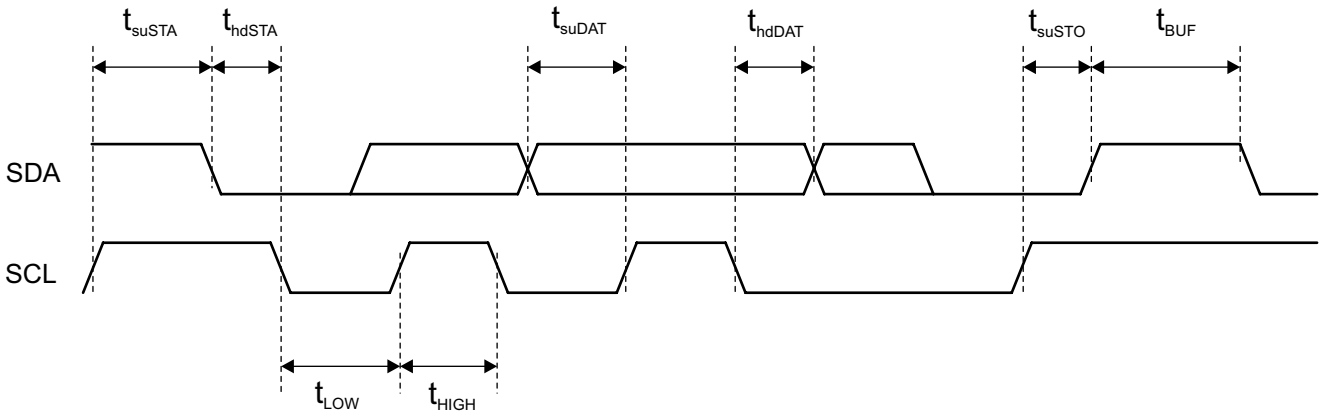


Figure 1: I²C Interface Timing Diagram

PRIMARY REGISTERS

Customer Accessible Registers

The following table shows registers that are customer accessible and can be read/written using the I²C protocol.

Table 1: Customer Accessible Registers

Address	Name	Bit Field																							
		25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0X1D	Temp Out [11:0]															Temperature Sensor Output											
0X1F	Output [11:0]															Sensor Output											
0X20	Sleep [)]																										Sleep

Sensor Output

The A1454 provides a 12 bit digital output that is proportional to the magnetic field applied normally to the hall element.

Table 2: Output [11:0], Address 0x1F, Bit Definition Table

Bits	Address	Name	Value	Description	R/W	Default
11:0	0x1F	Output	0/1 (for each bit)	12-bit signed signal proportional to field strength intensity. 0G is denoted by 12'b0 value.	R	–

Temperature Sensor Output

The A1454 provides a 12-bit digital output that is proportional to the junction temperature of the hall-sensor IC.

Table 3: Temp Out [11:0], Address 0x1D, Bit Definition Table

Bits	Address	Name	Value	Description	R/W	Default
11:0	0x1D	Temp Out	0/1 (for each bit)	12-bit signed signal proportional to temperature. 25C is denoted by a 12'b0 value. Temperature Slope is ~ 8 LSB/ºC.	R	–

Sleep Mode

The 1454 supports a sleep mode where numerous sub-systems are powered. To enter sleep mode, the user sets the sleep control bit. To awake from sleep mode the user clears the sleep bit. Since the I²C logic uses SCL as its clock source and the sleep bit implemented in the SCL clock domain, the system clock does not need to be operational for the sleep output to be cleared. Within a period of about 50 µs after clearing the sleep bit, the system clock will be operational, and the A1454 IC will respond to I²C commands. Furthermore, within a period of about 150 µs after clearing the sleep bit, the A1454 will be able to provide a digital output that is fairly accurate, but not temperature compensated. Lastly, within a period of about 500 µs after clearing the sleep bit, the A1454 will be able to provide an output value that is accurate to within the device accuracy specifications.

Therefore, a design trade-off can be made between wake-up time, and accuracy of output, based on the specific system-level requirements.

Table 4: Sleep [0], Address 0x20, Bit Definition Table

Bits	Address	Name	Value	Description	R/W	Default
0	0x20	Sleep Mode	0/1	Sleep Mode Enable Bit	R/W	–

CHARACTERISTIC DEFINITIONS

Active Mode Response Time

The Active Mode Response Time, $t_{PACTIVE}$, is the time required to settle internal voltages with an applied magnetic field, after either V_{CC} is above $V_{CC(min)}$, or the command to activate from Sleep mode has been received. The I²C master can issue a command to activate the device from Sleep mode by clearing the SLEEP bit (CR 0x04, D0). After the SLEEP bit has been cleared, the device requires a finite time to power-on its internal components before accurately responding to an applied magnetic field. (Note: When coming out of Sleep mode, the IC acts as if it is being powered on. This means that all volatile registers are reset to their default values, and those registers which can be programmed into EEPROM are reloaded with what is in EEPROM.)

Maximum Applied Field

The A1454 device will be able to handle magnetic signals as large as B_{max} before internal amplifiers begin to saturate. Fields above these values will result in uncertain device operation outside specification limits.

LINEAR SENSITIVITY ERROR

The A1454 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive ($L_{inERRPOS}$) and negative ($L_{inERRNEG}$) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\ (\%)$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\ (\%)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x}$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent voltage output such that $|B_{POS2}| = 2 \times |B_{POS1}|$ and $|B_{NEG2}| = 2 \times |B_{NEG1}|$. In the above equation, $V_{OUT(Q)}$ is the quiescent voltage output, and $V_{OUT(Bx)}$ is the Hall voltage when the field, B_X, is applied.

Then:

$$Lin_{ERR} = max(Lin_{ERRPOS}, Lin_{ERRNEG})$$

I²C Interface

This is a serial interface that uses two bus lines, SCL and SDA, to access the internal control registers. Data is exchanged between a microcontroller (master) and the A1454 (slave). The clock input to SCL is generated by the master, while the SDA line functions as either an input or an open drain output, depending on the direction of the data.

The I²C input thresholds depend on the V_{CC} voltage of the A1454. The threshold levels over the operating V_{CC} range are compatible with 3 V logic.

TIMING CONSIDERATIONS

I²C communication is composed of several steps in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address Cycle. 7 bits of address, plus 1 bit to indicate write (0) or read (1), and an acknowledge bit.
3. Data Cycles. Reading or writing 8 bits of data followed by an acknowledge bit.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A1454 always responds by resetting the data transfer sequence.

The state of the Read/$\overline{\text{Write}}$ bit is set to 0 to indicate a write cycle and set to 1 to indicate a read cycle.

The master monitors for an acknowledge pulse to determine if the slave device is responding to the address byte sent to the A1454. When the A1454 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A1454 pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow the handshaking to occur.

I²C Command to Write to the A1454

The master controls the A1454 by programming it as a slave. To do so, the master transmits data bits to the SDA input of the A1454, in synchronization with the clocking signal the master transmits simultaneously on the SCL input.

A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA line (Stop bit). As shown in figure 1, between these points, the master transmits two address bytes, the first with the A1454 (chip) address bits and a write command bit (D0 = 0) and the second with the initial target register address, which are followed by the data bytes. After every byte, regardless of byte payload, the slave A1454 acknowledges by transmitting a low to the master on the SDA line.

Multiple data bytes can be written by one I²C sequence, as shown in Figure 2. After the slave acknowledges a data byte, instead of sending a Stop bit, the master sends the next data byte. Only after the final data byte is written and the slave acknowledges, does the master provide a Stop bit. The A1454 automatically directs each additional data byte to the next register, in order of regiter address number. Note that only the initial register address is required. This allows faster data entry, although it restricts data entry to sequential registers. If non-sequential registers are to be written, separate write commands can be sent.

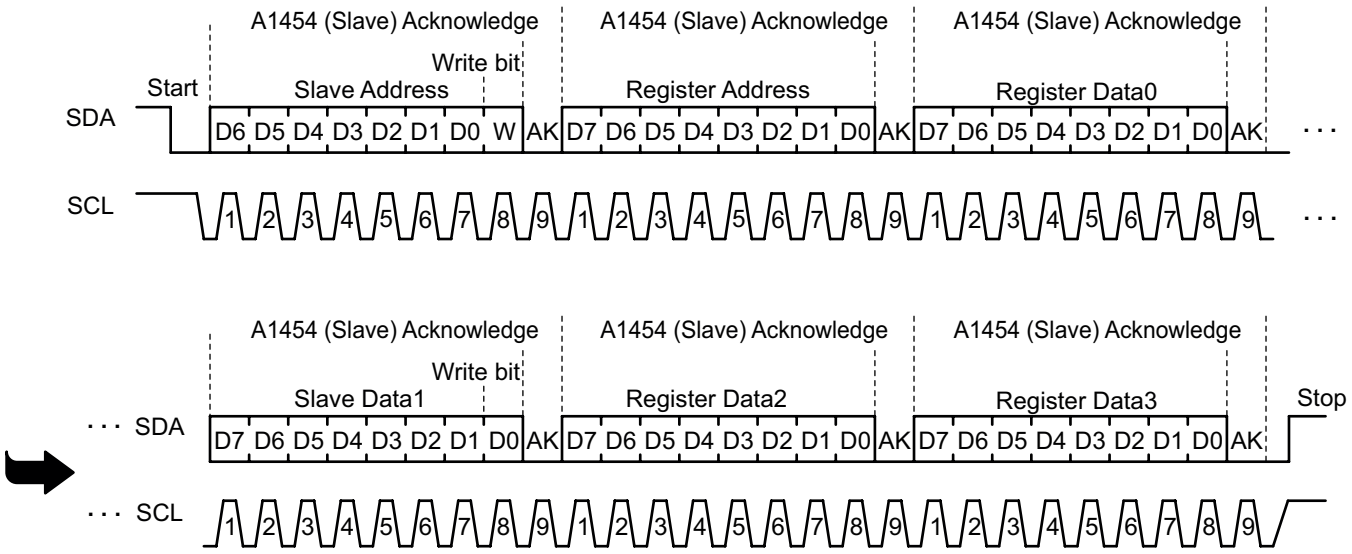


Figure 2: I²C Write Operation

Customer Write Access

Before attempting to write to any of the serial registers or EEPROM memory locations in the A1454, an access code must be entered, to put the device in customer access mode. If customer access mode is configured, then no writes to the device are allowed. The only exception this this is the SLEEP bit, which can be written regardless of the access mode. Furthermore, any register or EEPROM location can be read at any time regardless of the access mode.

To enter either customer access mode, an access command needs to be sent via the I²C interface. The command is simply a serial write operation with the address and data values as shown in Table 2. Once the access mode is set, it is not possible to change the mode without power-cycling the device. There is no time limit for entering the code.

Table 5: Customer Access Code

	Address	Data
Customer Access Mode	0x24	0x2C413534

I²C Command to Read from the A1454

This section applies to the reading of both volatile and non-volatile EEPROM registers. The master can read back the register values from the A1454. Similar to writing, the master transmits data bits to the SDA input of the A1454, in synchronization with the clocking signal the master transmits simultaneously on the SCL input.

A complete transmission consists of a read command from the master and a response from the A1454. It begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA line (Stop bit). As shown in Figure 3, between these points, the master transmits two address bytes, the first with the A1454 (chip) address bits and a write command bit (D0 = 0) and the second with the initial source register address. After each address byte, the slave A1454 acknowledges by transmitting a low to the master on the SDA line. The master then issues another Start bit (referred to as *restart*) followed by the same slave chip address and the Read/$\overline{\text{Write}}$ bit set to read (D0 = 1).

The A1454 then provides the data byte from the addressed regiter, synchronized with the clock pulse supplied by the master (the master must provide the clock pulses, as the A1454 slave does not have the capability to generate them).

In Figure 3, the transmission is of the entire contents of a single register location (bits 31:0). Optionally, the I²C master can continue to acknowledge instead of issuing a 'NACK' and stopping. This will result in the transfer of data [31:24] from Reg Address+1. The master can then continue acknowledging or issue the not acknowledge/stop after any byte to stop receiving data. Note that only the initial register address is required. This allows faster data retrieval, although it restricts data retrieval to sequential registers. When the master provides non-acknowledge bit and Stop bit, the A1454 stops sending data. If non-sequential registers are to be read, separate read commands can be sent.

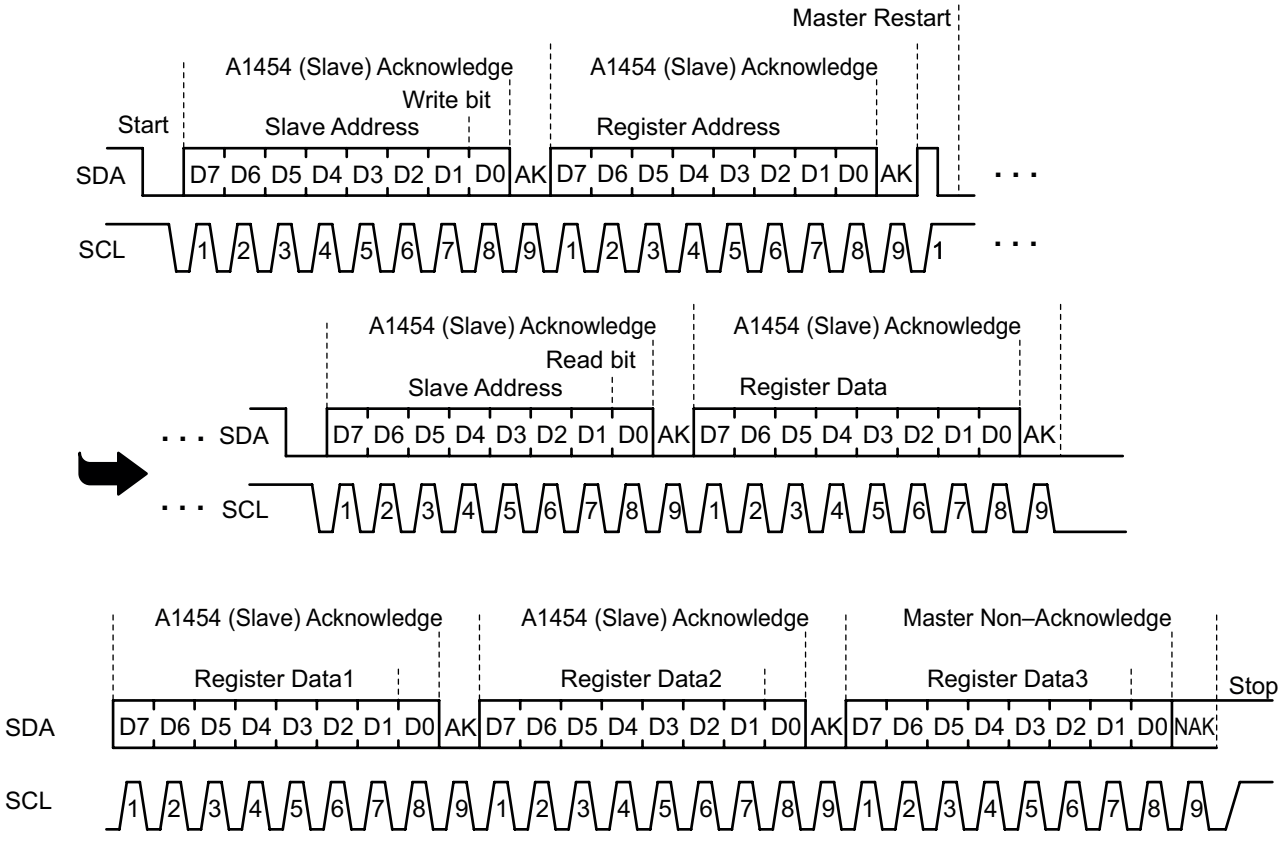


Figure 3: I²C Read Operation

I²C Address for the A1454

The default device address, in the case where VA0 and VA1 are set to VCC, is given by binary 1101 111[0/1], where the last bit determines if it is a read or a write instruction. For more options on slave addressing for the A1454, refer to the section: I²C Device (Slave) Address Coding.

EEPROM Functionality

The on-chip EEPROM is divided into eight rows, each thirty two bits long, with six of the MSBs being used for EEPROM ECC.

On power-up, all registers in EEPROM address 0x03 to 0x07 are loaded into the volatile registers which shadow them. For example, EE address 0x03 is loaded into registers 0x0C. The user can overwrite these volatile registers, and they will be reset to the values in the EEPROM only on a power cycle of the IC.

Programming EEPROM Blocks

Programming of the EEPROM is done through the I²C interface. Each row of EEPROM can only be written 1000 times. The I²C command for writing to EEPROM is very similar to the general I²C command for writing to the volatile serial registers in the A1454. Before attempting to write to EEPROM, please ensure that the device is in Customer Access Mode. For more details see the Customer Write Access section on page 7.

A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA line (Stop bit). As shown in Figure 4, between these points, the master transmits two address bytes, the first with the A1454 (chip) address bits and a write command bit (D0 = 0) and the second with the initial target EEPROM register address, which are followed by the data bytes. After every byte, regardless of byte payload, the slave A1454 acknowledges by transmitting a low to the master on the SDA line.

The 1454 always writes one entire EEPROM row at a time. As shown in Figure 4. After the slave acknowledges a data byte, the master sends the next data byte. Only after the final data byte is written and the slave acknowledges, does the master provide a Stop bit. The A1454 now takes these 4 data bytes and writes them to the requested register address. It takes the EEPROM 30 ms to perform the write command. After such time, the host can issue the next I²C EEPROM write command, if desired.

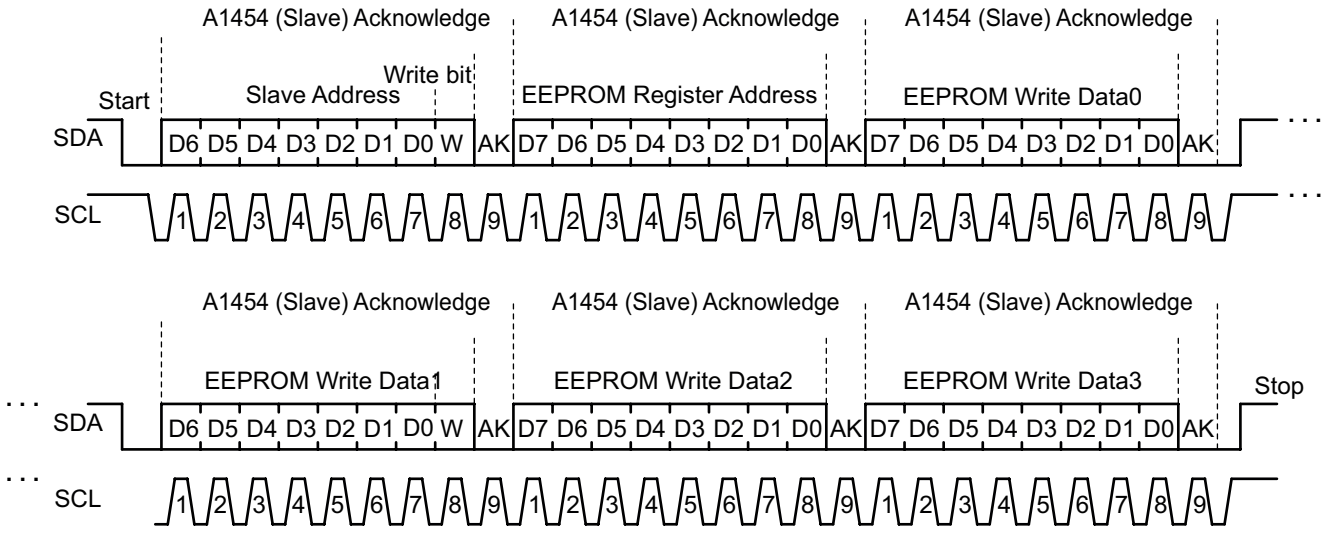


Figure 4: Programming EEPROM Blocks
This sequence enables programming of EEPROM blocks 2 through 3 from the volatile registers which shadow those blocks.

EEPROM Memory Check

The EEPROM Memory Check provides the capability to vary the EEPROM reference voltages and compare the data from each reference voltage, to ensure that no EEPROM memory cells are corrupted. A high reference voltage is used ensure that 1's are correctly programmed and a low reference voltage is used to ensure that the 0's are correctly programmed.

The Tables 6 and 7 describe the features available in customer accessible register EEPROM Check.

Table 6: Customer Accessible Register EEPROM Check

Register Name	Register Address	Bit Number						
		25:6						
EEPROM Check	0x1C	Unused	MM	MS		0	0	MCI

Table 7: Customer Accessible Register EEPROM Check

Parameter Name	Description	Value
MCI: Memory Check Initiate	The MCI bit can be written by the customer to initiate an EEPROM memory check procedure. This bit will self-clear upon completion of the memory test.	0: Reset Condition
		1: Start Memory Check
Bit 1	Must be set to '0'	0
Bit 2	Must be set to '0'	0
MS[1:0]: Memory Status	These are status bits that provide information on the progress and result of the Memory Check. These bits are cleared after a read, or a system reset.	00: Reset Condition
		01: Pass - No failure detected.
		10: Fail – Failure detected
		11: Running - Memory Check ongoing.
MM	In the case of MS [1:0] = [10], i.e. failure detected, MM will provide additional diagnostic information, indicating whether the failing memory reference was the low reference, or the high reference.	0: Low Reference Failed
		1: High Reference Failed

I²C Device (Slave) Address Coding

The four LSBs of the device (slave) address (A3, A2, A1, and A0) can be set by applying different voltages to pins ADR0 and ADR1 as show in figure X and defined in table X.

Table 1: A1454 I²C Address Bits

Address Bit						
A6	A5	A4	A3	A2	A1	A0
Binary Device Address Value						
0/1	0/1	0/1	0/1	0/1	0/1	0/1

Table 2: Slave Address Decoding

Voltage on AD1 Pin, V_{A1} (× VCC)	Voltage on AD0 Pin, V_{A0} (× VCC)	4-bit Code from ADR0 and ADR1 Voltages				Slave Address Bits							Slave Address
		E3	E2	E1	E0	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	1	1	0	0	0	0	0	96
	0.33	0	0	0	1	1	1	0	0	0	0	1	97
	0.67	0	0	1	0	1	1	0	0	0	1	0	98
	1	0	0	1	1	1	1	0	0	0	1	1	99
0.33	0	0	1	0	0	1	1	0	0	1	0	0	100
	0.33	0	1	0	1	1	1	0	0	1	0	1	101
	0.67	0	1	1	0	1	1	0	0	1	1	0	102
	1	0	1	1	1	1	1	0	0	1	1	1	103
0.67	0	1	0	0	0	1	1	0	1	0	0	0	104
	0.33	1	0	0	1	1	1	0	1	0	0	1	105
	0.67	1	0	1	0	1	1	0	1	0	1	0	106
	1	1	0	1	1	1	1	0	1	0	1	1	107
1	0	1	1	0	0	1	1	0	1	1	0	0	108
	0.33	1	1	1	0	1	1	0	1	1	1	0	109
	0.67	1	1	1	0	1	1	0	1	1	1	0	110
	1	1	1	1	1	X	X	X	X	X	X	X	Programmable: 0-127, (Using 7-bit EEPROM field). Set at factory for Default = 111

Note:
Different values for the three MSBs of the address (A6, A5, and A4) are available for factory programming if a conflict with other units occurs in the application design.

EEPROM Customer Space

Register 0x02 (Bits 25:0) are available as customer EEPROM space. This memory location is intended to be utilized by the user for storing information, such as factory time stamps, lot numbers, version numbers, and so forth. This registers is not shadowed, and so must be written 4 bytes at a time, as described in the Programming EEPROM section (second method). Also, as with all the EEPROM registers, these registers can only be written to 1000 times.

Table 3: EEPROM Memory Map

ADR	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	Auto ECC Bits						Factory Access Only																									
0x01	Auto ECC Bits						Factory Access Only																									
0x02	Auto ECC Bits						Customer ID																									
0x03	Auto ECC Bits						Test_Field_TBD																			Cust_Slave_Address						
0x04	Auto ECC Bits						Factory Locked																									
0x05	Auto ECC Bits						Factory Locked																									
0x06	Auto ECC Bits						Factory Locked																									
0x07	Auto ECC Bits						Factory Locked																									

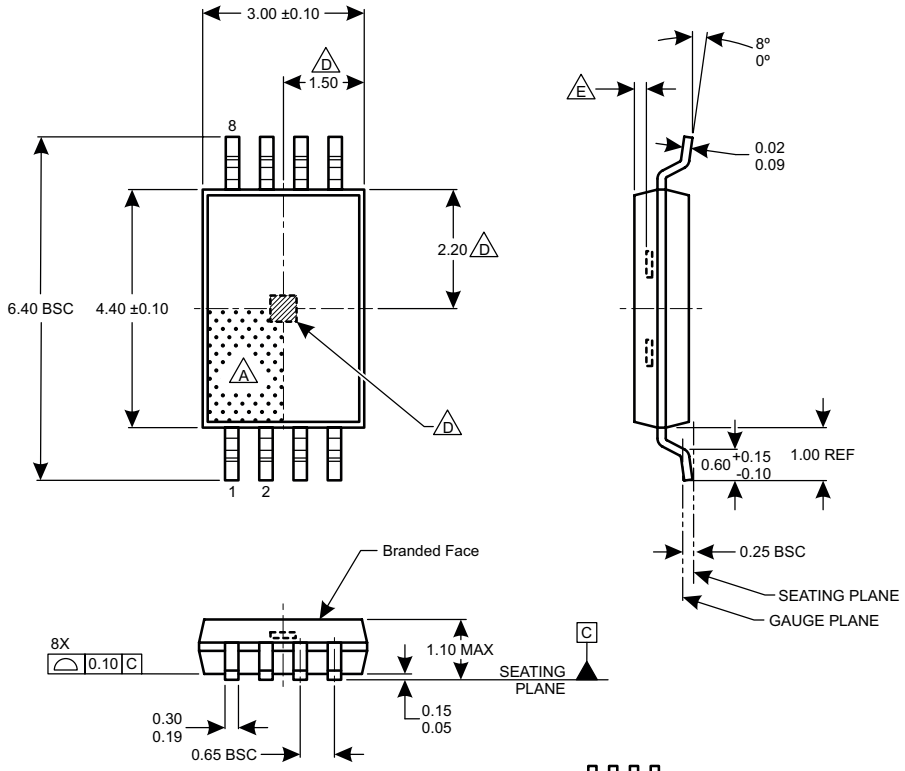
Table 4: Volatile Register That Shadow EEPROM (registers are loaded from EEPROM on power-up)

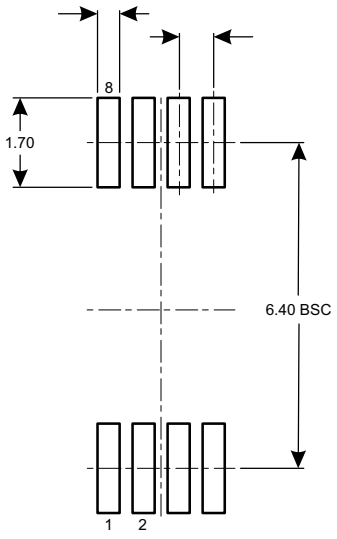
ADR	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0B	Auto ECC Bits						Test_Field_TBD																			Cust_Slave_Address						
0x0C	Auto ECC Bits						Factory Locked																									
0x0D	Auto ECC Bits						Factory Locked																									
0x0E	Auto ECC Bits						Factory Locked																									
0x0F	Auto ECC Bits						Factory Locked																									

PACKAGE OUTLINE DIAGRAM

For Reference Only – Not for Tooling Use

(Reference MO-153 AA)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





B PCB Layout Reference View

C Standard Branding Reference View

N = Last 3 digits of device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth = 0.36 mm REF

Figure 5: Package LE, 8-Pin TSSOP

Revision History

Revision	Current Revision Date	Description of Revision
–	April 3, 2015	Initial Release

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