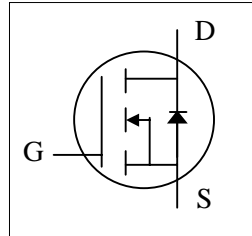




- ▼ Simple Drive Requirement
- ▼ SO-8 Compatible with Heatsink
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

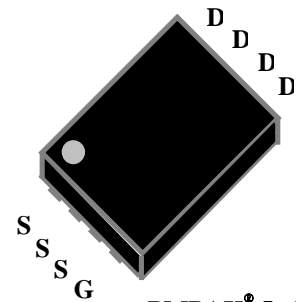


$BV_{DSS}$	80V
$R_{DS(ON)}$	3.9m $\Omega$
$I_D^4$	120A

### Description

AP8600 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK<sup>®</sup> 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



**PMPAK<sup>®</sup> 5x6**

### Absolute Maximum Ratings @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	80	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current (Chip), $V_{GS} @ 10V^4$	120	A
$I_D @ T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	26.6	A
$I_D @ T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	21.3	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	240	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	104	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation <sup>3</sup>	5	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>5</sup>	86.4	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	1.2	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	25	$^\circ\text{C}/\text{W}$



**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	80	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =19A	-	-	3.9	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	-	5	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =19A	-	50	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =64V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±300	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =19A	-	67	107	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =40V	-	17	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =10V	-	15	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =40V	-	15	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =19A	-	45	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =6Ω	-	58	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	85	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	4000	6400	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =40V	-	900	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	30	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	2	4	Ω

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =19A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =19A, V <sub>GS</sub> =0V,	-	65	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	90	-	nC

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t ≤10sec; 60°C/W at steady state.
- 4.Package limitation current is 60A .
- 5.Starting T<sub>j</sub>=25°C , V<sub>DD</sub>=40V , L=0.3mH , R<sub>G</sub>=25Ω

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

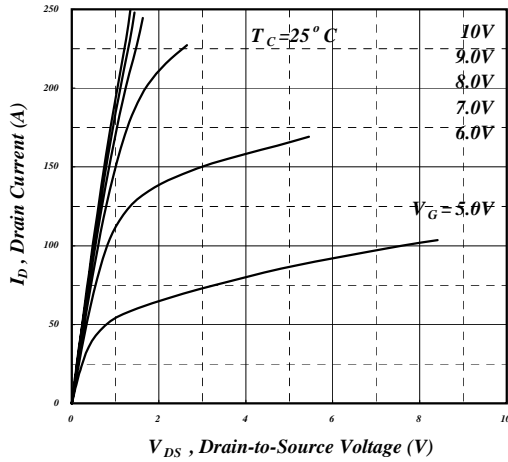


Fig 1. Typical Output Characteristics

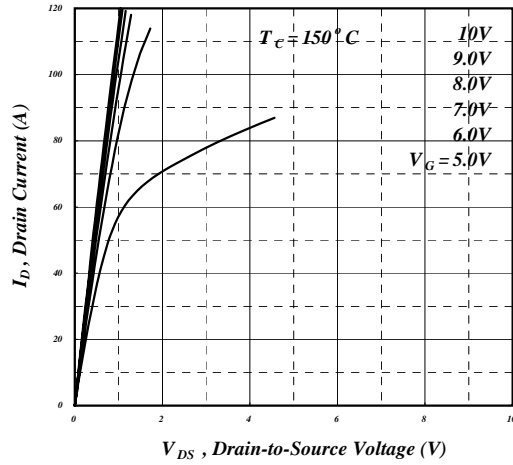


Fig 2. Typical Output Characteristics

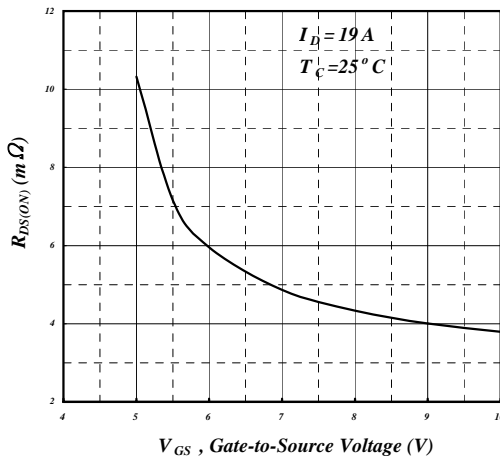


Fig 3. On-Resistance v.s. Gate Voltage

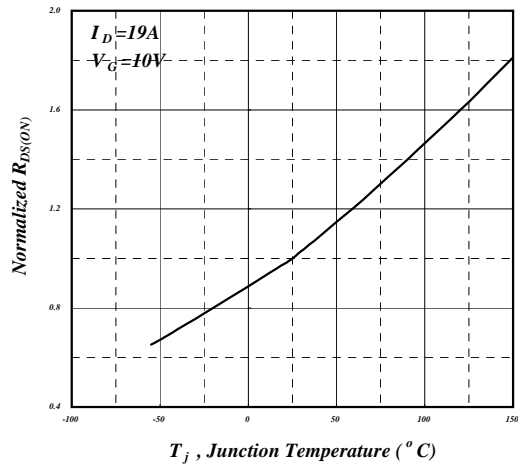


Fig 4. Normalized On-Resistance v.s. Junction Temperature

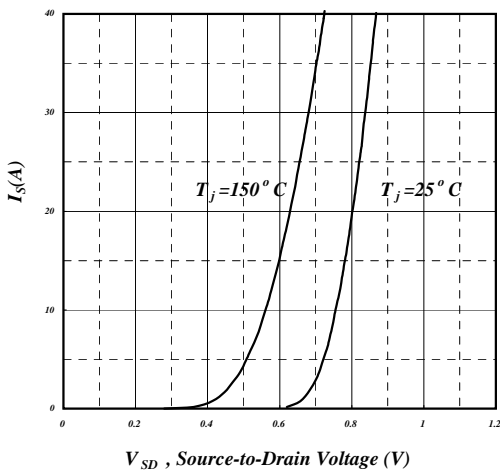


Fig 5. Forward Characteristic of Reverse Diode

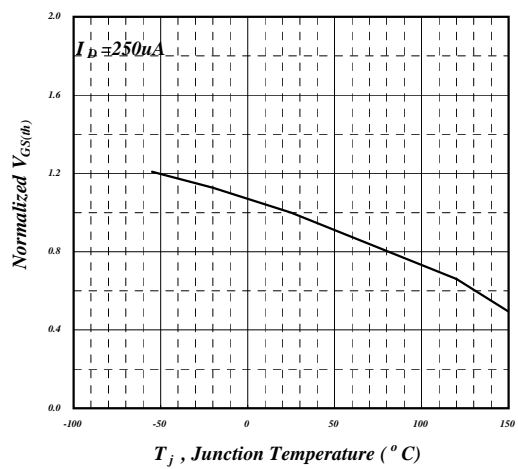


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

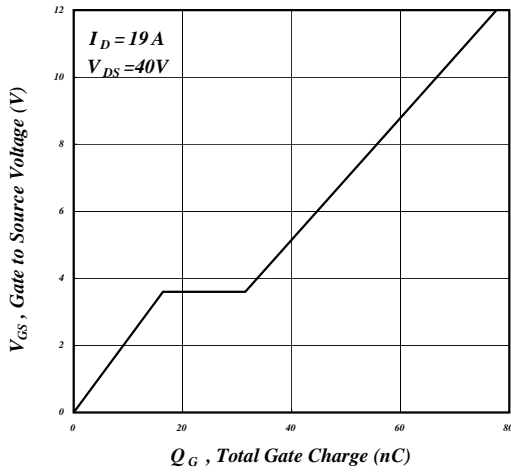


Fig 7. Gate Charge Characteristics

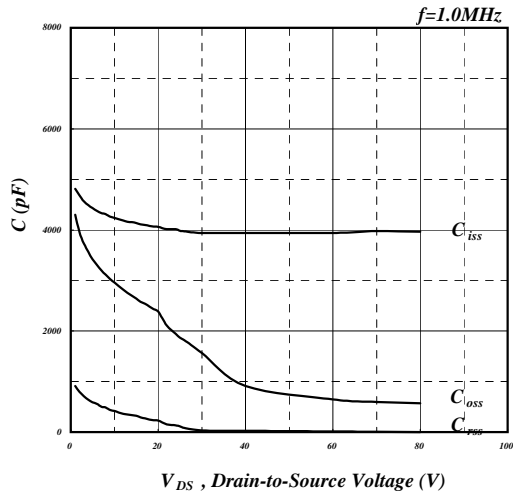


Fig 8. Typical Capacitance Characteristics

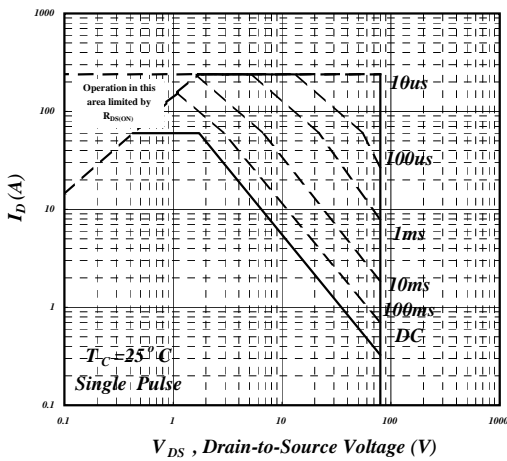


Fig 9. Maximum Safe Operating Area

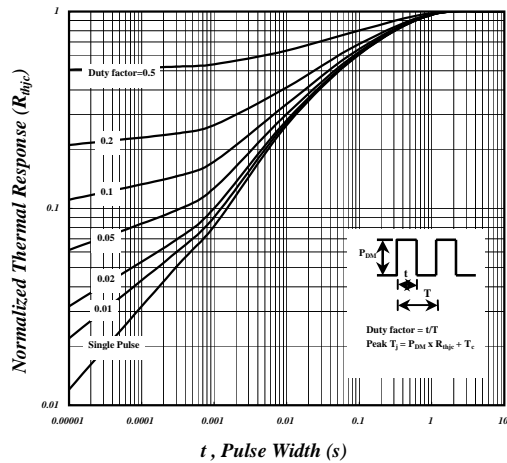


Fig 10. Effective Transient Thermal Impedance

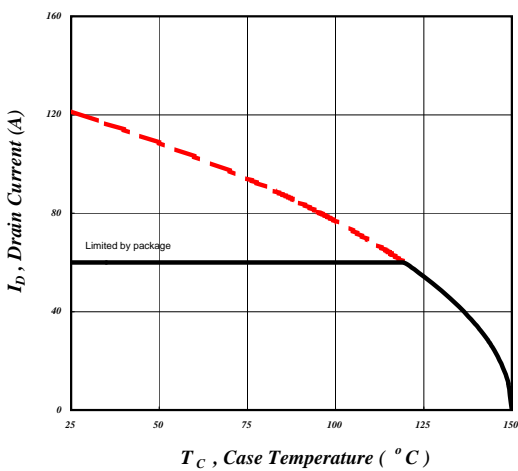


Fig 11. Drain Current v.s. Case Temperature

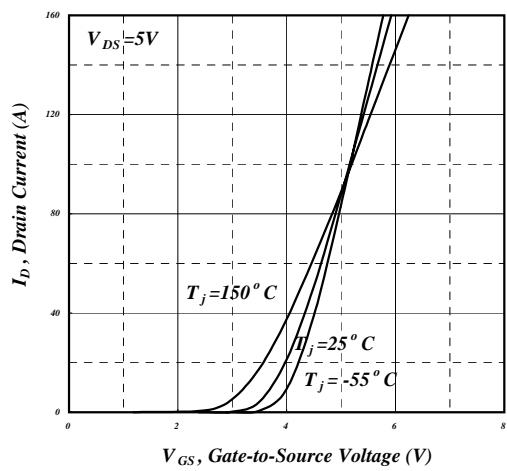


Fig 12. Transfer Characteristics

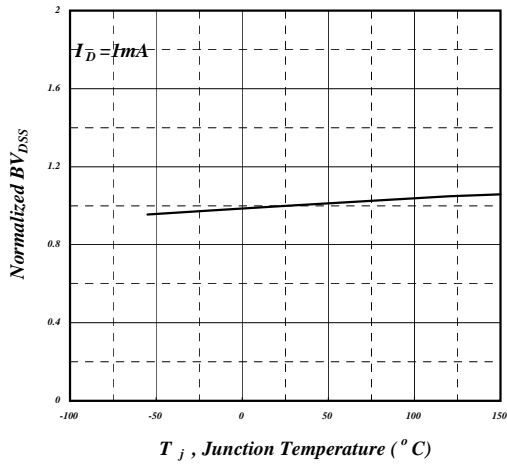


Fig 13. Normalized  $BV_{DSS}$  v.s. Junction Temperature

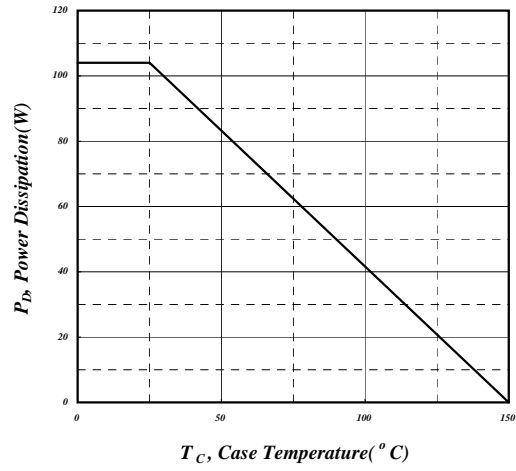


Fig 14. Total Power Dissipation

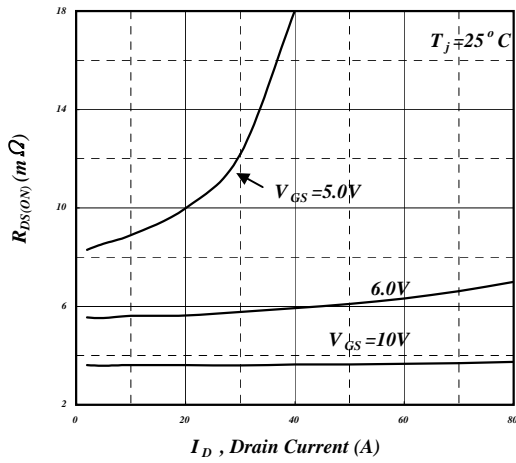
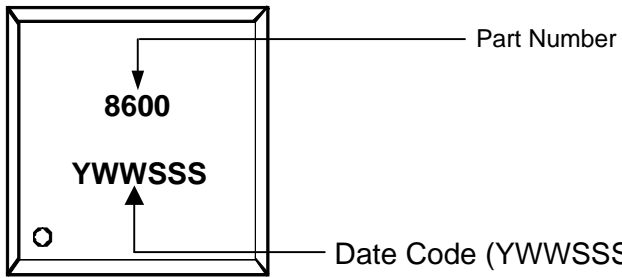


Fig 15. Typ. Drain-Source on State Resistance



**MARKING INFORMATION**



Date Code (YWWSSS)

Y : Last Digit Of The Year

WW : Week

SSS : Sequence