HV2601 / HV2701

Low-Charge Injection, 16-Channel, High-Voltage Analog Switch

Features

- High-Voltage CMOS technology for high performance
- 16-channel high voltage analog switch
- 3.3V input logic level compatible
- 20 MHz data shift clock frequency
- Very low quiescent power dissipation (-10 µA)
- Low parasitic capacitance
- DC to 50 MHz small signal frequency response
- -60dB typical OFF-isolation at 5.0 MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages
- Integrated bleed resistors on the outputs (HV2701 only)

Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Optical MEMS modules

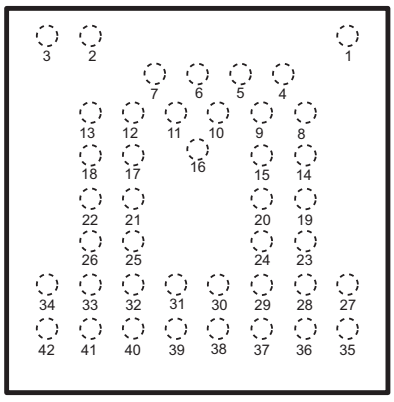
Description

HV2601/HV2701 are low-charge injection, 16-channel, high-voltage analog switch integrated circuits (ICs). These devices are designed for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging and other piezoelectric transducer drivers. HV2701 has integrated bleed resistors which eliminate voltage build-up on capacitive loads such as piezoelectric transducers.

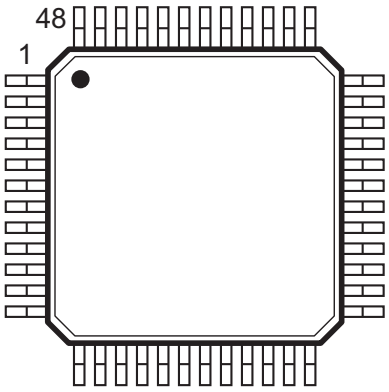
These ICs shift input data into a 16-bit shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock. Using High-Voltage CMOS technology, this device combines high-voltage, bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN}: +40V/-160V, +100V/-100V, and +160V/-40V.

Package Types



42-Ball Bumped Die (Top View)



48-Lead LQFP (Top View)

See Table 2-1 and Table 2-2 for pin information

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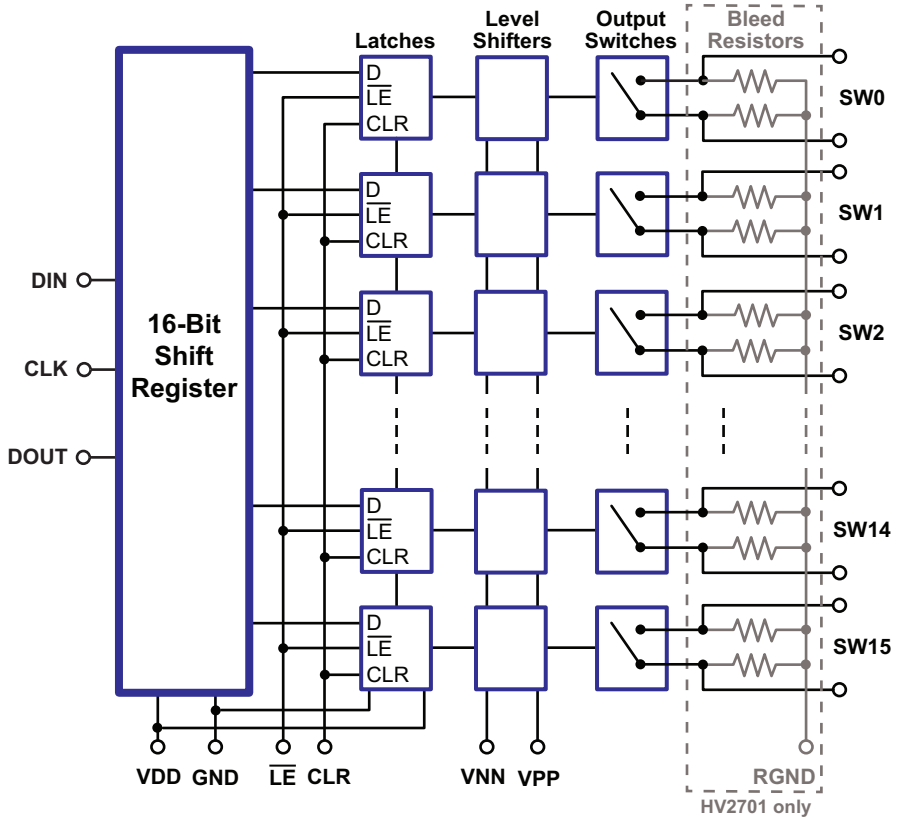
Block Diagram



Note: Bleed resistors and RGND apply to HV2701 only.

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1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

V_{DD} logic supply ..... -0.5V to +7.0V
V_{PP} - V_{NN} differential supply 220V
V_{PP} positive supply ..... -0.5V to V_{NN} + 200V
V_{NN} negative supply ..... +0.5V to -200V
Logic input voltage ..... -0.5V to V_{DD} + 0.3V
Analog signal range ..... V_{NN} to V_{PP}
Peak analog signal current/channel 3.0A
Storage temperature ..... -65°C to +150°C
Power dissipation 42-Ball Bumped Die 1.5W
Power dissipation 48-Lead LQFP 1.0W

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Notes 1 – 3)

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1 V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

Note 1: Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.

2: V_{SIG} must be V_{NN} and V_{PP} or floating during power up/down transition.

3: Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Symbol	0°C		25°C			70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
Small signal switch ON-resistance	R_{ONS}	-	30	-	26	38	-	48	Ω	I_{SIG}= 5.0 mA	V_{PP}= +40V V_{NN}= -160V
		-	25	-	22	27	-	32		I_{SIG}= 200 mA	
		-	25	-	22	27	-	30		I_{SIG}= 5.0 mA	V_{PP}= +100V V_{NN}= -100V
		-	18	-	18	24	-	27		I_{SIG}= 200 mA	
		-	23	-	20	25	-	30		I_{SIG}= 5.0 mA	V_{PP}= +160V V_{NN}= -40V
		-	22	-	16	25	-	27		I_{SIG}= 200 mA	
Small signal switch ON-resistance matching	ΔR_{ONS}	-	20	-	5.0	20	-	20	%	I_{SIG}= 5.0mA, V_{PP}= +100V, V_{NN}= -100V	
Large signal switch ON-resistance	R_{ONL}	-	-	-	15	-	-	-	Ω	V_{SIG}= V_{PP}-10V, I_{SIG}= 1.0A	
Value of output bleed resistor (HV2701 only)	R_{INT}	-	-	20	35	50	-	-	kΩ	Output Switch to R_{GND} I_{RINT}= 0.5 mA	
Switch OFF leakage per switch	I_{SOL}	-	5.0	-	1.0	10	-	15	µA	V_{SIG}= V_{PP}-10V and V_{NN}+10V (Note 1)	
DC offset switch OFF	V_{OS}	-	300	-	100	300	-	300	mV	HV2601:100 kΩ load HV2701: no load (Note 1)	
DC offset switch ON		-	500	-	100	500	-	500	mV		
Quiescent V_{PP} supply current	I_{PPQ}	-	-	-	10	50	-	-	µA	All switches OFF	
Quiescent V_{NN} supply current	I_{NNQ}	-	-	-	-10	-50	-	-	µA	All switches OFF	
Quiescent V_{PP} supply current	I_{PPQ}	-	-	-	10	50	-	-	µA	All switches ON, I_{SW}= 5.0 mA	
Quiescent V_{NN} supply current	I_{NNQ}	-	-	-	-10	-50	-	-	µA	All switches ON, I_{SW}= 5.0 mA	
Switch output peak current	I_{SW}	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
Output switching frequency	f_{SW}	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
Average V_{PP} supply current	I_{PP}	-	6.5	-	-	7.0	-	8.0	mA	V_{PP}= +40V V_{NN}= -160V	All output switches are turning ON and OFF at 50 kHz with no load.
		-	4.0	-	-	5.5	-	5.5		V_{PP}= +100V V_{NN}= -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP}= +160V V_{NN}= -40V	
Average V_{NN} supply current	I_{NN}	-	6.5	-	-	7.0	-	8.0	mA	V_{PP}= +40V V_{NN}= -160V	All output switches are turning ON and OFF at 50 kHz with no load.
		-	4.0	-	-	5.0	-	5.5		V_{PP}= +100V V_{NN}= -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP}= +160V V_{NN}= -40V	
Average V_{DD} supply current	I_{DD}	-	4.0	-	-	4.0	-	4.0	mA	f_{CLK}= 5.0 MHz, V_{DD}= 5.0V	

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over recommended operating conditions unless otherwise noted.

Parameter	Symbol	0°C		25°C			70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
Quiescent V_{DD} supply current	I_{DDQ}	-	10	-	-	10	-	10	µA	All logic inputs are static
Data out source current	I_{SOR}	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT}= V_{DD}- 0.7V
Data out sink current	I_{SINK}	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT}= 0.7V
Logic input capacitance	C_{IN}	-	10	-	-	10	-	10	pF	–

Note 1: See Figure 3-1.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD}=5.0V, t_R = t_F≤5.0 ns, 50% duty cycle, C_{LOAD} = 20 pF, unless otherwise noted.

Parameter	Symbol	0°C		25°C			70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
Set up time before $\overline{LE}$ rises	t_{SD}	25	-	25	-	-	25	-	ns	–
Time width of $\overline{LE}$	t_{WLE}	56	-	-	56	-	56	-	ns	V_{DD}= 3.0V
		12	-	-	12	-	12	-		V_{DD}= 5.0V
Clock delay time to data out	t_{DO}	50	100	50	78	100	50	100	ns	V_{DD}= 3.0V
		15	40	15	30	40	15	40		V_{DD}= 5.0V
Time width of CLR	t_{WCLR}	55	-	55	-	-	55	-	ns	–
Set up time data to clock	t_{SU}	21	-	-	21	-	21	-	ns	V_{DD}= 3.0V
		7.0	-	-	7.0	-	7.0	-		V_{DD}= 5.0V
Hold time data from clock	t_H	2.0	-	2.0	-	-	2.0	-	ns	V_{DD}= 3.0 or 5.0V
Clock frequency	f_{CLK}	-	8.0	-	-	8.0	-	8.0	MHz	V_{DD}= 3.0V
		-	20	-	-	20	-	20		V_{DD}= 5.0V
Clock rise and fall times	t_R,t_F	-	50	-	-	50	-	50	ns	–
Turn ON time	T_{ON}	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG}= V_{PP}-10V, R_{LOAD}= 10kΩ (Note 1)
Turn OFF time	T_{OFF}	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG}= V_{PP}-10V, R_{LOAD}= 10kΩ (Note 1)
Maximum V_{SIG} slew rate	dv/dt	-	20	-	-	20	-	20	v/ns	V_{PP}= +40V, VNN= -160V
		-	20	-	-	20	-	20		V_{PP}= +100V, VNN= -100V
		-	20	-	-	20	-	20		V_{PP}= +160V, VNN= -40V
OFF isolation	K_O	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ//15pF load (Note 1)
		-58	-	-58	-	-	-58	-		f = 5.0MHz, 50Ω load (Note 1)
Switch crosstalk	K_{CR}	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load (Note 1)
Output switch isolation diode current	I_{ID}	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle (Note 1)
OFF capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
ON capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
Output voltage spike	$+V_{SPK}$	-	-	-	-	150	-	-	mV	V_{PP}= +40V, V_{NN}= -160V, R_{LOAD}= 50Ω (Note 1)
	$-V_{SPK}$									
	$+V_{SPK}$	-	-	-	-	150	-	-		V_{PP}= +100V, V_{NN}= -100V, R_{LOAD}= 50Ω (Note 1)
	$-V_{SPK}$									
	$+V_{SPK}$	-	-	-	-	150	-	-		V_{PP}= +160V, V_{NN}= -40V, R_{LOAD}= 50Ω (Note 1)
	$-V_{SPK}$									
Charge injection	QC	-	-	-	820	-	-	-	pC	V_{PP}= +40V, V_{NN}= -160V, V_{SIG}= 0V (Note 1)
		-	-	-	600	-	-	-		V_{PP}= +100V, V_{NN}= -100V, V_{SIG}= 0V (Note 1)
		-	-	-	350	-	-	-		V_{PP}= +160V, V_{NN}= -40V, V_{SIG}= 0V (Note 1)

Note 1: See Figure 3-1.

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2.0 PIN DESCRIPTION

The locations of the pads/balls are listed in Package Types.

TABLE 2-1: PIN DESCRIPTION: 42-BALL BUMPED DIE PACKAGE

Pin #	HV2601	HV2701	Description
1	NC	RGND	No connect/Ground for bleed resistor
2	V_{PP}	V_{PP}	Positive supply voltage
3	V_{NN}	V_{NN}	Negative supply voltage
4	D_{OUT}	D_{OUT}	Data out logic output
5	CLR	CLR	Latch clear logic input
6	CLK	CLK	Clock logic input for shift register
7	GND	GND	Ground
8	SW15A	SW15A	Analog switch 15 terminal A
9	SW15B	SW15B	Analog switch 15 terminal B
10	$\overline{LE}$	$\overline{LE}$	Latch-enable logic input, low active
11	V_{DD}	V_{DD}	Logic supply voltage
12	SW0A	SW0A	Analog switch 0 terminal A
13	SW0B	SW0B	Analog switch 0 terminal B
14	SW14A	SW14A	Analog switch 14 terminal A
15	SW14B	SW14B	Analog switch 14 terminal B
16	D_{IN}	D_{IN}	Data in logic input
17	SW1A	SW1A	Analog switch 1 terminal A
18	SW1B	SW1B	Analog switch 1 terminal B
19	SW13A	SW13A	Analog switch 13 terminal A
20	SW13B	SW13B	Analog switch 13 terminal B
21	SW2A	SW2A	Analog switch 2 terminal A
22	SW2B	SW2B	Analog switch 2 terminal B
23	SW12A	SW12A	Analog switch 12 terminal A
24	SW12B	SW12B	Analog switch 12 terminal B
25	SW3A	SW3A	Analog switch 3 terminal A
26	SW3B	SW3B	Analog switch 3 terminal B
27	SW11A	SW11A	Analog switch 11 terminal A
28	SW11B	SW11B	Analog switch 11 terminal B
29	SW9B	SW9B	Analog switch 9 terminal B
30	SW8B	SW8B	Analog switch 8 terminal B
31	SW7A	SW7A	Analog switch 7 terminal A
32	SW6A	SW6A	Analog switch 6 terminal A
33	SW4A	SW4A	Analog switch 4 terminal A
34	SW4B	SW4B	Analog switch 4 terminal B
35	SW10B	SW10B	Analog switch 10 terminal B
36	SW10A	SW10A	Analog switch 10 terminal A
37	SW9A	SW9A	Analog switch 9 terminal A
38	SW8A	SW8A	Analog switch 8 terminal A
39	SW7B	SW7B	Analog switch 7 terminal B
40	SW6B	SW6B	Analog switch 6 terminal B
41	SW5B	SW5B	Analog switch 5 terminal B
42	SW5A	SW5A	Analog switch 5 terminal A

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TABLE 2-2: PIN DESCRIPTION: 48-LEAD LQFP

Pin #	HV2601	HV2701	Description
1	NC	NC	No connect
2	NC	NC	No connect
3	SW4B	SW4B	Analog switch 4 terminal B
4	SW4A	SW4A	Analog switch 4 terminal A
5	SW3B	SW3B	Analog switch 3 terminal B
6	SW3A	SW3A	Analog switch 3 terminal A
7	SW2B	SW2B	Analog switch 2 terminal B
8	SW2A	SW2A	Analog switch 2 terminal A
9	SW1B	SW1B	Analog switch 1 terminal B
10	SW1A	SW1A	Analog switch 1 terminal A
11	SW0B	SW0B	Analog switch 0 terminal B
12	SW0A	SW0A	Analog switch 0 terminal A
13	V_{NN}	V_{NN}	Negative supply voltage
14	NC	NC	No connect
15	V_{PP}	V_{PP}	Positive supply voltage
16	NC	NC	No connect
17	GND	GND	Ground
18	V_{DD}	V_{DD}	Logic supply voltage
19	D_{IN}	D_{IN}	Data in logic input
20	CLK	CLK	Clock logic input for shift register
21	$\overline{LE}$	$\overline{LE}$	Latch-enable logic input, low active
22	CLR	CLR	Latch clear logic input
23	D_{OUT}	D_{OUT}	Data out logic output
24	NC	RGND	No connect/Ground for bleed resistor
25	SW15B	SW15B	Analog switch 15 terminal B
26	SW15A	SW15A	Analog switch 15 terminal A
27	SW14B	SW14B	Analog switch 14 terminal B
28	SW14A	SW14A	Analog switch 14 terminal A
29	SW13B	SW13B	Analog switch 13 terminal B
30	SW13A	SW13A	Analog switch 13 terminal A
31	SW12B	SW12B	Analog switch 12 terminal B
32	SW12A	SW12A	Analog switch 12 terminal A
33	SW11B	SW11B	Analog switch 11 terminal B
34	SW11A	SW11A	Analog switch 11 terminal A
35	NC	NC	No connect
36	NC	NC	No connect
37	SW10B	SW10B	Analog switch 10 terminal B
38	SW10A	SW10A	Analog switch 10 terminal A
39	SW9B	SW9B	Analog switch 9 terminal B
40	SW9A	SW9A	Analog switch 9 terminal A
41	SW8B	SW8B	Analog switch 8 terminal B
42	SW8A	SW8A	Analog switch 8 terminal A
43	SW7B	SW7B	Analog switch 7 terminal B

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TABLE 2-2: PIN DESCRIPTION: 48-LEAD LQFP

Pin #	HV2601	HV2701	Description
44	SW7A	SW7A	Analog switch 7 terminal A
45	SW6B	SW6B	Analog switch 6 terminal B
46	SW6A	SW6A	Analog switch 6 terminal A
47	SW5B	SW5B	Analog switch 5 terminal B
48	SW5A	SW5A	Analog switch 5 terminal A

3.0 DETAILED DESCRIPTION

3.1 Application Information

FIGURE 3-1: TEST CIRCUITS

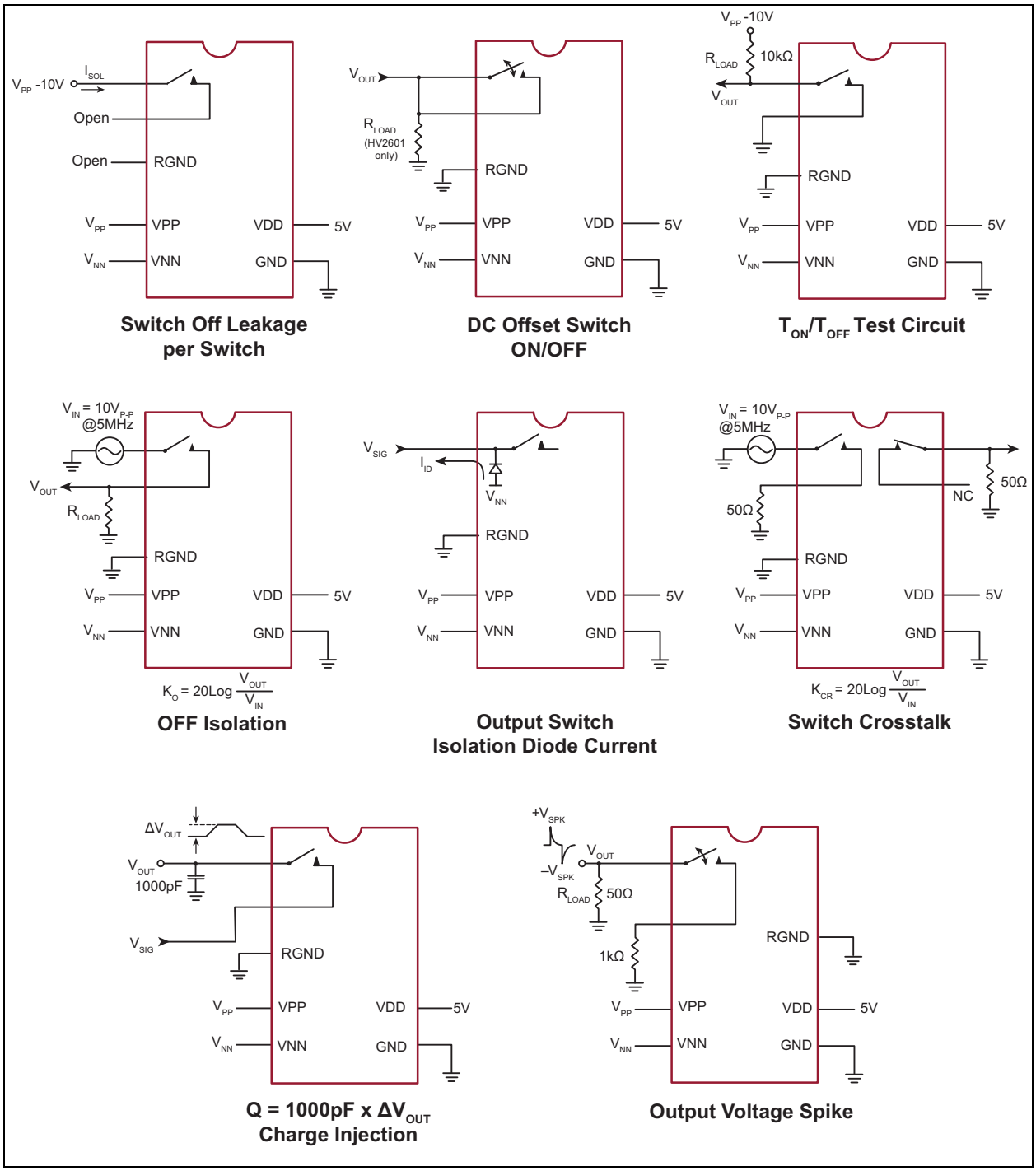

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TABLE 3-1: LOGIC FUNCTION TABLE

D0	D1	...	D7	D8	...	D15	LE	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-	...	-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 16 switches operate independently.

2: Serial data is clocked in on the L to H transition of the CLK.

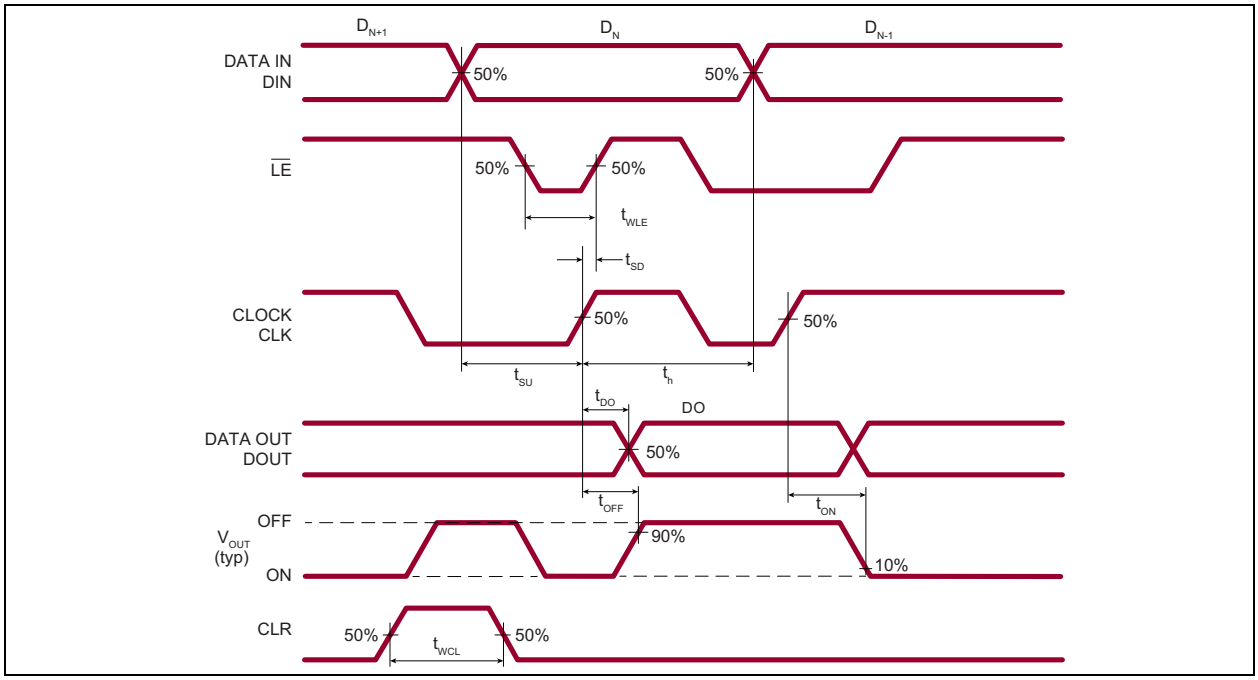
3: All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.

4: D_{OUT} is high when data in the shift register 15 is high.

5: Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR clear input overrides all other inputs.

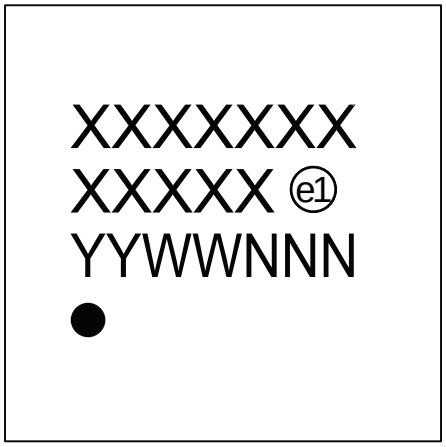
FIGURE 3-2: LOGIC TIMING WAVEFORMS



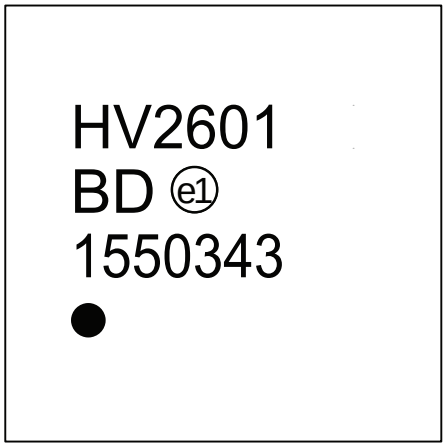
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

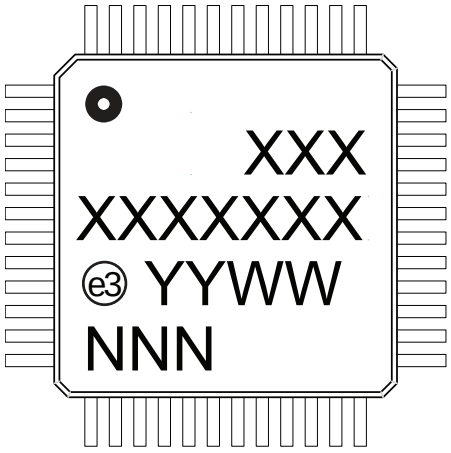
42-ball Bumped Die



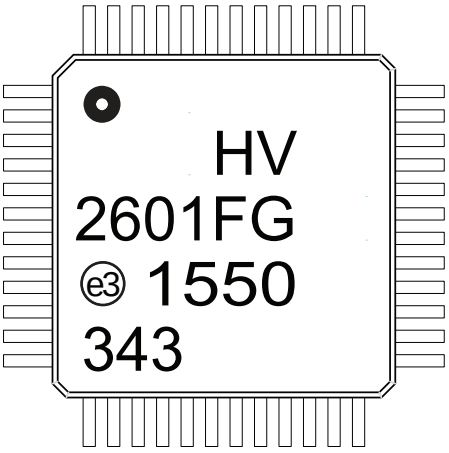
Example



48-lead LQFP



Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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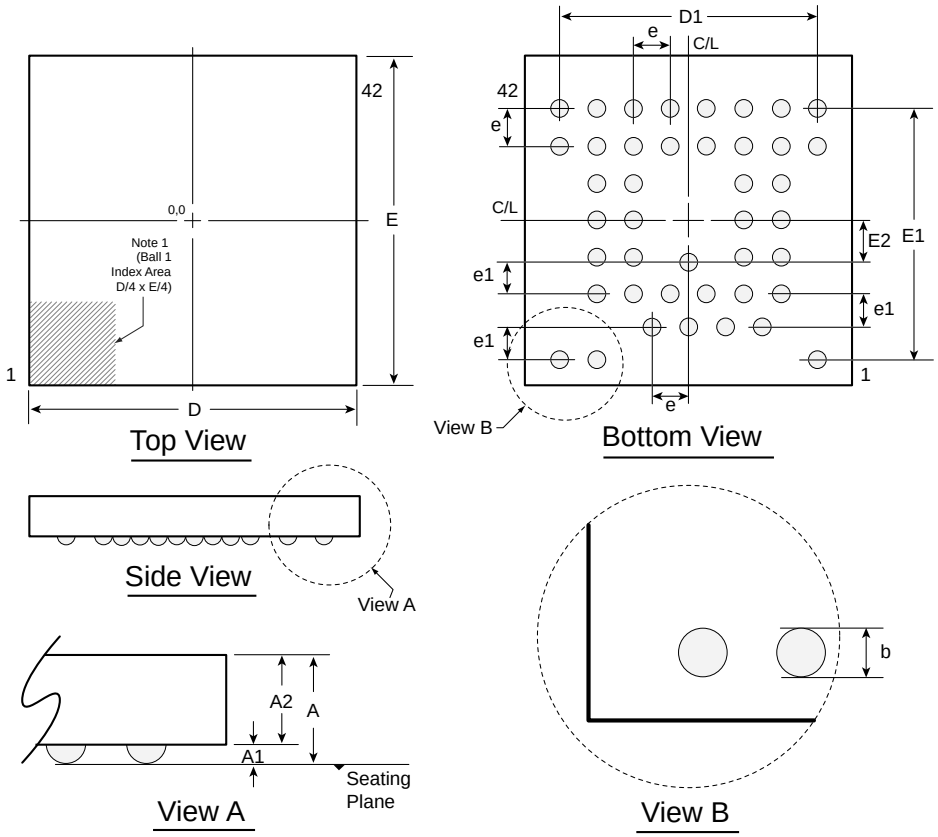
42-Ball Bumped Die Package Outline (BD)

5.29x5.30mm body, 1.0 mm height (max), 0.52 / 0.60mm pitch



1RWH)RU WKH PRVW FXUUHQW SDFNDJH GUDZLQJV SOHDVH VHH WKH 0LFURFKLS 3DFNDJLQJ 6SHFLILFDWLRQ ORFDWHG DW KWWS ZZZ PLFURFKLS FRP SDFN

Notes:

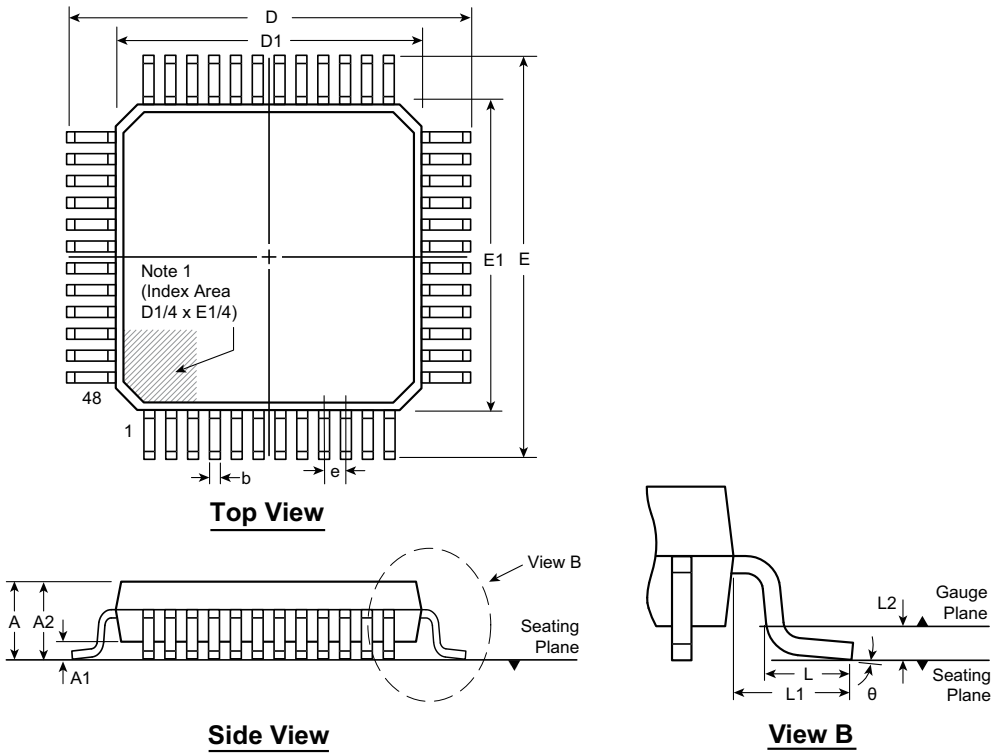
1. %DOO LGHQWLILHU PXVW EH ORFDWHG LQ WKH LQGLFDWHG]RQH DQG PD\ EH HLWKHU D FLUFXODU RU HOOLSWLFDO VKDSH 7KH EDOO LGHQWLILHU PD\ EH HOHYDWHG RU PD\ EH SDUW RI WKH SDFNDJH PDWHULDO 2ULHQWDWLRQ PXVW EH LQGLFDWHG E\ WKH SUHVHQFH RI D SLQ RU SDG RI D GLIIHUHQW VL]H RU VKDSH WKDQ WKH RWKHU SLQV RU SDGV RU E\ D SULQWHG LQGLFDWRU

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	e1
Dimension (mm)	MIN	0.9	0.21	0.	0.29	5.19	4.20 BSC	5.20	4.04 BSC	0.68 BSC	0.60 BSC	0.52 BSC
	NOM	0.9 5	0.24	0.7	0.32	5.29		5.30				
	MAX	1.0	0.27	0.7	0.35	5.39		5.40				

Note: For more information about ball coordinates, contact Microchip sales.

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Converted Supertex Doc #s DSFP-HV2601 and DSFP-HV2701 to Microchip DS20005391B.
- Combined HV2601/HV2701 into one document.
- Revised **Section 4.0 “Packaging Information”**
- Removed package GA from the data sheet.
- Made minor text changes throughout.

Revision B (March 2016)

- Moved **“Block Diagram”** to page 2 and made a minor change for clarity.
- Removed Confidential status from document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package		Environmental		Media Type

Device:	HV2601 = 16-Channel HV Analog Switch HV2701 = 16-Channel HV Analog Switch with Bleed Resistors	
Package:	BD = 42-Ball Bumped Die FG = 48-lead LQFP	
Environmental	G = Lead (Pb)-free/ROHS-compliant package (not used for BD packages)	
Media Type:	(blank) = 250/Tray for FG package M931 = 1000/Reel for FG package M936 = 2500/Reel for BD package	

Examples:

a) HV2601FG-G: 48-lead LQFP package, 250/Tray

b) HV2601FG-G-M931: 48-lead LQFP package, 1000/Reel

c) HV2701BD-M936 42-ball Bumped Die, 2500/Reel

Note: HV2601BD and HV2701BD are RoHS-compliant products

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