PL613-01

1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC

Features

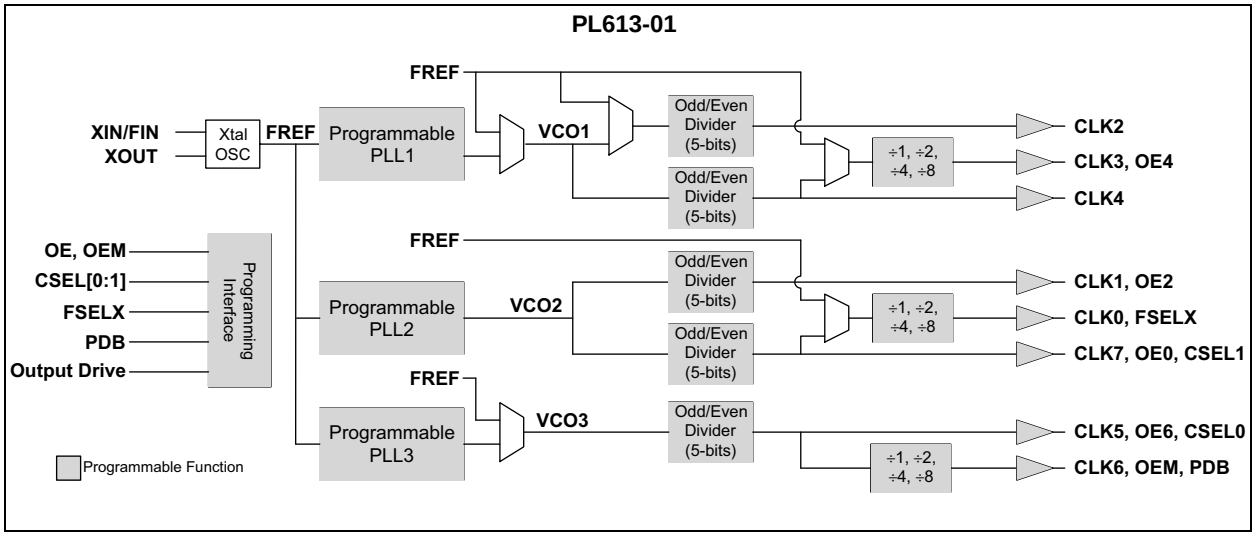
- Designed for PCB Space Savings with Three Low-Power Programmable PLLs and up to 8 Clock Outputs
- Low Power Consumption
  - 10 µA Typical When PDB is Activated
- Output Frequency:
  - ≤110 MHz at 1.8V Operation
  - ≤166 MHz at 2.5V Operation
  - ≤200 MHz at 3.3V Operation
- Input Frequency:
  - Fundamental Crystal: 10 MHz to 40 MHz
  - Reference Input: 10 MHz to 200 MHz
- Programmable I/O Pins Can be Configured as Output Enable (OE), Configuration Switching (CSEL), Frequency Switching (FSELX), Power Down (PDB) Inputs, or Clock Outputs
- Disabled Outputs Programmable as HiZ or Active Low
- Four Distinct Configurations Selectable with CSEL[0:1]
- Single 1.8V, 2.5V, or 3.3V ±10% Power Supply
- Temperature range: 0°C to 70°C, –40°C to +85°C
- Available in 3 mm x 3 mm QFN or TSSOP Packages

General Description

The PL613-01 is an advanced triple PLL design based on Microchip's PicoPLL™, the world's smallest programmable clock, technology. This advanced technology allows the eight output PL613-01 to fit in to a small 3 mm x 3 mm QFN or TSSOP package for high performance, low-power, low-cost applications. Besides its small form factor and 8 outputs that can reduce overall system costs, the PL613-01 offers superior phase noise, jitter and power consumption performance.

The power down feature of PL613-01, when activated, allows the IC to consume less than 10 µA of power, while its CSEL[0:1] allows switching between up to four pre-programmed configurations. The FSELX, on the other hand, allows frequency switching of two outputs (CLK1 and CLK2) on a single clock pin (CLK2).

Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage Range (V_{DD}) ..... –0.5V to +4.6V
Input Voltage Range (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Output Voltage Range (V_{OUT}) ..... –0.5V to V_{DD} + 0.5V
Data Retention at +85°C ..... 10 Years

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

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TABLE 1-1: AC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Crystal Input Frequency	X_{IN}	10	—	40	MHz	Fundamental Crystal
Input Frequency	F_{IN}	10	—	200	MHz	at V_{DD} = 3.3V, ±10%
		10	—	166	MHz	at V_{DD} = 2.5V, ±10%
		10	—	110	MHz	at V_{DD} = 1.8V, ±10%
Input Signal Amplitude	—	0.8	—	V_{DD}	V_{PP}	Internally AC-Coupled
Output Frequency	—	1	—	200	MHz	at V_{DD} = 3.3V, ±10% (High Drive)
		1	—	166	MHz	at V_{DD} = 2.5V, ±10% (High Drive)
		1	—	110	MHz	at V_{DD} = 1.8V, ±10% (High Drive)
Settling Time	—	—	—	2	ms	At power-up (V_{DD} ≥ 90% of operating V_{DD})
Output Enable Time	—	—	—	500	ns	OE function; T_A = 25°C, 15 pF load. Add one clock period to this measurement for a usable clock output.
		—	—	2	ms	PDB function; T_A = 25°C, 15 pF load.
V_{DD} Sensitivity	—	–2	—	2	ppm	Frequency vs. V_{DD}, ±10%
Output Rise Time	—	—	1.2	1.7	ns	15 pF load, 10/90% V_{DD}, High Drive, 3.3V
Output Fall Time	—	—	1.2	1.7	ns	15 pF load, 10/90% V_{DD}, High Drive, 3.3V
Duty Cycle	—	45	50	55	%	PLL-driven output, @ V_{DD}/2, 15 pF load, High Drive, over entire frequency range
Period Jitter (Note 1) (10,000 Samples)	—	—	300	—	ps	Configuration-dependent, with capacitive decoupling between V_{DD} and GND

Note 1: Jitter performance depends on the programming parameters.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current (V_{DD} = 3.3V)	I_{DD}	—	17	23	mA	All 8 outputs @ 20 MHz No load
Supply Current (V_{DD} = 2.5V)	I_{DD}	—	13.5	18	mA	All 8 outputs @ 20 MHz No load
Supply Current (V_{DD} = 1.8V)	I_{DD}	—	9.5	13	mA	All 8 outputs @ 20 MHz No load
Supply Current	I_{DD}	—	10	—	µA	When PDB = 0
Operating Voltage	V_{DD}	2.97	3.3	3.63	V	Configured for 3.3V Operation
		2.25	2.5	2.75	V	Configured for 2.5V Operation
		1.62	1.8	1.98	V	Configured for 1.8V Operation
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = +4 mA, Standard Drive, 3.3V

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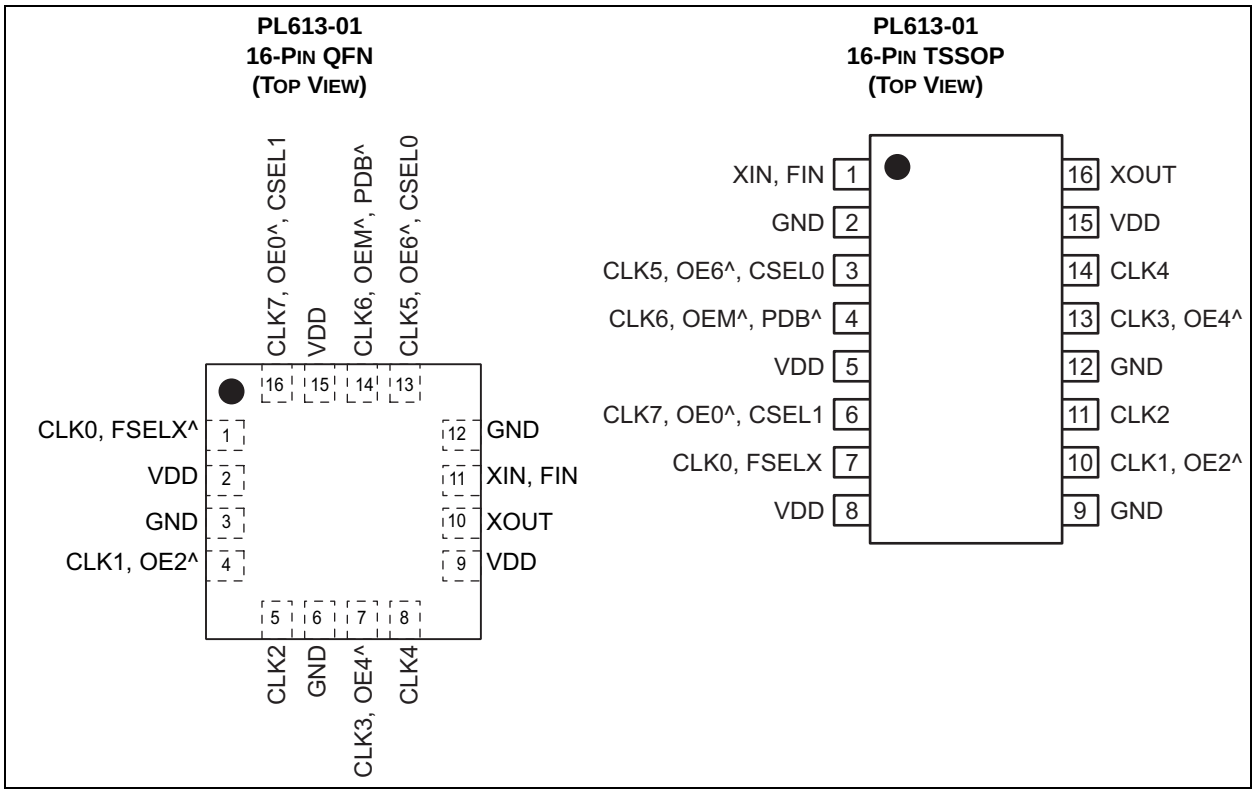
2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

Package Types



Note 1: ^ denotes internal pull-up.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number QFN-16	Pin Number TSSOP-16	Pin Name	Pin Type (Note 1)	Description
1	7	CLK0, FSELX	B	Programmable clock (CLK0) output or CLK2 frequency switching (FSELX) input.
3, 6, 12	2, 9, 12	GND	P	Ground connection.
2, 9, 15	5, 8, 15	VDD	P	V_{DD} connection.
4	10	CLK1, OE2	B	Programmable clock (CLK1) output or Output Enable (OE) input for CLK2.
5	11	CLK2	O	Programmable clock (CLK2) output.
7	13	CLK3, OE4	B	Programmable clock (CLK3) output or Output Enable (OE) input for CLK4.
8	14	CLK4	O	Programmable clock (CLK4) output.
10	16	XOUT	O	Crystal output pin. Do not connect when using FIN.
11	1	XIN, FIN	I	Crystal or reference clock input.
13	3	CLK5, OE6, CSEL0	B	Programmable clock (CLK5) output or Output Enable (OE) input for CLK6 or configuration switching input.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number QFN-16	Pin Number TSSOP-16	Pin Name	Pin Type (Note 1)	Description
14	4	CLK6, OEM, PDB	B	Programmable clock (CLK6) output or Output Enable master (OEM) all clock outputs or power down mode (PDB) input.
16	6	CLK7, OE0, CSEL1	B	Programmable clock (CLK7) output or Output Enable (OE) input for CLK0 or configuration switching input.

Note 1: All bidirectional buffers (I/Os) incorporate an internal 60 kΩ pull-up resistor when used as an input, except when PDB mode is used. In configurations that use PDB, the PDB pin will have a 10 MΩ pull-up resistor.

TABLE 2-2: KEY PROGRAMMING PARAMETERS

CLK[0:7] Output Frequency	Output Drive Strength	Programmable Input/Output
CLK[0,3,6]: F_{VCOx} / (P*(1,2,4,8)), F_{REF}, or F_{REF} / (P*(1,2,4,8)) **CLK[1,4,7]:** F_{VCOx} / P **CLK[2,5]:** F_{VCOx} / P, F_{REF}, or F_{REF} / P Where $F_{VCOx} = F_{REF} * M / R$ M = 11 bit R = 8 bit P = 5 bit (odd/even divider)	Each output has three optional drive strengths to choose from: • Low: 4 mA • Standard: 8 mA (default) • High: 16 mA	Most pins are multi-function I/Os. In addition to CLK, they can be configured to perform as the following: • OE[0,2,4,6]: Output Enable for Individual I/Os. • OEM: Master OE Controlling All Outputs. • CSEL[0:1]: Device Configuration Switching. • FSELX: CLK2 Frequency Switching. • PDB: Power Down. • CLK[0:8]: Output. • HiZ or Active-Low Disabled State.

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3.0 FUNCTIONAL DESCRIPTION

The PL613-01 is a highly featured, very flexible, advanced triple-PLL design for high performance, low-power applications. The device accepts a low-cost fundamental crystal input of 10 MHz to 40 MHz or a reference clock input of 10 MHz to 200 MHz and is capable of producing eight distinct output frequencies up to 200 MHz. All three PLLs are fully programmable, with a total of five, 5-bit post-VCO, odd/even 'P-counter' dividers with an additional 1, 2, 4, or 8 'Post P-counter' dividers that easily generate the most demanding frequencies. The outputs can be programmed to deliver the generated frequencies from the PLLs or the reference input. Each bidirectional feature pin (I/O) on the PL613-01 incorporates a 60 kΩ pull-up resistor and can be configured to perform various functions. Usage of various design features of these products is mentioned in the following paragraphs.

3.1 PLL Programming

The three PLLs in PL613-01 are fully programmable. Each PLL is equipped with an 8-bit input frequency divider (R-Counter) and an 11-bit VCO frequency feedback loop (M-Counter) divider. The three PLL outputs are transferred to five 5-bit post-VCO, odd/even dividers (P-Counter), as shown in the Block Diagram. In addition, there are three optional (÷1, ÷2, ÷4, or ÷8) post P-Counter dividers that can further divide the VCO frequency. In general, the PLL output frequency is determined by the following formula:

EQUATION 3-1:

$$F_{OUT} = (F_{REF} \times M)/(R \times P)$$

For output calculations, please note that 'P' includes the P-Counter bits plus the additional optional dividers (÷1, ÷2, ÷4, or ÷8), if used.

3.2 CLKx (Clock Outputs)

There are a maximum of eight outputs available on the PL613-01. Clock output frequencies can be configured as follows:

- CLK[0,3,6]
  - F_{VCOx} / (P*(1, 2, 4, 8))
  - F_{REF} (Crystal or Reference Clock frequency)
  - F_{REF} / (P*(1,2,4,8))
- CLK[1, 7]
  - F_{VCOx} / P
- CLK[2, 4, 5]
  - F_{VCOx} / P
  - F_{REF}
  - F_{REF} / P

Each output can be programmed with a 4 mA, 8 mA, or 16 mA drive strength. The maximum output frequency is 200 MHz at 3.3V, 166 MHz at 2.5V, or 110 MHz at 1.8V.

3.3 OE (Output Enable)

Four pins can be configured as OE inputs for controlling individual clock outputs, as show in the table below.

OEx	Controls Output on CLK#
OE0	CLK0
OE2	CLK2
OE4	CLK4
OE6	CLK6

Typical enable time is <500 ns plus one clock period.

The OE feature can be programmed to allow the output to float (HiZ) or to operate in active-low mode. The programming control for individual OEs is show below.

OE Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (default)	On	On	HiZ
	1	On	On	Active 0
1	Normal Operation (default)			

3.4 OEM (Master Output Enable)

One pin can be configured to be a single Master OE (OEM) input pin that controls all the outputs of the PL613-01. In addition, the state of the disabled outputs can be programmed to float (HiZ) or to operate in active-low mode. The OEM function operates on the following logic:

OE Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (default)	On	On	HiZ
	1	On	On	Active 0
1	Normal Operation (default)			

Typical enable time is <500 ns plus one clock period.

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4.0 LAYOUT RECOMMENDATIONS

The following guidelines are designed to help create a performance-optimized PCB design.

4.1 Signal Integrity and Termination Considerations

- Keep traces short.
- Trace = Inductor. With capacitive loads, this creates ringing.
- Long trace = long transmission line. Without proper termination, this causes reflections that look like ringing.
- Design long traces (greater than one inch) as striplines or microstrips with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

4.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply.
- Multiple V_{DD} pins should be decoupled separately for best performance.
- The addition of resistors in series with V_{DD} can help prevent noise from other board sources.
  - Traditionally, ferrite beads are used for this purpose, but with the PL613-01 the results are better when using resistors.

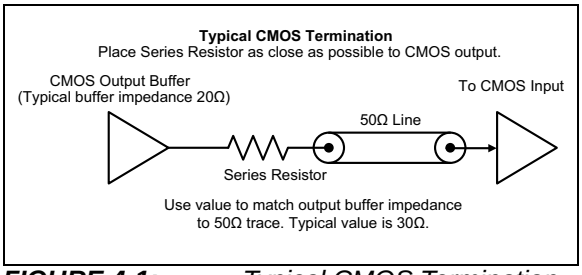

FIGURE 4-1: *Typical CMOS Termination.*

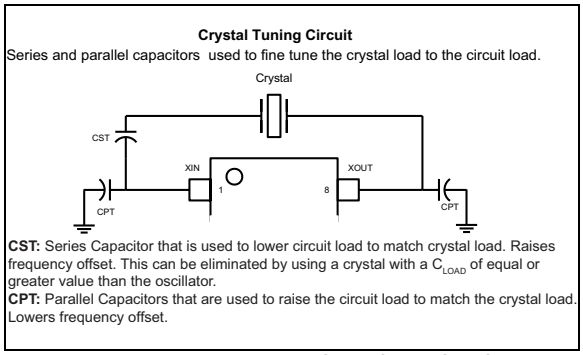

FIGURE 4-2: *Crystal Tuning Circuit.*

4.3 Layout Example

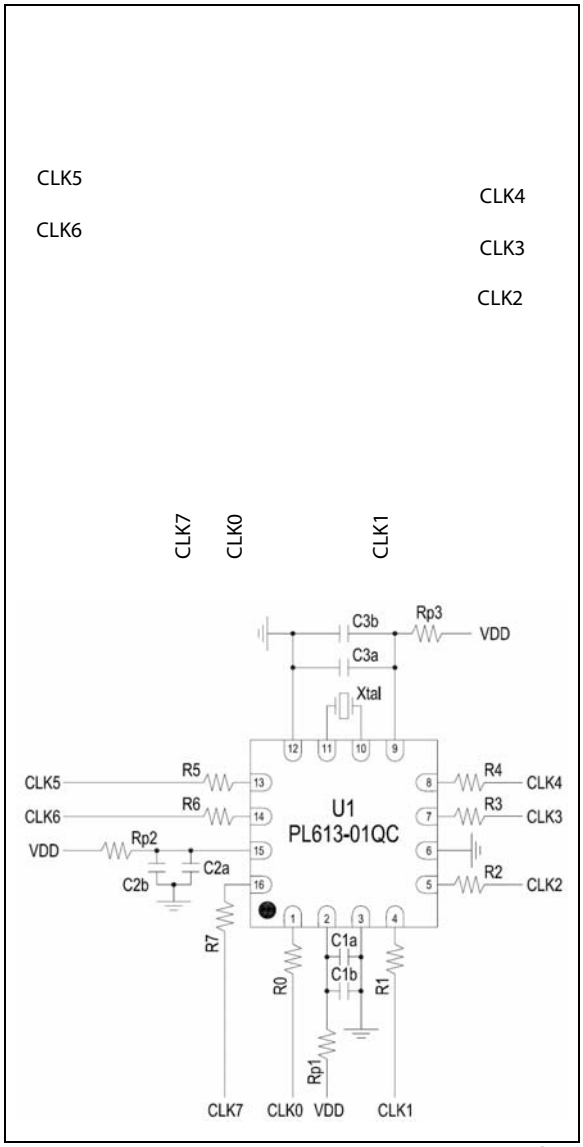

FIGURE 4-3: *PL613-01 Layout Example.*

U1 = PL613-01 in QFN-16L. In this example, all eight outputs are used.

C1a, C2a, C3a = 0.1 µF and C1b, C2b, C3b = 1 µF for power supply decoupling. The vias connected to the capacitors go to the ground plane inside the PCB.

Rp1, Rp2, Rp3 = 10Ω for power supply filtering. The power supply filter is a first order low pass filter with –3 dB at 30 kHz. It is important that the frequencies of the loop bandwidth of the PLLs are filtered properly. The loop bandwidth of the PLLs is in the range of 100 kHz to 1 MHz depending upon the programmed configuration. The vias connected to Rp1, Rp2, and Rp3 go to the V_{DD} plane inside the PCB.

R0 ~ R7 = 30Ω for matching CLK0 ~ CLK7 outputs to the PCB trace impedance. Place the resistors as close as possible to the IC pins and design the traces to the

target clock inputs as transmission lines (microstrip or stripline) for the best signal integrity and the lowest EMI.

When using ferrite beads instead of Rp1, Rp2, or Rp3, make sure the resonance frequency of the bead with the decoupling capacitors is below 50 kHz so as not to interfere with the PLL loop bandwidth. This requirement is difficult to fulfill, so it is recommended to use the resistors Rp1, Rp2, and Rp3 for power supply filtering.

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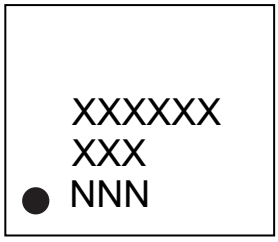
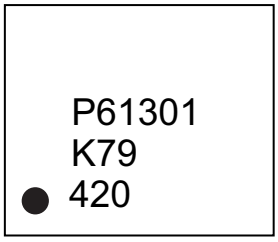
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

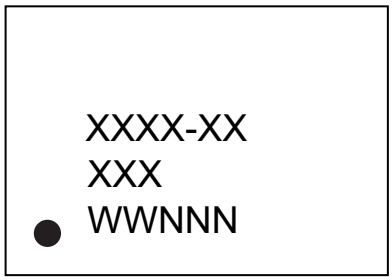
16-Pin QFN*



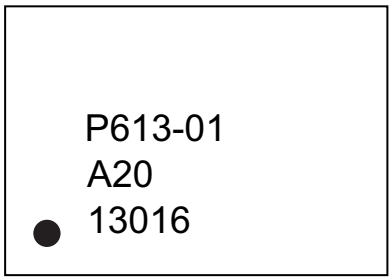
Example



16-Pin TSSOP*



Example

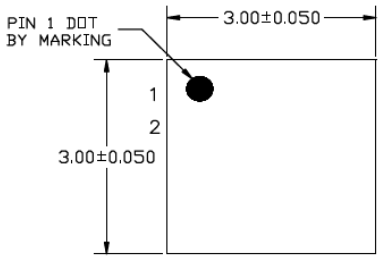


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

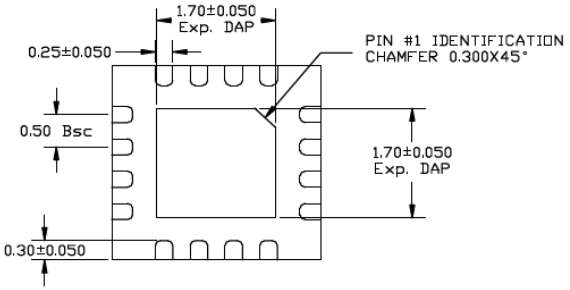
16-Lead QFN Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

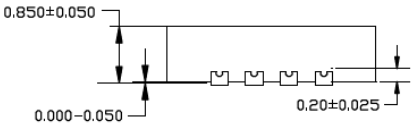
DRAWING #	QFN33-16LD-PL-3	**UNIT**	MM
Lead Frame	NiPdAu	**Lead Finish**	NiPdAu



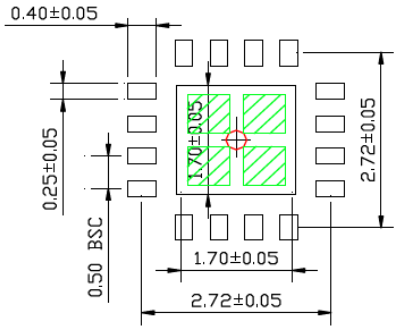
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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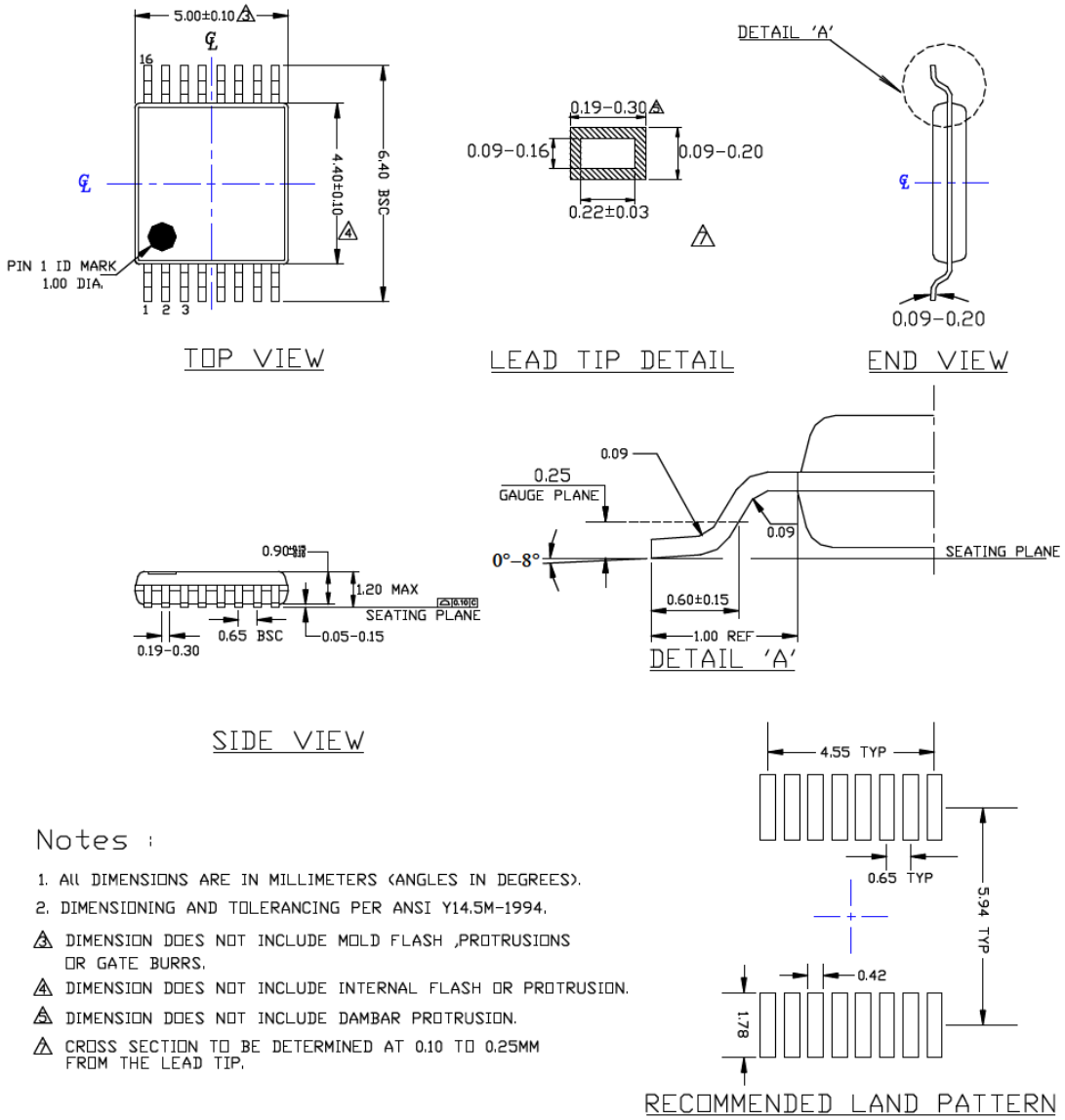
16-Lead TSSOP Package Outline and Recommended Land Pattern

TITLE
16 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-16LD-PL-1	UNIT	MM



Notes :

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
6. CROSS SECTION TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Micrel document PL613-01 to Microchip data sheet DS20005650A.
- Minor text changes throughout.
- Discontinued SSOP package offering.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	—	XXX	X	X	—	XX
Device		ID Code	Package	Temperature		Media Type

Device:	PL613-01:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC
ID Code:	XXX =	Unique 3-digit code assigned at programming time
Package:	O =	16-Lead TSSOP
	Q =	16-Lead QFN
Temperature:	C =	0°C to +70°C (Commercial)
	I =	–40°C to +85°C (Industrial)
Media Type:	blank=	Tube
	TR =	Tape & Reel

Examples:

a) PL613-01-XXXOC:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead TSSOP, Commercial Temperature Range, Tube
b) PL613-01-XXXOI-TR:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead TSSOP, Industrial Temperature Range, Tape & Reel
c) PL613-01-XXXQC-TR:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead QFN, Commercial Temperature Range, Tape & Reel
d) PL613-01-XXXQI:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead QFN, Industrial Temperature Range, Tube
e) PL613-01-XXXOC-TR:	1.8V to 3.3V, PicoPLL, 3-PLL, 200 MHz, 8 Output Clock IC 3-Digit ID Code, 16-Lead TSSOP, Commercial Temperature Range, Tape & Reel

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NOTES:

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