



General

The AK1594 is a low power consumption transmitter IC that supports Bluetooth® 4.2. The AK1594 is a simplest Bluetooth® Low Energy transmitter without the need for a microcontroller, providing advertising data in the on-chip EEPROM.

Features

- Single Chip Bluetooth® Low Energy Transmitter
 - Only the AK1594 and a few passive components are required to complete Bluetooth® Low Energy advertising transmission function.
- Microcontroller-less(MCU-less)
 - Bluetooth® Low Energy advertising transmissions can be broadcasted using the AK1594's on-chip EEPROM data. This MCU-less architecture eases system design without a complicated development environment.
- Functional Switches
 - 4-hardware switches works as on-off, interval and power controller for advertising transmission.
- Programmable Output Power
 - Support wide range output power from -32dBm to +6dBm.
- Data whitening and CRC
 - Build-in data whitening feature and CRC that are compliant with Bluetooth® Low Energy.
 - Support GFSK(1Mbps)
- Security
 - AES-128 Hardware Encryption
- Package
 - 28-pin QFN (4.0mm x 4.0mm x 0.70mm, 0.4mm pitch)

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2. Notation

The following notations are used for specific signals and register names:

- [Name]: Internal signal name
- <Name>: EEPROM address name
- {Name}: EEPROM bit name

The numerical values are expressed as follows

- 0x63A: Hexadecimal numbers
- 0d1594 or 123: Decimal numbers
- 0b11000111010: Binary numbers

Terms and acronyms

- AdvA Advertiser’s Device Address
- AES Advanced Encryption Standard
- BLE Bluetooth® Low Energy
- CRC Cyclic Redundancy Check
- EEPROM Electrically Erasable Programmable Read-Only Memory
- GFSK Gaussian Frequency Shift Keying
- IRK Identity Resolving Key
- LDO Low Drop Out
- LSB Least Significant Bit
- MCU Micro Controller Unit
- MSB Most Significant Bit
- PDU Protocol Data Unit
- PLL Phase Locked Loop
- POR Power On Reset
- PPM Part Per Million
- RF Radio Frequency
- SPI Serial Peripheral Interface
- SW Switch
- Tx Transmit

These 3 words mean data packet of Bluetooth® Low Energy Advertising channel. The data format is shown in Figure 1.

- Payload
- AdvA
- AdvData

Preamble	Access Address	PDU				CRC
		Header	Payload			
			AdvA	AdvData		
1octet	4octets	2octets	6octets	0 to 31octets	3octets	

Figure 1 Bluetooth® Low Energy Advertising Channel packet format

3. Block Diagram

Power supply and ground pins are not included.

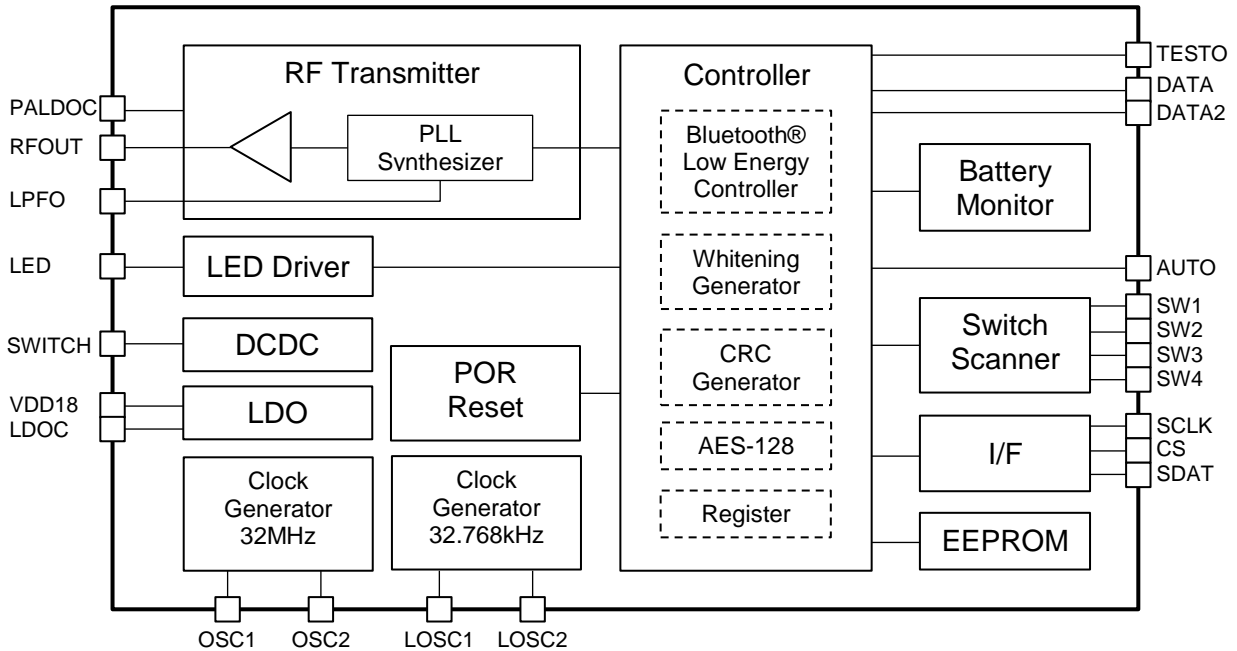


Figure 2 Overall Block Diagram

- RF Transmitter
This block outputs RF signal after GFSK modulation.
- Switch Scanner
This block detects switch actions.
- EEPROM
EEPROM holds AK1594 setting and TX data.
- Register
EEPROM read data is stored temporary to the register. It's not accessible to users.
- Battery Monitor
This block monitoring VDD voltage
- LED Driver
This block lights LED.

4. Pin / Function

<The meaning of abbreviations used in the "I/O" column of the pin table is shown below>

AI: Analog input pin AO: Analog output pin AIO: Analog I/O pin DI: Digital input pin	DO: Digital output pin DIO: Digital I/O pin P: Power supply pin G: Ground pin
---	--

Pin No.	Pin name	I/O	Pin Functions	State after POR	Max. load capacitance	pullup/pulldown	Remarks
TX Section							
22	RFOUT	AO	RF signal Output				
23	PALDOC	AO	Connection for an external TX output adjustment inductor to RFOUT pin.				
External Interface							
6	SW1	DI	Switch 1 Input (Start trigger signal input for burst transmission)				Note1
9	SW2	DI	Switch 2 Input (Stop trigger signal input for burst transmission)				Note1
16	SW3	DI	Switch 3 Input (Transmission power control signal input)				Note1
17	SW4(RXD)	DI	Switch 4 Input (Advertising interval control signal input) RXD : Bluetooth® Certification test input pin				Note1
5	LED	AO	LED Output (Leave this pin open if a LED is not used)				
19	DATA	DI	This pin is not use. Tie to ground				
20	DATA2	DI	This pin is not use. Tie to ground				
18	TESTO(TXD)	DO	For AKM Test (Leave this pin open) TXD : Bluetooth® Certification test output pin	L	15pF		
Common Section							
24	LDOC	AO	Connection for an external capacitor for LDO.				
7	OSC1	AI	32MHz Crystal oscillator				
8	OSC2	AO	32MHz Crystal oscillator				
15	LOSC1	AI	32.768kHz Crystal oscillator				
14	LOSC2	AO	32.768kHz Crystal oscillator				
12	CS	DI	EEPROM access mode when CS pin="H" Normal mode when CS pin = "L"			Pull down	
11	SCLK	DI	EEPROM access clock input when CS pin="H" Normal mode when CS pin = "L"			Pull down	
13	SDAT	DIO	EEPROM access data in/output when CS pin="H" Normal mode when CS pin = "L"		15pF	Pull up	Input mode after POR
4	LPFO	AIO	Connection for an external capacitor for the loop filter				
28	SWITCH	AO	DCDC converter output				
26	VDD18	AI	Power supply Connect to SWITCH pin via an external inductor.				

Pin No.	Pin name	I/O	Pin Functions	State after POR	Max. load capacitance	pullup/pulldown	Remarks
25	AUTO	DI	Selection of AUTO mode. AUTO pin = "L", Switch action transmission mode AUTO pin = "H", Automatic transmission mode Do not leave this pin open.				
Power supply							
2	AVDD	P	Power supply				
1	DCVDD	P	Power supply for DCDC converter				
21	RFVSS	G	Ground for RFAMP				
3,10	VSS	G	Ground				
27	DCVSS	G	Ground for DCDC converter				

Note 1 Must be connected to VDD or pull up if the pin is unused.

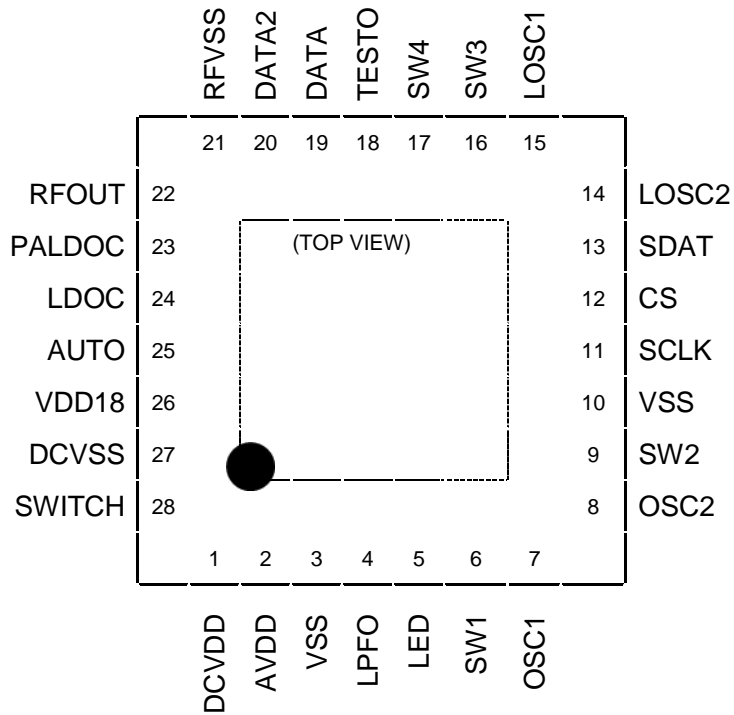


Figure 3 Pin configurations

5. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	-0.3	6.0	V	Note 1
Ground Level	VSS	0	0	V	
Input Voltage	Vin	VSS-0.3	VDD+0.3	V	Note 1
Input Current	Iin	-50	+50	mA	
Output Current	Iout	-50	+50	mA	
Storage Temperature	Tstg	-55	+125	°C	

Note 1 All voltages with respect to the ground level as 0V

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

6. Recommended Operating Range

The specifications are applicable within operating range (supply voltage/operating temperature) specified below.

Parameter	Symbol	Voltage	Ground pin	Remarks
Ground pin	VSS	0V	VSS, DCVSS, RFVSS	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD	2.0	3.0	3.7	V	AVDD, DCVDD pin Note 1,2

Note 1 When VDD voltage falls below 2V and the AK1594 is needed to be power-up, please reset the AK1594. Performance is not guaranteed for power-on without the AK1594 reset.

Note 2 This specification in case of {POWR_MODE[1]} = "0b0", Minimum value is 2.3V in case of {POWR_MODE[1]} = "0b1"

Note 3 All voltages with respect to the ground level as 0V

Note 4 AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

7. Electric Characteristics

The specifications are applicable within recommended operating range (supply voltage/operating temperature), using the Test schematic.

7.1. Characteristics of RF output

Parameter		Min.	Typ.	Max.	Unit	Remarks
Channel Frequency Note 1	Frequency1		2402		MHz	
	Frequency2		2426		MHz	
	Frequency3		2480		MHz	
Output Power	Power setting 1 for high power mode		+6		dBm	{POWRD[4:0]} = "0d31" {POWR_MODE[1]} = "1"
	Power setting 2 for normal power mode		0		dBm	{POWRD[4:0]} = "0d28" {POWR_MODE[1:0]}="0b00"
	Power setting 3 for normal power mode		-3		dBm	{POWRD[4:0]} = "0d16" {POWR_MODE[1:0]}="0b00"
	Power setting 4 for normal power mode		-32		dBm	{POWRD[4:0]} = "0d0" {POWR_MODE[1:0]}="0b00"
Adjustable step for output power		0			dB	Note 3
GFSK Note2	Average frequency deviation for 00001111 sequence(Δf)	± 225	± 250	± 275	kHz	
	Ratio average Frequency deviation (10101010 sequence / 00001111 sequence)	80			%	
	Minimum frequency deviation(Δf min)	± 185			kHz	
	Bit rate		1.0		Mbps	
	BT(Bandwidth-Time)		0.5			
	Modulation index(m)	0.45	0.50	0.55		$m=(2* \Delta f) / (\text{bit rate})$
	Spurious			-20 -30	dBm dBm	1MHzBW @2MHz offset 1MHzBW @>3MHz offset

Note 1 Channel frequency means center frequency of modulation.

Note 2 GFSK characteristics based on Bluetooth® Low Energy test specification(RF-PHY.TS.4.2.3)

Note 3 Guaranteed by design (Not tested)

7.2. Current Consumption

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Full Power down	SIDD1	SW pins:VDD, LED:open, Note 1		15	100	nA
TX ON	IDD1a	LED pin : open, Note 2		5	8	mA
	IDD1b	LED pin : open, Note 3		5	13	mA
	IDD1_2a	LED pin : open, Note 4		11	18	mA
	IDD1_2b	LED pin : open, Note 5		11	30	mA
Sleep	IDD2a	LED pin : open, Note 6		0.9	1.2	uA
	IDD2b	LED pin : open, Note 7		0.9	1.5	uA
LED Current (Drivability)	ILED1	LED pin voltage : 1.6V(typ) Note1 Note8		3.0	5.0	mA
	ILED2	LED pin voltage : 1.6V(typ) Note1 Note9		1.0	2.0	mA

Note 1 VDD=3.0V, Room Temperature (25 °C.).

Note 2 VDD=3.0V, Room Temperature (25 °C.),

TX_ch:2426MHz, RFOUT: 0dBm(typ.), {POWRD[4:0]}=0d28, {POWR_MODE[1:0]}="0b0"

Note 3 VDD=VSLEEPN to 3.7V, Temperature range = -40 to 85 °C,

TX_ch:2426MHz, RFOUT: 0dBm(typ.), {POWRD[4:0]}="0d28", {POWR_MODE[1:0]}="0b0"

Note 4 VDD=3.0V, Room Temperature (25 °C.),

TX_ch:2426MHz, RFOUT: +6dBm(typ.), {POWRD[4:0]}="0d31", {POWR_MODE[1]}="0b1"

Note 5 VDD=VSLEEPH to 3.7V, Temperature range = -40 to 85 °C,

TX_ch:2426MHz, RFOUT:+6dBm(typ.), {POWRD[4:0]}="0d31", {POWR_MODE[1]}="0b1"

Note 6 VDD=3.0V, Room Temperature (25 °C.), RFOUT: off, LOSC: active.

Note 7 VDD=VSLEEPN to 3.7V, Temperature range = -40 to 85deg, RFOUT: off, LOSC: active.

Note 8 {I_LED} ="0b1"

Note 9 {I_LED} ="0b0"

7.3. Characteristics of Battery monitor

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Detect Voltage1	VALERT		2.3		V	For LED
Release Voltage1	VRELEASE		2.46		V	For LED release voltage
Detect Voltage2N	VSLEEPN		2.05		V	For full power down Normal power mode
Detect Voltage2H Note 1	VSLEEPH		2.3		V	For full power down High power mode

Note 1 When High power mode {POWR_MODE[1:0]} is "0b11" or "0b10", the AK1594 goes into full power down. LED pin function does not work. Refer 10.7 Battery monitor.

Note 2 VSLEEPN release voltage is VSLEEPN

Note 3 VSLEEPH release voltage is VRELEASE

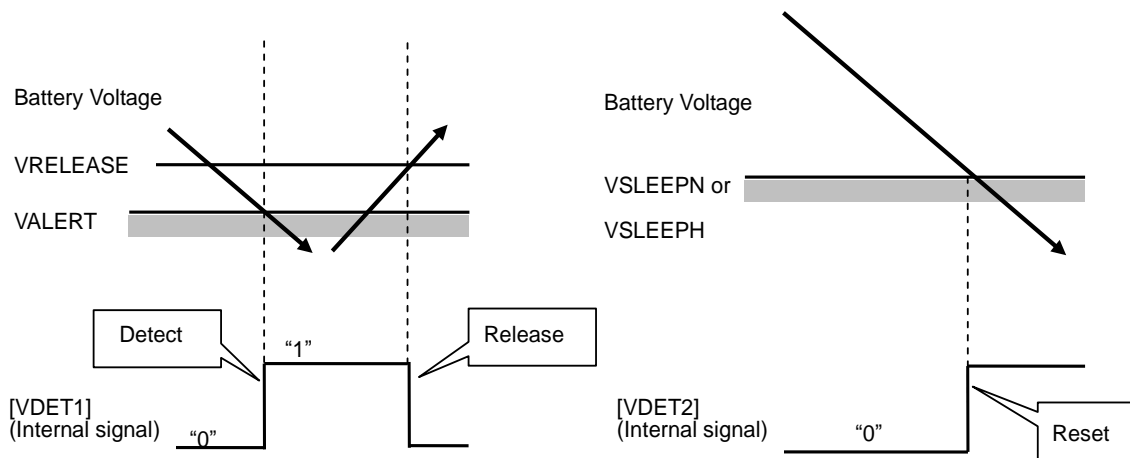


Figure 4 Battery monitor function

7.4. Characteristics of EEPROM

Parameter	Conditions	Min.	Typ.	Max.	Unit
Number of rewrite times Note1		100,000			times
Endurance Note1	Ta = 85°C	10			years

Note 1 Guaranteed by design (Not tested)

7.5. Characteristics of Crystal Oscillator 32MHz

Parameter	Min.	Typ.	Max.	Unit	Remarks
Oscillator frequency		32.000		MHz	
Frequency tolerance	-50		+50	ppm	
Stabilization time after startup			2	msec	Note1

Note 1 Guaranteed by design (Not tested)

7.6. Characteristics of Crystal Oscillator 32.768kHz

Parameter	Min.	Typ.	Max.	Unit	Remarks
Oscillator frequency		32.768		kHz	
Frequency tolerance	-500		+500	ppm	
Stabilization time after startup			1	sec	Note1

Note 1 Guaranteed by design (Not tested)

7.7. Characteristics of Power On Timing

Operating conditions for POR (Power On Reset) function.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Voltage of OFF state	Voff			0.05	V	Note1
Interval of under Voff	Tvoff	500			msec	Note1
Rising time	Tr			10	msec	Note1
Stabilized state VDD	VDDSTB	2.0		3.7	V	Note1

Note 1 Guaranteed by design (Not tested)

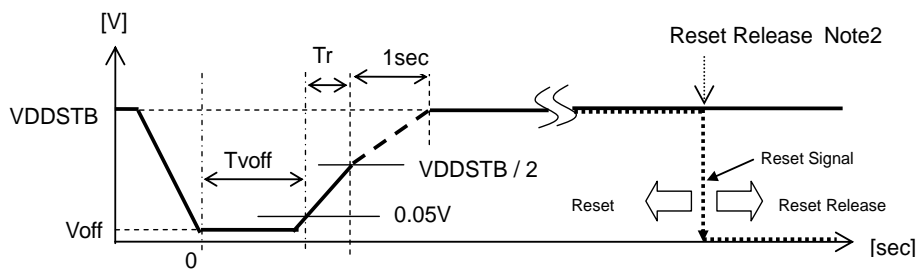


Figure 5 Power on timing

Note 2 Reset release timing is follows,
 AUTO pin = "H", the first rising edge of LOSC clock
 AUTO pin = "L", the falling edge of SW1 pin

7.8. Characteristics of Timer

Parameter	Min.	Typ.	Max.	Unit	Remarks
Tch_int		$(8 + \{PDULEN[5:0]\}) * 8 + 30$		μsec	
advInterval	0.10		10.24	sec	15 control bits which is programmed by EEPROM
advDelay	0		10	msec	Randomly generated 4 control bits.

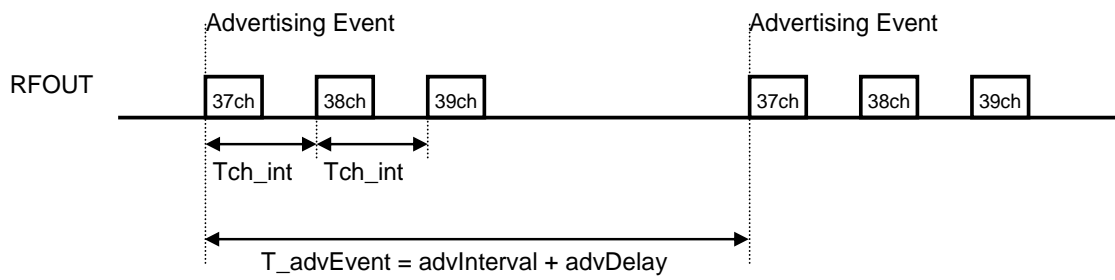


Figure 6 Interval of Advertising Event

8. Electric Characteristics of Digital Interface

The specifications are applicable within recommended operating range (supply voltage/operating temperature).

8.1. Digital DC Characteristics

Parameter	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	Vih	Note 1		0.8×VDD	-	-	V
Low level input voltage	Vil	Note 1		-	-	0.2×VDD	V
High level input current	Iih	Note 3	Vih = VDD	-10	-	+10	μA
Low level input current	Iil	Note 4	Vil = VSS	-10	-	+10	μA
High level output voltage	Voh	Note 2	Ioh = -100μA	0.8×VDD	-	-	V
Low level output voltage	Vol	Note 2	Iol = 100μA	-	-	0.2×VDD	V
Pull up	Rpu	Note 5		10	20	30	kohm
Pull down	Rpd	Note 6		15	30	45	kohm

Note 1 Digital input pins: SW1, SW2, SW3, SW4, CS, SCLK, SDAT, AUTO, DATA, DATA2 pins

Note 2 Digital output pins: SDAT, TESTO pins

Note 3 Digital input pins: SW1, SW2, SW3, SW4, SDAT, AUTO, DATA, DATA2 pins

Note 4 Digital input pins: SW1, SW2, SW3, SW4, CS, SCLK, AUTO, DATA, DATA2 pins

Note 5 Digital input pins: SDAT pin

Note 6 Digital input pins: CS, SCLK pins

8.2. Digital AC Characteristics

Switchover timing of digital AC characteristics are specified at 1/2VDD level unless otherwise noted.

8.2.1. Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCLK	tSKP	1000	-	-	nsec	
SCLK pulse width	tSKW	500	-	-	nsec	
CS high level to SCLK high level Delay	tCSS	100	-	-	nsec	
SCLK low level to CS low level Delay	tCSLW	5	-	-	msec	@Write access
	tCSL	100	-	-	nsec	@Read access
Setup time	tDIS	100	-	-	nsec	
Hold time	tDIH	100	-	-	nsec	
Transient time (rise)	tr			100	nsec	Note1
Transient time (fall)	tf			100	nsec	Note1
Output delay	tDLY	-	-	300	nsec	Output Load CL<15pF

Note 1 Guaranteed by design (Not tested)

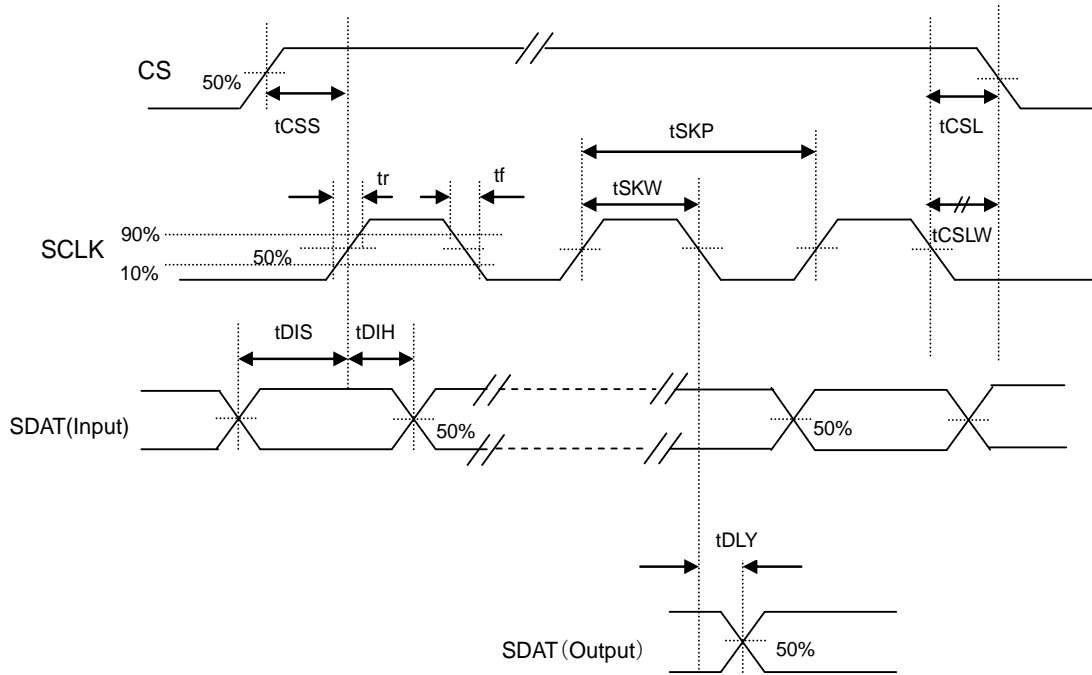
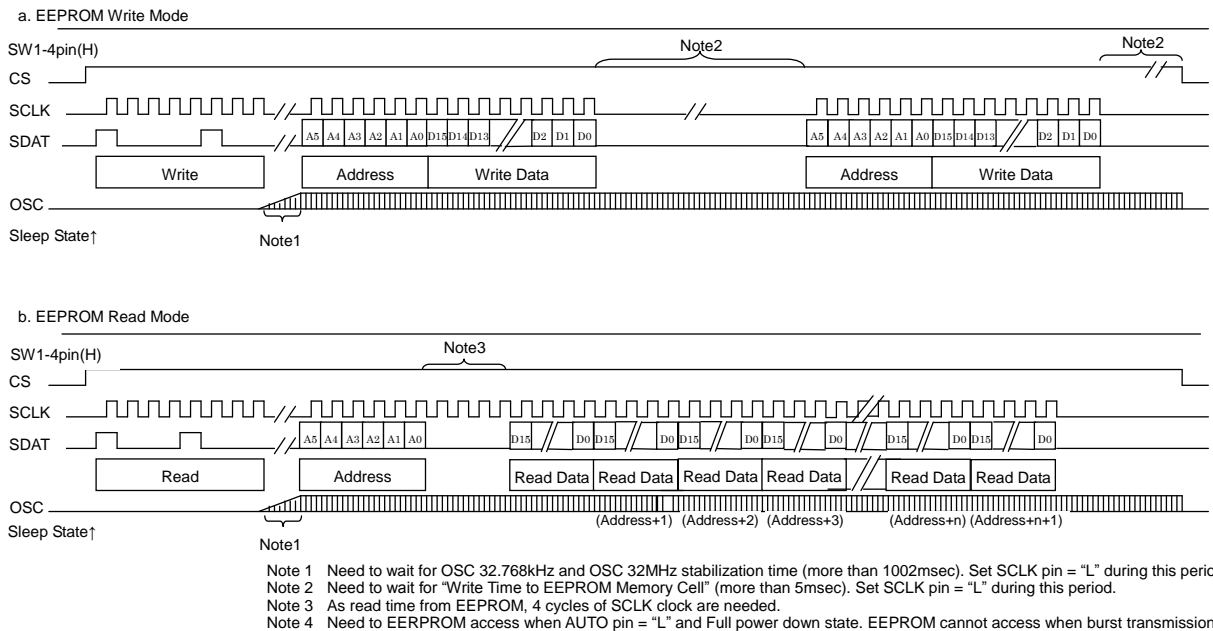


Figure 7 AC timing of serial interface

8.2.2. Timing chart of EEPROM ACCESS



Note 1 Need to wait for OSC 32.768kHz and OSC 32MHz stabilization time (more than 1002msec). Set SCLK pin = "L" during this period.
 Note 2 Need to wait for "Write Time to EEPROM Memory Cell" (more than 5msec). Set SCLK pin = "L" during this period.
 Note 3 As read time from EEPROM, 4 cycles of SCLK clock are needed.
 Note 4 Need to EEPROM access when AUTO pin = "L" and Full power down state. EEPROM cannot access when burst transmission.

Figure 8 Timing chart of EEPROM access

8.2.3. SW1 pin , SW2 pin, SW3 pin, SW4 pin timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low Pulse width	tSWL	25	-	-	msec	
High Pulse width	tSWH	25	-	-	msec	

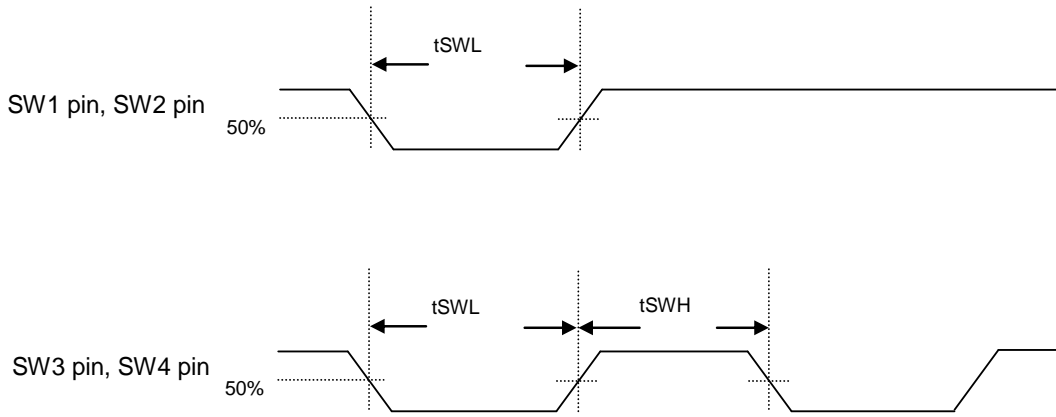


Figure 9 AC timing of Switch Pin

9. Operation State

9.1. State Description

The AK1594 has 5-state.

State	Description
Full Power Down	All blocks are powered down.
32.768kHz clock stabilization	The AK1594 is in stand-by state in order to stabilize 32.768KHz clock.
32MHz clock stabilization + Read EEPROM	The state that the AK1594 is reading EEPROM data during the 32MHz clock stabilization state.
Transmitter ON (TX ON)	RF transmissions followed by TX data generation from the EEPROM, PLL and RFAMP power up.
Sleep	Stand-by status for next advertising event after RF transmissions.

The term “burst transmission” means following 3-state transition.

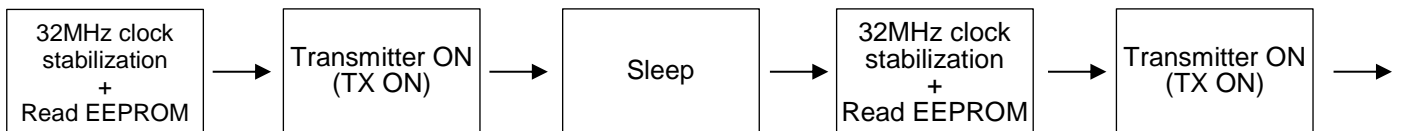


Figure 10 Burst transmission

10. Function Description

10.1. TX MODE

There are two transmission modes “Continuous Burst Mode” and “Configured TX Mode”.

Continuous Burst Mode: {MODE} = “0b0”

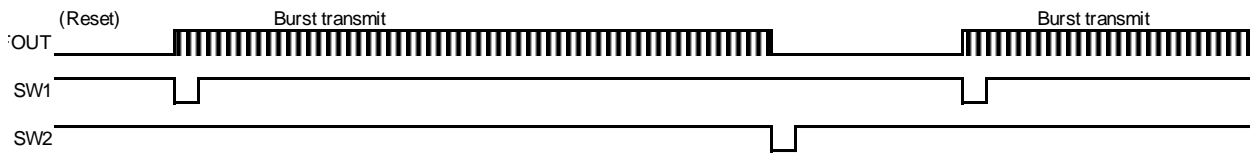
The AK1594 continues RF transmission until the AK1594 detects SW2 pin falling edge. SW2 pin falling edge valid only AUTO pin = “L” and {SW2_DIS} = “0b0”.

Configured TX Mode: {MODE} = “0b1”

The AK1594 automatically stops transmission and goes to power down status after configured number of transmission is attempted. The AK1594 can configure 1 to 5 transmissions that is set by {EVENTNUM [2:0]}

The AK1594 automatically stops transmission triggered on SW1 falling edge. After the AK1594 detects SW1 pin falling edge, the AK1594 does advertising transmission configured number of time (Note), and then goes into power down status.

Note: The AK1594 can configure 1 to 5 transmissions that is set by {EVENTNUM [2:0]}



note1: SW2 pin falling edge is valid when AUTO pin = “L” and {SW2_DIS} = “0b0”.

Figure 11 Continuous Burst Mode {MODE}= “0b0”

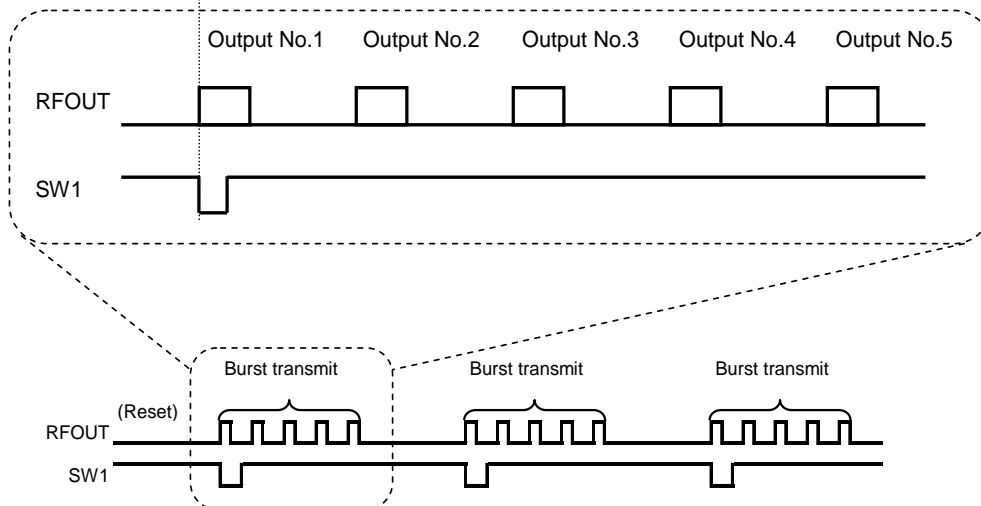


Figure 12 Configured TX Mode {MODE} = “0b1” and {EVENTNUM[2:0]} = “0d5”

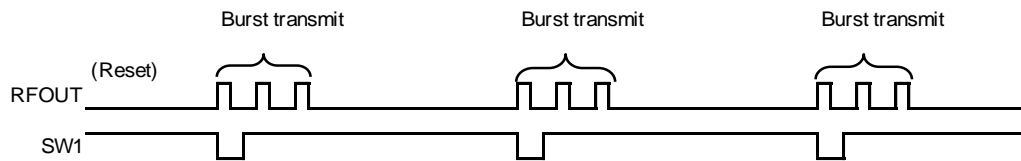


Figure 13 Configured TX Mode {MODE} = “0b1” and {EVENTNUM[2:0]} = “0d3”

10.2. POWER MODE

There are two mode based on output power, Normal Power Mode and High Power Mode by setting {POWR_MODE[1:0]}. Normal Power Mode has a benefit to save power. High Power Mode supports +6dBm (Typ.) output.

10.3. Auto Operation mode

When AUTO pin set to “High”, the AK1594 starts burst transmission automatically after the AK1594 powered-on. {MODE} register is “0b0” automatically when AUTO pin = “H”. {SW2_DIS} value is “0b1” automatically when AUTO pin = “H”.

AK1594 EEPROM cannot access when AUTO pin = “H”. AK1594 EEPROM access valid AUTO pin = “L” and “Full power down” state.

10.4. Switch Action

10.4.1. SW1 pin

The AK1594 starts burst transmission triggered on SW1 pin input falling edges.

10.4.2. SW2 pin

The AK1594 sets to full power down state triggered on SW2 pin input falling edges during burst transmission.

{SW2_DIS} enables or disables this function. This function is ignored when AUTO pin = "H".

10.4.3. SW1 and SW2 Simultaneous Control(Reset)

When SW1 pin and SW2 pin are status "low" simultaneously more than 2 seconds, the AK1594 resets internal digital blocks.

10.4.4. SW3 pin

SW3 provides two functions, Power Step Adjustment and High Power Switch.

- Power step adjustment ({SW3_FUNC} = "0b0")

TX power is changed every SW3 pin input triggered on falling edges. The AK1594 supports 6-state power transition (SW3State) and power step size is defined by {SW3STEP[2:0]}. The AK1594 LED function helps to determine which power state is configured monitoring number of LED blinks. When the AK1594 doesn't detect another SW3 falling edge for more than 4 seconds after the SW3 falling edge detection, the AK1594 finishes internal process and begins burst transmission with the latest power state setting.

- High power switch({SW3_FUNC} = "0b1")

The AK1594 switches transmission power to maximum by SW3 pin input. The maximum power is programmed by register ({POWER_MODE [1:0]} = "0b11", {POWRD [4:0]} = "31"). After maximum power is set by this function, the AK1594 transmission power will not go down from maximum power setting unless powered off (POR) or SW1 and SW2 simultaneous control.

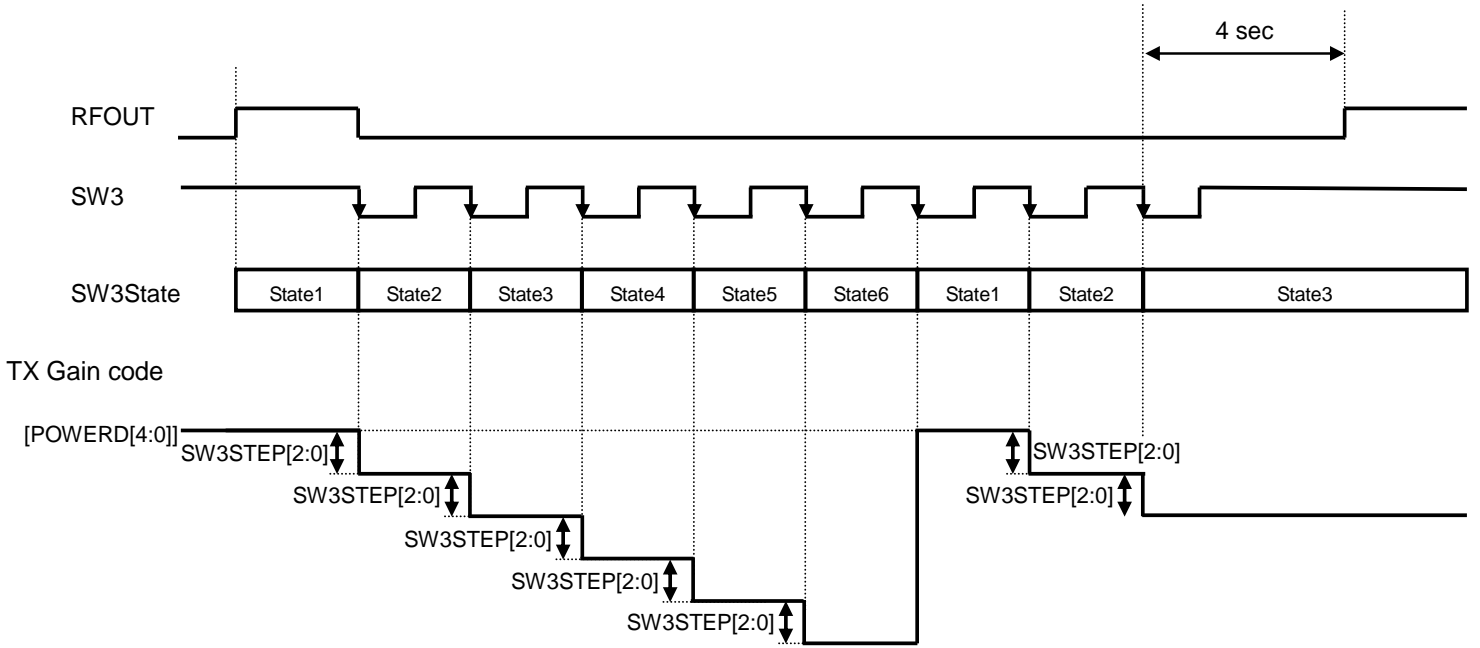


Figure 14 Transmission Power Step Adjustment

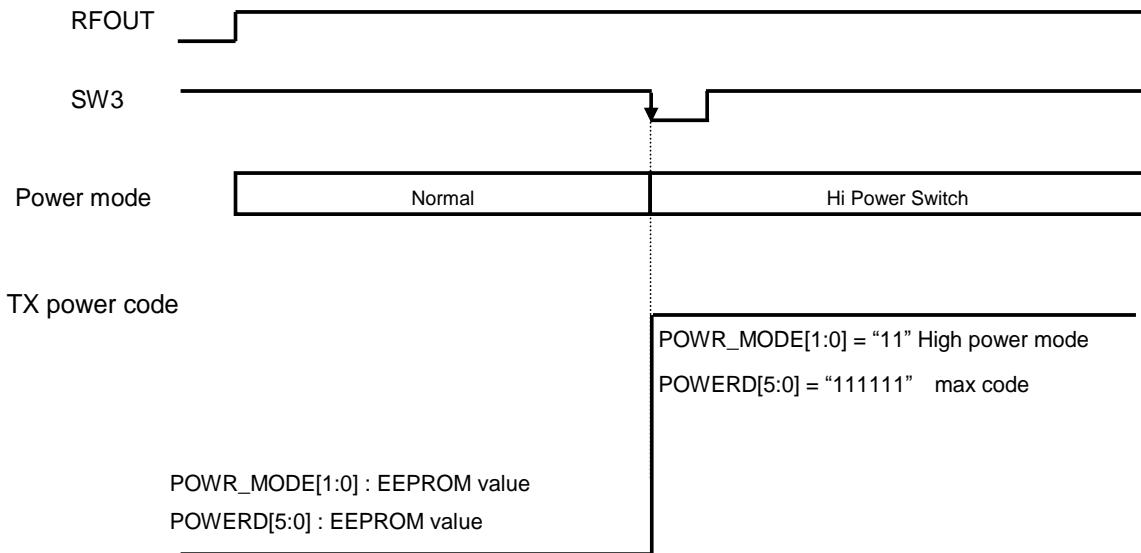


Figure 15 High power switch

10.4.5. SW4 pin

Advertising interval is changed every SW4 pin input triggered on falling edges. The AK1594 supports 6-state advertising interval (SW4State) and advertising interval length is defined by {SW4STEP[2:0]}. The AK1594 LED function helps to determine which advertising interval length is configured monitoring number of LED blinks. When the AK1594 doesn't detect another SW4 falling edge for more than 4 seconds after the SW4 falling edge detection, the AK1594 finishes internal process and begins burst transmission with the latest advertising interval length setting.

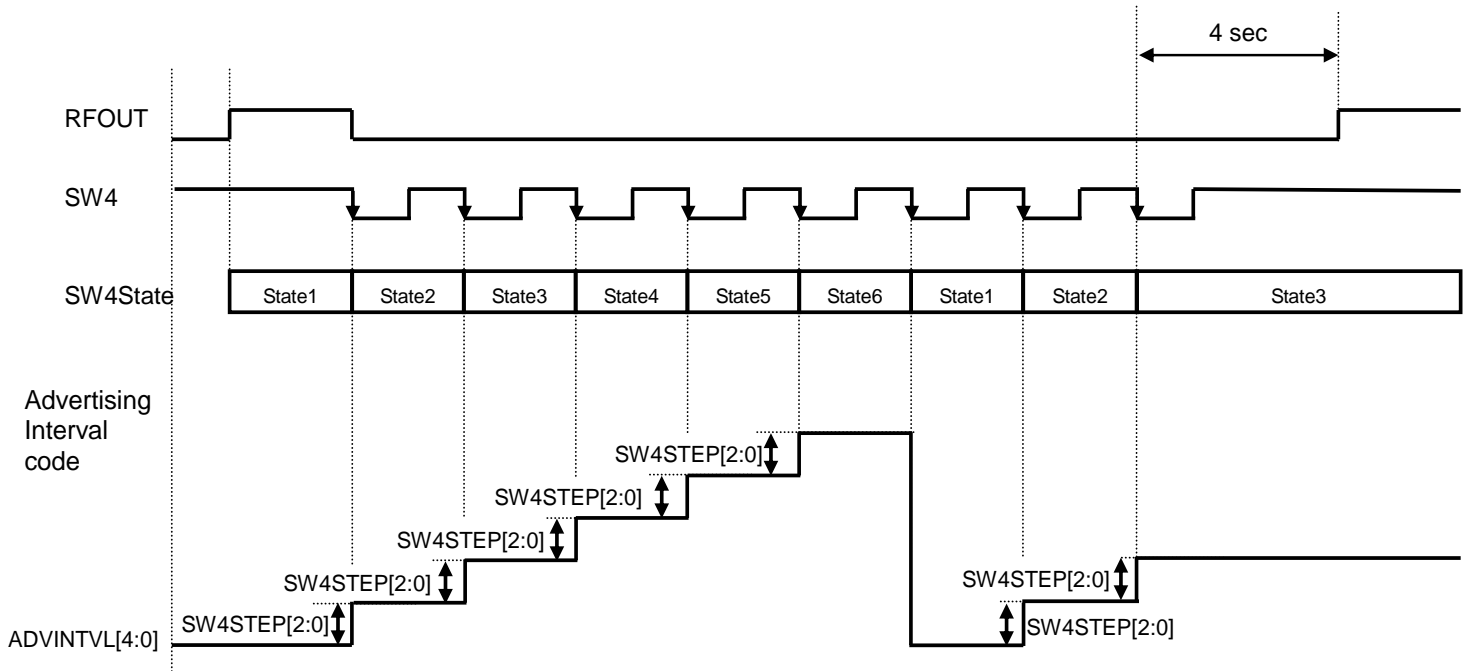


Figure 16 Advertising interval Step Adjustment

10.5. Reset

- In order to reset the AK1594 all functional blocks, following conditions are required.
- meet Power on Reset conditions; please refer 7.7 Characteristics of Power On Timing.
 - SW1 pin and SW2 pin are status "low" simultaneously more than 2 seconds; please refer 10.4.3.

10.6. Switch Detector

The AK1594 samples status of SW2, SW3 and SW4 falling edges by 7.8125ms cycle. When the AK1594 detects same status for the second time in a low, the switch status is updated at the next sampling timing. Refer Figure 18 Timing chart of SW2/SW3/SW4 Detector.

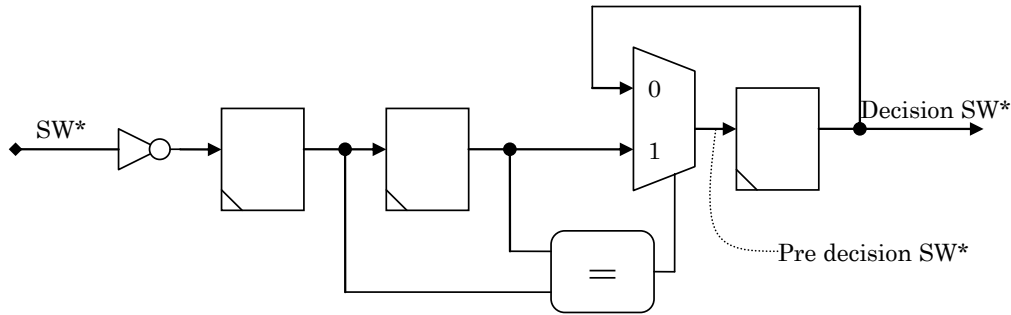


Figure 17 Circuit of SW2/SW3/SW4 Detector

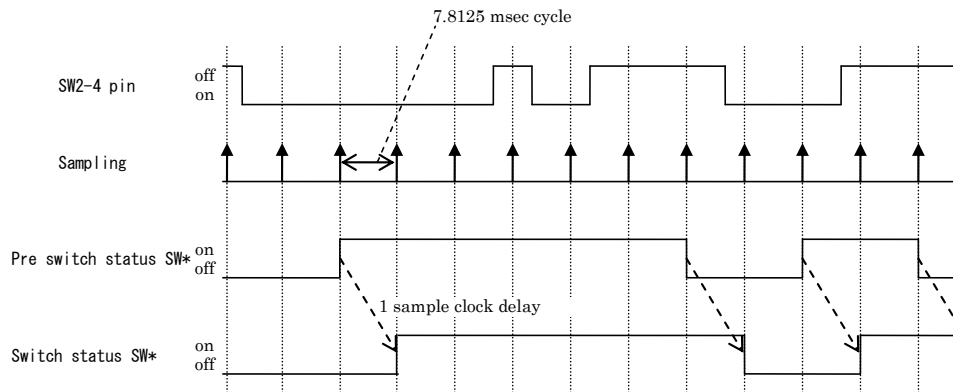


Figure 18 Timing chart of SW2/SW3/SW4 Detector

10.7. Battery monitor

The battery monitor controls LED and can set the AK1594 in power down.

LED Control

The battery monitor controls LED light ON or blinks when AVDD voltage drops below Detect Voltage1 (VALERT).

Power down controller

The battery monitor sets the AK1594 in full power down status when AVDD voltage drops below Detect Voltage2N or Detect Voltage2H. (VSLEEPN or VSLEEPH)

This function is controlled by {BAT_EN}. Detect voltage1 is not available when {POWR_MODE} = "0b10", or "0b11".

Refer to 7.3 Characteristics of Battery monitor.

10.8. LED

The AK1594 has handy LED functions to know device status. LED pin drives 1mA or 3mA setting by {I_LED}. To disable LED function for saving power consumption, LED pin should be set to open or disable all registers listed below. ({SW1LED_EN} = {SW2LED_EN} = {SW3LED_EN} = {SW4_LED_EN} = {BAT_LED_EN} = "0b0")

LED Blink Mode	EEPROM Setting	LED Status
SW1pin falling	{SW1LED_EN} = "0b1" : LED enable {SW1LED_EN} = "0b0" : LED disable	Normally on during SW1 pin = "L"
SW2pin falling	{SW2LED_EN} = "0b1" : LED enable {SW2LED_EN} = "0b0" : LED disable	Normally on during SW2 pin = "L"
SW3pin falling and {SW3_FUNC}="0b0"	{SW3_FUNC}="0b0" and {SW3LED_EN} = "0b1" : LED enable {SW3LED_EN} = "0b0" : LED disable	As many state when SW3 pin Falling
SW3pin falling and {SW3_FUNC}="0b1"	{SW3_FUNC}="0b1" and {SW3LED_EN} = "0b1" : LED enable {SW3LED_EN} = "0b0" : LED disable	Cyclic 9.750s sleeps and 0.25s blinks after SW3 pin falling
SW4pin Falling	{SW4_LED_EN} = "0b1": LED enable {SW4_LED_EN} = "0b0": LED disable	As many state when SW4 pin falling
AVDD voltage drops below Detect voltage1 at Normal Power Mode	{BAT_EN} = "0b1" and {BAT_LED_EN} = "0b1" : LED enable {BAT_LED_EN} = "0b0" : LED disable	{BAT_SEL1} = "0b0" :LED On {BAT_SEL1} = "0b1": Cyclic 9.750s sleeps and 0.25s blinks.

11. Power-up Sequence

AK1594 Power-up sequence is below.

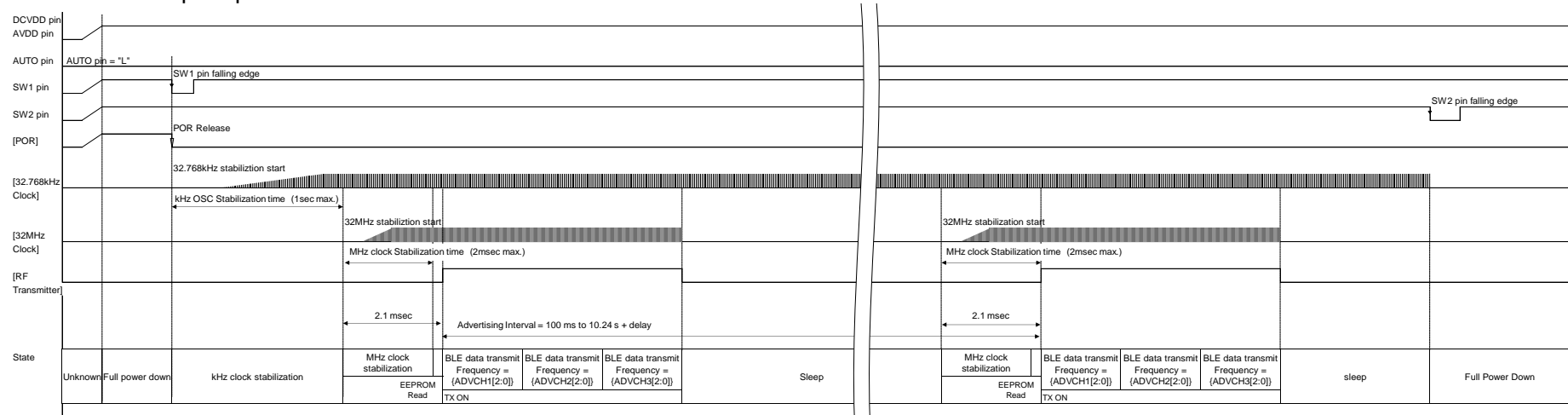


Figure 19 Power-up sequence (AUTO pin = "L")

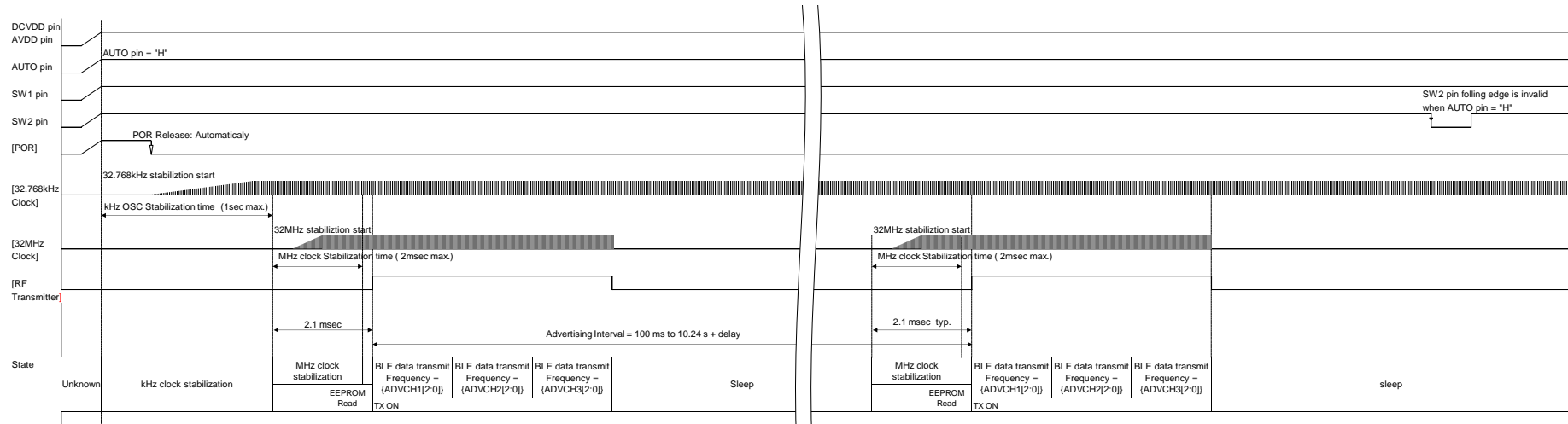
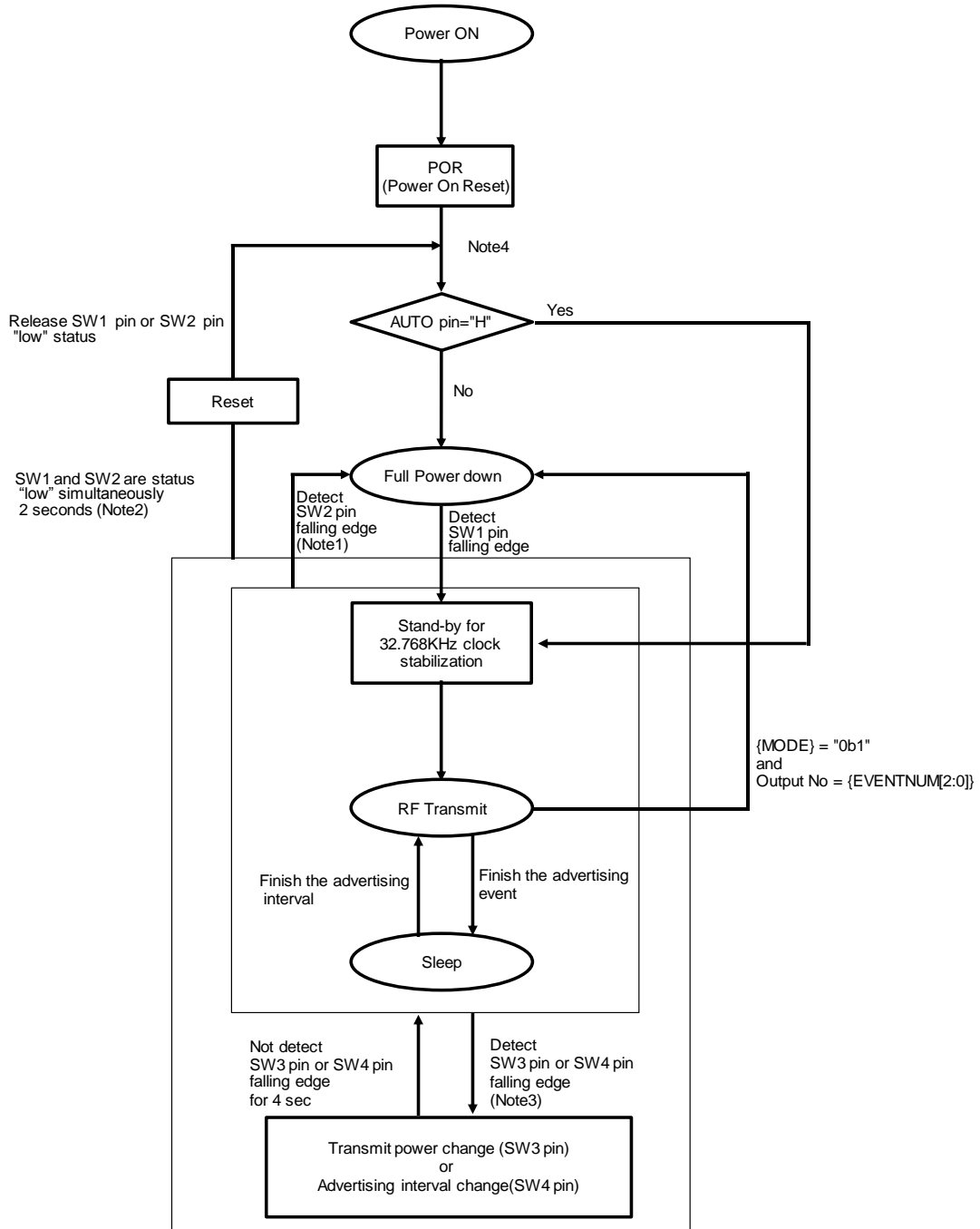


Figure 20 Power-up sequence (AUTO pin = "H")

12. Power up flow

AK1594 power up flow is below.



- Note1) It becomes valid only AUTO pin = "L" and {SW2_DIS} = "0b0".
- Note2) The AK1594 is reset when SW1 and SW2 set to "L" more than 2 seconds at the same time.
The AK1594 goes to full power down if SW1 and SW2 are kept "L" state simultaneously after the reset.
- Note3) SW3 pin function becomes valid only {SW3_FUNC} = "0b0". When {SW3_FUNC} = "0b1",
the transmission power will not be changed by SW3 falling edge after the AK1594 sets transmitter gain to maximum.
- Note4) The AK1594 set Output No = "1" after the reset.

Figure 21 AK1594 power up flow

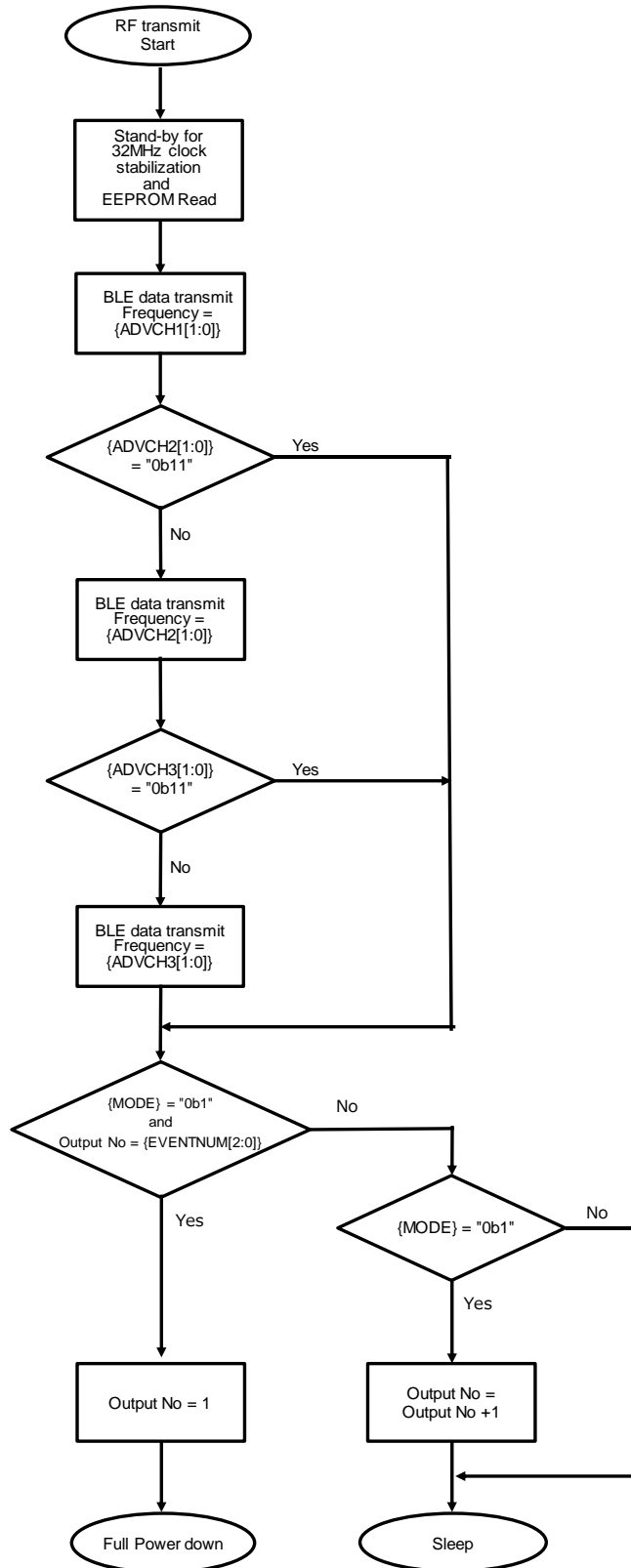


Figure 22 AK1594 RF transmit flow

13. EEPROM Function

13.1. EEPROM access

The AK1594 supports EEPROM access via the serial interface.
 The value (0) or (1) or 0x06, 0x07, 0x08 address in the EEPROM map below is fixed. Please set values listed in the EEPROM map.
 Ex. 0x08 = 0x0000.
 Access to other EEPROM address listed in the table below is prohibited.

13.2. EEPROM map

<Name>	Addr.	D15(MSB) D07	D14 D06	D13 D05	D12 D04	D11 D03	D10 D02	D09 D01	D08 D00(LSB)
AKM1	0x00	AKMTEST							
AKM2	0x01								
MODE1, FIXED	0x02	BAT_EN ADVCH1[1]	BAT_LED_EN ADVCH1[0]	BAT_SEL1 ADVCH2[1]	BAT_SEL2 ADVCH2[0]	I_LED ADVCH3[1]	(0) ADVCH3[0]	(0) TXDATA_LOOP	MODE TXDATA_CW
MODE2, FIXED	0x03	(0)	POWR_MODE[1]	POWR_MODE[0]	POWRD[4]	POWRD[3]	POWRD[2]	POWRD[1]	POWRD[0]
SWACT	0x04	(0)	SW1LED_EN	EVENTNUM[2]	EVENTNUM[1]	EVENTNUM[0]	SW2_DIS	SW2LED_EN	SW3_FUNC
		SW3LED_EN	SW3STEP[2]	SW3STEP[1]	SW3STEP[0]	SW4LED_EN	SW4STEP[2]	SW4STEP[1]	SW4STEP[0]
ADVINT	0x05	(1)	ADVINTVL[14]	ADVINTVL[13]	ADVINTVL[12]	ADVINTVL[11]	ADVINTVL[10]	ADVINTVL[9]	ADVINTVL[8]
		ADVINTVL[7]	ADVINTVL[6]	ADVINTVL[5]	ADVINTVL[4]	ADVINTVL[3]	ADVINTVL[2]	ADVINTVL[1]	ADVINTVL[0]
FIXED	0x06	(0x0800)							
FIXED	0x07	(0x010C)							
FIXED	0x08	(0x0000)							
Preamble	0x09	CRC_EN	WHITE_EN	PDULEN[5]	PDULEN[5]	PDULEN[4]	PDULEN[3]	PDULEN[2]	PDULEN[1]
Access Address	0x0A	Preamble							
		Access Address1							
		Access Address2							
		Access Address3							
PDU	0x0C	Access Address4							
		PDU1							
		PDU2							
		PDU3							
		PDU4							
		PDU5							
		PDU6							
		PDU7							
		PDU8							
		PDU9							
		PDU10							
		PDU11							
		PDU12							
		PDU13							
		PDU14							
		PDU15							
		PDU16							
PDU17									
PDU18									
PDU19									
PDU20									
PDU21									
PDU22									
PDU23									
PDU24									
PDU25									
PDU26									
PDU27									
PDU28									
PDU29									
PDU30									
PDU31									
PDU32									
PDU33									
PDU34									
PDU35									
PDU36									

<Name>	Addr.	D15(MSB) D07	D14 D06	D13 D05	D12 D04	D11 D03	D10 D02	D09 D01	D08 D00(LSB)
	0x1E	PDU37							
		PDU38							
	0x1F	PDU39							
		CRC1							
CRC	0x20	CRC2							
		CRC3							

Note 1 When AK1594 status is EEPROM Read in 11.Power-up Sequence Figure 19 or Figure 20, the EEPROM setting is valid. The AK1594 just stores raw data in the EEPROM. The EEPROM setting becomes valid once the raw data is transferred to the internal register.

Note 2 All internal register values are set to 0 after reset.

Note 3 When the AK1594 goes into Full Power Down state, all internal register values are set to 0 except {I_LED}, {SW1LED_EN}, {SW2_DIS} and {SW2LED_EN}.

13.2.1. AKM1, AKM2 (0x00, 0x01)

Do not access these address.

13.2.2. MODE1 (0x02)**13.2.2.1. BAT_EN**

Battery monitor enable

BAT_EN	Function
0	Battery monitor function disable
1	Battery monitor function enable

13.2.2.2. BAT_LED_EN

LED function enable

BAT_LED_EN	Function
0	LED disable
1	LED enable

Note 1 This setting is valid only when {BAT_EN} = "0b1".

Note 2 Detect voltage₁ is 2.3V Typ.

Note 3 Refer to 10.7Battery monitor

13.2.2.3. BAT_SEL1

LED ON/Blink selector

BAT_SEL1	Function
0	LED On
1	LED Blink Note ₃

Note 1 This setting is valid only when {BAT_EN} = "0b1" and {BAD_LED_EN} = "0b1".

Note 2 Detect voltage₁ is 2.3V Typ.

Note 3 9.750sec sleeps and 0.25sec blinks

Note 4 Refer to 10.7Battery monitor

13.2.2.4. BAT_SEL2

Full power down mode enable for battery monitor

BAT_SEL2	Function
0	Full power down disable
1	Full power down enable

Note 1 This setting is valid only when {BAT_EN} = "0b1"

Note 2 When power mode is normal, Detect Voltage₂ = 2.0V Min. When power mode is high, Detect Voltage₂ = 2.225V Min.

Note 3 Refer to 10.7Battery monitor

13.2.2.5. I_LED

LED current setting

I_LED	Function
0	1.0 mA
1	3.0 mA

Note 1 All internal register values of the AK1594 are "0" right after resetting. {I_LED} setting becomes valid after the process that the AK1594 transfers EEPROM data to the internal register. {I_LED} is 0 during this transfer process even if {I_LED} is set to 1.

13.2.2.6. Beacon operating mode setting

MODE	Function
0	Continuous Burst Mode
1	Configured TX Mode

Note 1 When AUTO pin is "H", The AK1594 keeps Continuous Transmission, which is {MODE} = "0b0", even if {MODE} is set to "0b1".

13.2.2.7. Advertising channel 1st setting

Advertising channel 1st setting

ADVCH1[1]	ADVCH1[0]	Function
0	0	37ch
0	1	38ch
1	0	39ch
1	1	37ch

Note 1 This value is used as advertising channel index for data whitening

13.2.2.8. Advertising channel 2nd setting

Advertising channel 2nd setting

ADVCH2[1]	ADVCH2[0]	Function
0	0	37ch
0	1	38ch
1	0	39ch
1	1	OFF

Note 1 This value is used as advertising channel index for data whitening

Note 2 In case of {ADVCH2[1:0]} = "0b11", the AK1594 doesn't output 2nd, 3rd advertising channel output.

13.2.2.9. Advertising channel 3rd setting

Advertising channel 3rd setting

ADVCH3[1]	ADVCH3[0]	Function
0	0	37ch
0	1	38ch
1	0	39ch
1	1	OFF

Note 1 This value is used as advertising channel index for data whitening

Note 2 In case of {ADVCH3[1:0]} = "0b11", the AK1594 doesn't output 3rd advertising channel.

Setting Example 1)

Advertising channel 1st: 37ch
 Advertising channel 2nd: 38ch
 Advertising channel 3rd: 39ch



Register name	Value
ADVCH1[1:0]	0b00 (37ch)
ADVCH2[1:0]	0b01 (38ch)
ADVCH3[1:0]	0b10 (39ch)

Setting Example 2)

Advertising channel 1st: 39ch
 Advertising channel 2nd: 37ch
 Advertising channel 3rd: 38ch



Register name	value
ADVCH1[1:0]	0b10 (39ch)
ADVCH2[1:0]	0b00 (37ch)
ADVCH3[1:0]	0b01 (38ch)

Setting Example 3)

Advertising channel 1st: 37ch
 Advertising channel 2nd: 38ch
 Advertising channel 3rd: OFF



Register name	Value
ADVCH1[1:0]	0b00 (37ch)
ADVCH2[1:0]	0b01 (38ch)
ADVCH3[1:0]	0b11(OFF)

Setting Example 4)

Advertising channel 1st: 37ch
 Advertising channel 2nd: OFF
 Advertising channel 3rd: OFF



Register name	Value
ADVCH1[1:0]	0b00 (37ch)
ADVCH2[1:0]	0b11(OFF)
ADVCH3[1:0]	0b11(OFF)

13.2.2.10. TXDATA_LOOP

TXDATA_LOOP	Function
0	Burst Transmission
1	Continuous Transmission

Please set {TXDATA_LOOP} = "0b0" except regulatory testing. This register is enabled when CS pin is = "H". The AK1594 transmits continuous signal via RFOUT pin. Channel frequencies are set by {ADVCH1[1:0]}. Data whitening is done by based on {ADVCH1[1]} setting when {WHITE_EN} = "0b1".

13.2.2.11. TXDATA_CW

Modulation Mode Select

TXDATA_CW	Function
0	GFSK
1	Continuous Wave

Please set {TXDATA_CW} = "0" except regulatory testing. The AK1594 transmits fixed frequency signal via RFOUT when {TXDATA_CW} = 1. The frequency setting is set by {ADVCH1[1:0]} to {ADVCH3[1:0]} that are 37ch=2402MHz, 38ch=2426MHz, 39ch=2480MHz.

13.2.3. MODE2 (0x03)**13.2.3.1. POWR_MODE [1:0]**

Power mode setting

POWR_MODE[1]	POWR_MODE[0]	Function
0	0	Normal power mode
0	1	Prohibited
1	Don't care	High power mode

13.2.3.2. POWRD[4:0] (TX power setting)

For normal power mode

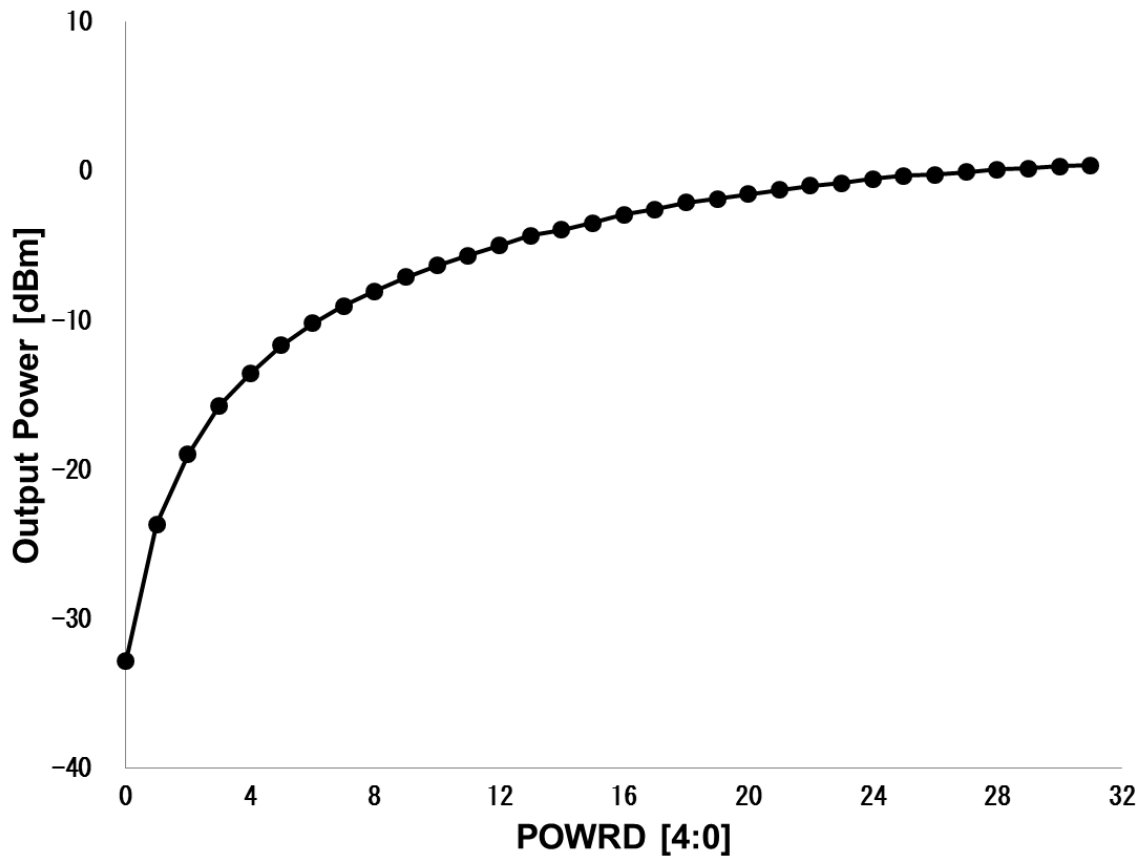


Figure 23 POWRD code vs Output power for normal mode

Note 1 The output power (Figure 23) is a reference value. Output power specification will be changed by RF matching network and board design.

For high power mode

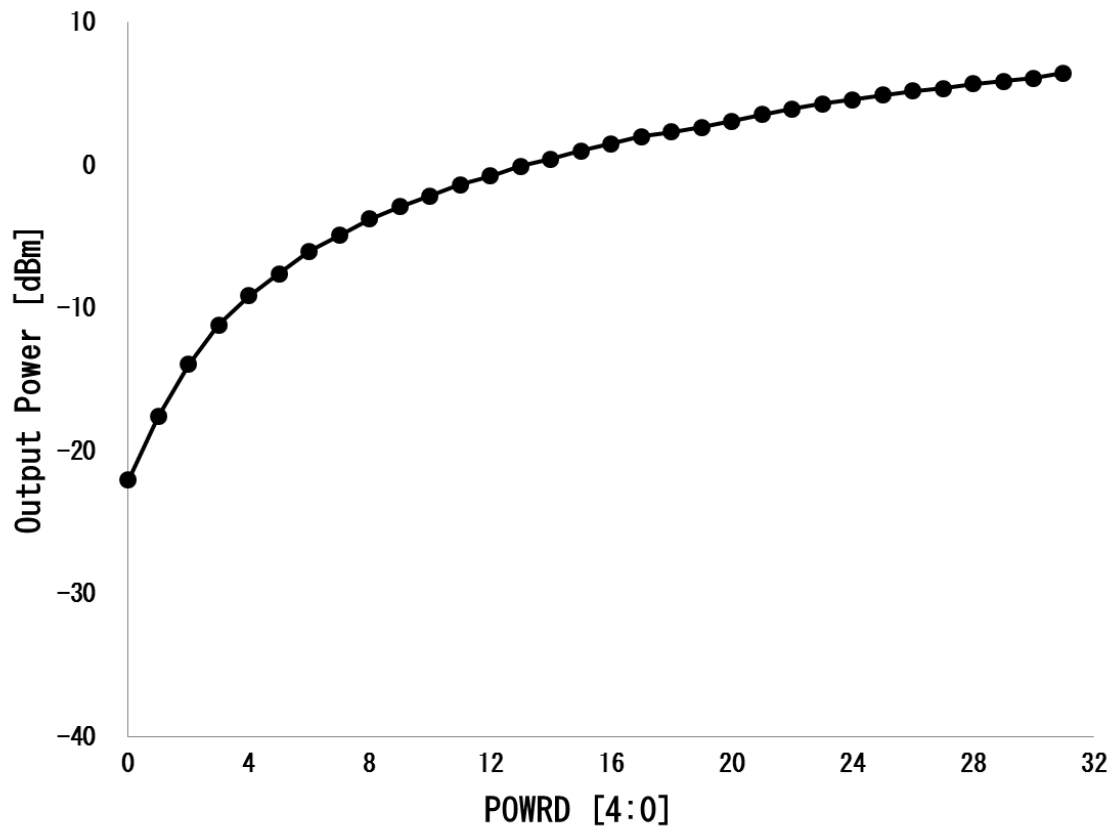


Figure 24 POWRD code vs Output power for high power mode

Note 1 The output power (Figure 24) is a reference value. Output power specification will be changed by RF matching network and board design.

13.2.4. SWACT (0x04)**13.2.4.1. SW1LED_EN**

LED ON/OFF for SW1 pin

SW1LED_EN	Function
0	LED OFF
1	LED ON LED ON when SW1 pin = "L".

Note 1 All internal register values of the AK1594 are 0 right after resetting. {SW1LED_EN} setting becomes valid after the process that the AK1594 transfers EEPROM data to the internal register. {SW1LED_EN} is 0b0 during this transfer process even if {SW1LED_EN} is set to 0b1.

13.2.4.2. EVENTNUM[2:0]

The number of advertising event setting

EVENTNUM[2]	EVENTNUM[1]	EVENTNUM[0]	Function
0	0	0	Prohibited
0	0	1	1time Advertising event
0	1	0	2 times Advertising event
0	1	1	3 times Advertising event
1	0	0	4 times Advertising event
1	0	1	5 times Advertising event
1	1	0	Prohibited
1	1	1	Prohibited

Note 1 {EVENTNUM[2:0]} is enabled by setting {MODE} = "1".

13.2.4.3. SW2_DIS

SW2 pin disable setting

SW2_DIS	Function
0	SW2 pin enable
1	SW2 pin disable

Note 1 All internal register values of the AK1594 are 0 right after resetting. {SW2_DIS} setting becomes valid after the process that the AK1594 transfers EEPROM data to the internal register. {SW2_DIS} is 0 during this transfer process even if {SW2_DIS} is set to 1.

Note 2 {SW2_DIS} = "1" automatically when AUTO pin = "H".

13.2.4.4. SW2LED_EN

LED ON/OFF for SW2 pin

SW2LED_EN	Function
0	LED OFF
1	LED ON LED ON when SW2 pin = "L".

Note 1 {SW2LED_EN} is enabled by {SW2_DIS} = "0b0"

Note 2 All internal register values of the AK1594 are 0 right after resetting. {SW2LED_EN} setting becomes valid after the process that the AK1594 transfers EEPROM data to the internal register. {SW2LED_EN} is 0b0 during this transfer process even if {SW2LED_EN} is set to 0b1.

13.2.4.5. SW3_FUNC

SW3 pin function setting

SW3_FUNC	Function
0	Power Step Adjustment is enabled
1	High power switch is enabled. Transmission power is set by {POWR_MODE[1]}="0b1", and POWRD[4:0]="31"

Refer to 10.4.4SW3 pin.

13.2.4.6. SW3LED_EN

LED ON/OFF for SW3 pin

SW3LED_EN	Function
0	LED OFF
1	LED ON Note 1,2

Note 1 When {SW3_FUNC} = "0b0", LED blinks based on {SW3STEP [2:0]} setting.

Note 2 When {SW3_FUNC} = "0b1", LED blinks 0.25s and 9.750s sleeps.

13.2.4.7. SW3STEP [2:0]

Transmission Power Step Adjustment

SW3STEP[2]	SW3STEP[1]	SW3STEP[0]	Step value[dec]
0	0	0	Prohibited
0	0	1	1
-	-	-	-
1	1	0	6
1	1	1	7

Note 1 {SW3STEP[2:0]} are enabled by {SW3_FUNC} = "0b0"

When {SW3_FUNC} = "0b0", the AK1594 changes output power at the SW3 pin falling edge. TX power is set by {POWRD [4:0]}

When SW3 pin set to High to Low, AK1594 changes status from burst transmission to TX power setting mode. The AK1594 changes TX power every SW3 pin falling edge during the TX power setting mode.

The AK1594 changes status SW3state1 → SW3state2 → SW3state3 → SW3state4 → SW3state5 → SW3state6 → SW3state1 → SW3state2→, number of LED blinks shows status when {SW3LED_EN}="0b1". LED blinking cycle is 360 msec.

When the AK1594 doesn't detect another SW3 pin falling edge for more than 4 seconds after the SW3 pin falling edge detection, the AK1594 finishes this power step adjustment process and returns to burst transmission.

Refer to 10.4.4 SW3 pin.

SW3State	TX power formula Note 1	Number of LED blink times (Note 2)
State1	{POWRD[4:0]} – {SW3STEP[2:0]} x 0	1
State2	{POWRD[4:0]} – {SW3STEP[2:0]} x 1	2
State3	{POWRD[4:0]} – {SW3STEP[2:0]} x 2	3
State4	{POWRD[4:0]} – {SW3STEP[2:0]} x 3	4
State5	{POWRD[4:0]} – {SW3STEP[2:0]} x 4	5
State6	{POWRD[4:0]} – {SW3STEP[2:0]} x 5	6

Note 1 Minimum TX power code = "0b0". If the calculation result is negative, the AK1594 just set TX power code = "0b0".as the result.

Note 2 LED function is enabled by setting {SW3LED_EN} = "0b1".

13.2.4.8. SW4LED_EN

SW4 pin LED ON/OFF setting

SW4LED_EN	Function
0	LED OFF
1	LED blinks as many SW4STEP[2:0] state when SW4 pin falling

13.2.4.9. SW4STEP[2:0]

Advertising Interval Step Adjustment

SW4STEP[2:0]	Interval Step[msec]
000	0.625
001	10
010	20
011	50
100	100
101	200
110	500
111	1000

The AK1594 changes advertising interval at the SW4 pin falling edge. Advertising intervals are set by {ADVINTVL [14:0]}

When SW4 pin set to High to Low, AK1594 changes status from burst transmission to advertising interval setting mode. The AK1594 changes interval timing every SW4 pin falling edge during the advertising interval setting mode.

The AK1594 changes status SW4state1 → SW4state2 → SW4state3 → SW4state4 → SW4state5 → SW4state6 → SW4state1 → SW4state2 →, number of LED blinks shows status when {SW4LED_EN}="0b1". LED blinking cycle is 360 msec.

When the AK1594 doesn't detect another SW4 falling edge for more than 4 seconds after the SW4 falling edge detection, the AK1594 finishes this advertising interval step adjustment process and returns to burst transmission.

Refer to 10.4.5 SW4 pin.

SW4State	Advertising interval formula Note 1	Number of LED blink times (Note 2)
State1	"ADVINTVL[14:0]" + "SW4STEP[2:0]" x 0	1
State2	"ADVINTVL[14:0]" + "SW4STEP[2:0]" x 1	2
State3	"ADVINTVL[14:0]" + "SW4STEP[2:0]" x 2	3
State4	"ADVINTVL[14:0]" + "SW4STEP[2:0]" x 3	4
State5	"ADVINTVL[14:0]" + "SW4STEP[2:0]" x 4	5
State6	"ADVINTVL[14:0]" + "SW4STEP[2:0]" x 5	6

Note 1 Maximum value is 0x4000. If the calculation result is larger than 0x4000, the AK1594 just set 0x4000 as the advertising interval result.

Note 2 LED function is valid when {SW4LED_EN} = "0b1".

13.2.5. ADVINT (0x05)

13.2.5.1. Advertising Interval setting

ADVINTVL[14:0]	Advertising interval[msec]
000 0000 0000 0000	Prohibited
~	~ (Prohibited)
000 0000 1001 1111	Prohibited
000 0000 1010 0000	100.000
000 0000 1010 0001	100.625
000 0000 1010 0001	101.250
~	~
011 1111 1111 1110	10238.750
011 1111 1111 1111	10239.375
100 0000 0000 0000	10240.000
Other setting	10240.000

Advertising Interval setting example)

EEPROM 0x05 value	Advertising Interval [msec]
0x80A0	100
0x8140	200
0x81E0	300
0x8280	400
0x8320	500
0x83C0	600
0x8460	700
0x8500	800
0x85A0	900
0x8640	1000
0x8C80	2000
0x92C0	3000
0x9900	4000
0x9F40	5000
0xA580	6000
0xABC0	7000
0xB200	8000
0xB840	9000
0xBE80	10000

13.2.6. Preamble (0x09h[15:8])**13.2.6.1. CRC_EN**

CRC setting

CRC_EN	Function
0	CRC disable
1	CRC enable

Note 1 Please set {CRC_EN} = "0b1" except regulatory testing.

Note 2 For details of CRC function, refer to Bluetooth[®] specification**13.2.6.2. Whitening_EN**

Data whitening setting

WHITE_EN	Function
0	Data whitening disable
1	Data whitening enable

Note 1 Please set {CRC_EN} = "0b1" except regulatory testing.

Note 2 For details of whitening function, refer to Bluetooth[®] specification**13.2.6.3. PDU Length setting**

PDULEN[5:0]	Length[octet]
00 0000	Prohibited
00 0001	Prohibited
00 0010	2
00 0011	3
~	~
10 0101	37
10 0110	38
10 0111	39
Other setting	39

PDU length is the data length between access address and CRC.

Preamble (1 octet)	Access Address (4 octets)	PDU (2~39 octets)	CRC (3 octets)
-----------------------	---------------------------	-------------------	----------------

13.2.7. TX data (0x09 - 0x20)

Write TX data to the following addresses.

Preamble (0x09[7:0])

Access Address(0x0A,0x0B)

PDU(0x0C~0x1F[15:8])

CRC(0x1F[7:0], 0x20)

Note1 Unused sectors value are “don’t care”.

The EEPROM maximum size for transmission data is 47octets.

Preamble (1 octet)	Access Address (4 octets)	PDU (2~39 octets)	CRC (3 octets) Note1
-----------------------	---------------------------	-------------------	-------------------------

Note 1 When {CRC_EN} = “0b1”, CRC(0x1F[7:0], 0x20) is not need be set.

The output order of the data bits is as follows.

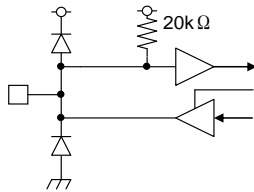
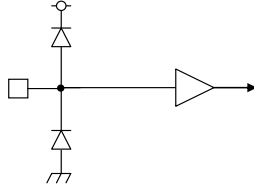
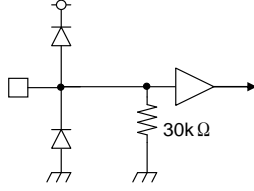
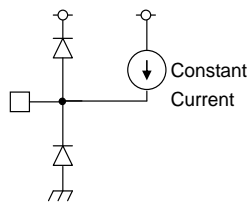
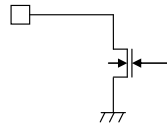
<Name>	Addr.	D15(MSB)	D14	D13	D12	D11	D10	D9	D8
		D07	D06	D05	D04	D03	D02	D01	D0(LSB)
Data[15:0]	-	Data[15]	Data[14]	Data[13]	Data[12]	Data[11]	Data[10]	Data[9]	Data[8]
		Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]

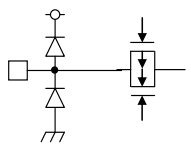
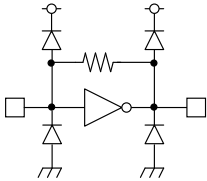
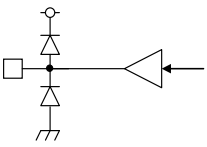
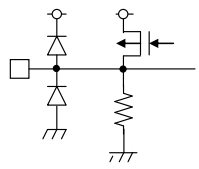
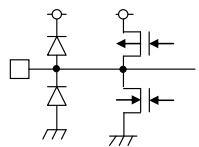
Data[8] → Data[9] → Data[10] → Data[11] → Data[12] → Data[13] → Data[14] → Data[15] →
 → Data[0] → Data[1] → Data[2] → Data[3] → Data[4] → Data[5] → Data[6] → Data[7]

Factory EEPROM value

Address	Factory Code	Address	Factory Code
0x00	Don't care	0x16	0x5555
0x01	Don't care	0x17	0xAAAA
0x02	0x5555	0x18	0x5555
0x03	0xAAAA	0x19	0xAAAA
0x04	0x5555	0x1A	0x5555
0x05	0xAAAA	0x1B	0xAAAA
0x06	0x5555	0x1C	0x5555
0x07	0xAAAA	0x1D	0xAAAA
0x08	0x5555	0x1E	0x5555
0x09	0xAAAA	0x1F	0xAAAA
0x0A	0x5555	0x20	0x5555
0x0B	0xAAAA		
0x0C	0x5555		
0x0D	0xAAAA		
0x0E	0x5555		
0x0F	0xAAAA		
0x10	0x5555		
0x11	0xAAAA		
0x12	0x5555		
0x13	0xAAAA		
0x14	0x5555		
0x15	0xAAAA		

14. LSI Interface Circuit

No	Pin Name	I/O	Function
13	SDAT	IO	Digital input / output pin 
6	SW1	I	Digital input pin 
9	SW2	I	
16	SW3	I	
17	SW4	I	
25	AUTO	I	
19	DATA	I	
20	DATA2	I	
11	SCLK	I	Digital input pin 
12	CS	I	
5	LED	O	Analog output pin 
22	RFOUT	O	Analog output pin 

No	Pin Name	I/O	Function
4	LPFO	IO	Analog input / output pin 
7	OSC1	I	Analog input pin 
8	OSC2	O	
15	LOSC1	I	
14	LOSC2	O	
18	TESTO	O	Digital output pin 
24	LDOC	O	Analog output pin 
23	PALDOC	O	Analog output pin 
28	SWITCH	O	

15. Recommended External Circuits

15.1. Recommended External Circuits

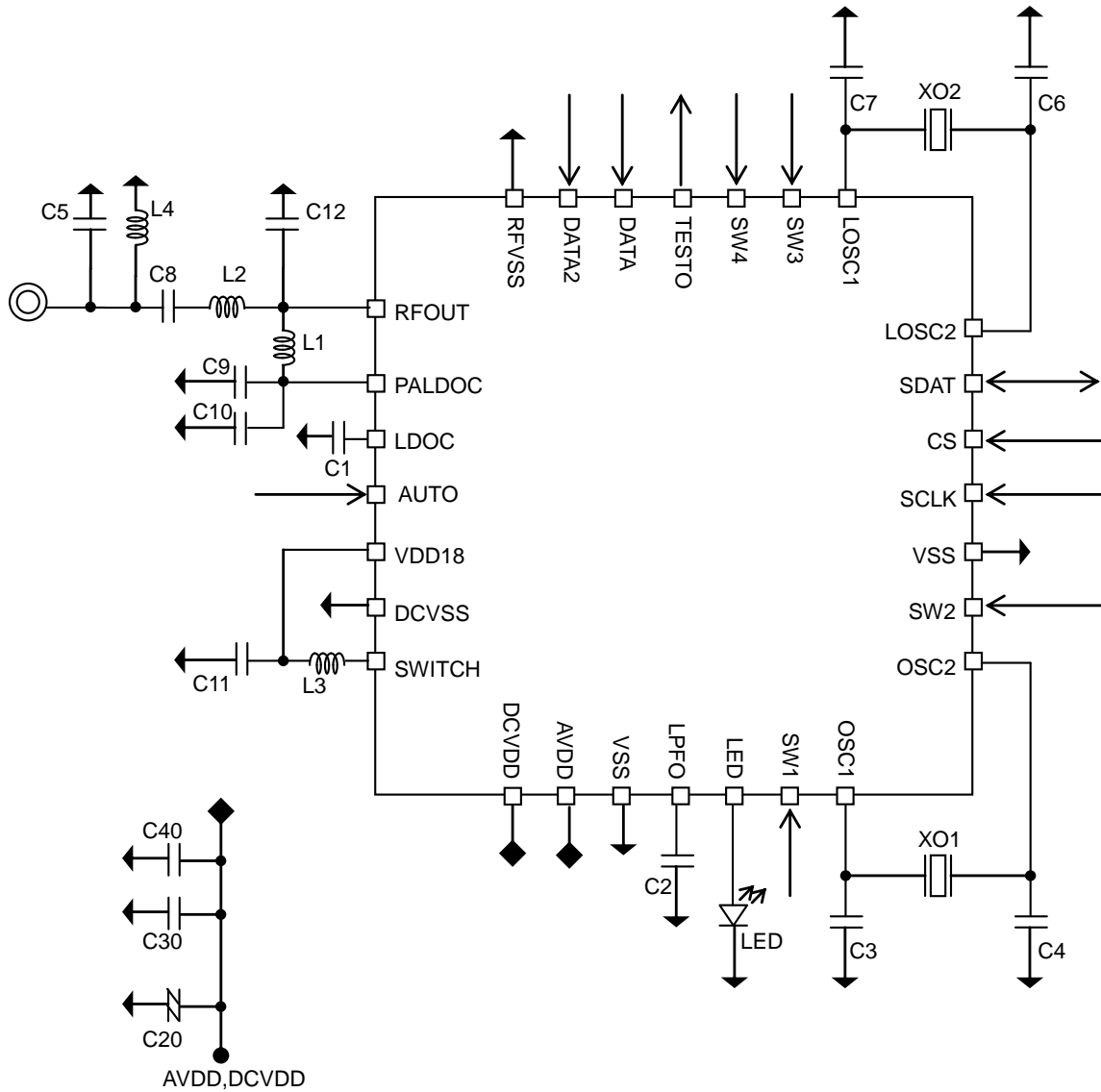


Figure 25 Recommended External Circuits

15.2. External component

Number	Value	Parts Number
C1	0.22 μ F	GRM155R71C224KA12D
C2	680pF	GRM1555C1H681JA01D
C3	6.8pF	GRM1555C1H6R8CA01D
C4	6.8pF	GRM1555C1H6R8CA01D
C5	1.8pF	GJM1555C1H1R8BB01D
C6	10pF	GRM1555C1H100JA01D
C7	10pF	GRM1555C1H100JA01D
C8	100pF	GRM1555C1H101JA01D
C9	10pF	GRM1555C1H100JA01D
C10	1000pF	GRM155R71H102KA01D
C11	0.047 μ F	GRM155R71E473KA88D
C12	0.6pF	GJM1555C1HR60BB01D
C20	10 μ F	GRM188C81C106MA73D
C30	-	
C40	10 μ F	GRM188C81C106MA73D
L1	3.3nH	LQW15AN3N3D10
L2	2.7nH	LQW15AN2N7C00D
L3	4.7 μ H, Avg DC resistance 0.44 ohm	LQM18PN4R7MFRL
L4	2.2nH	LQG15HS2N2S02D
XO1	32MHz, Load capacitance 6pF	FA-128 6pF, Q22FA12800517xx
XO2	32.768kHz, Load capacitance 9pF	FC-135 9pF, Q13FC13500003xx
LED	-	

Reference value. RF specification will be changed by RF matching network and board design.

16. Package

16.1. Outline Dimensions

28-pin QFN (4.0 x 4.0 x 0.70, 0.4mm pitch)
 (Unit: mm)

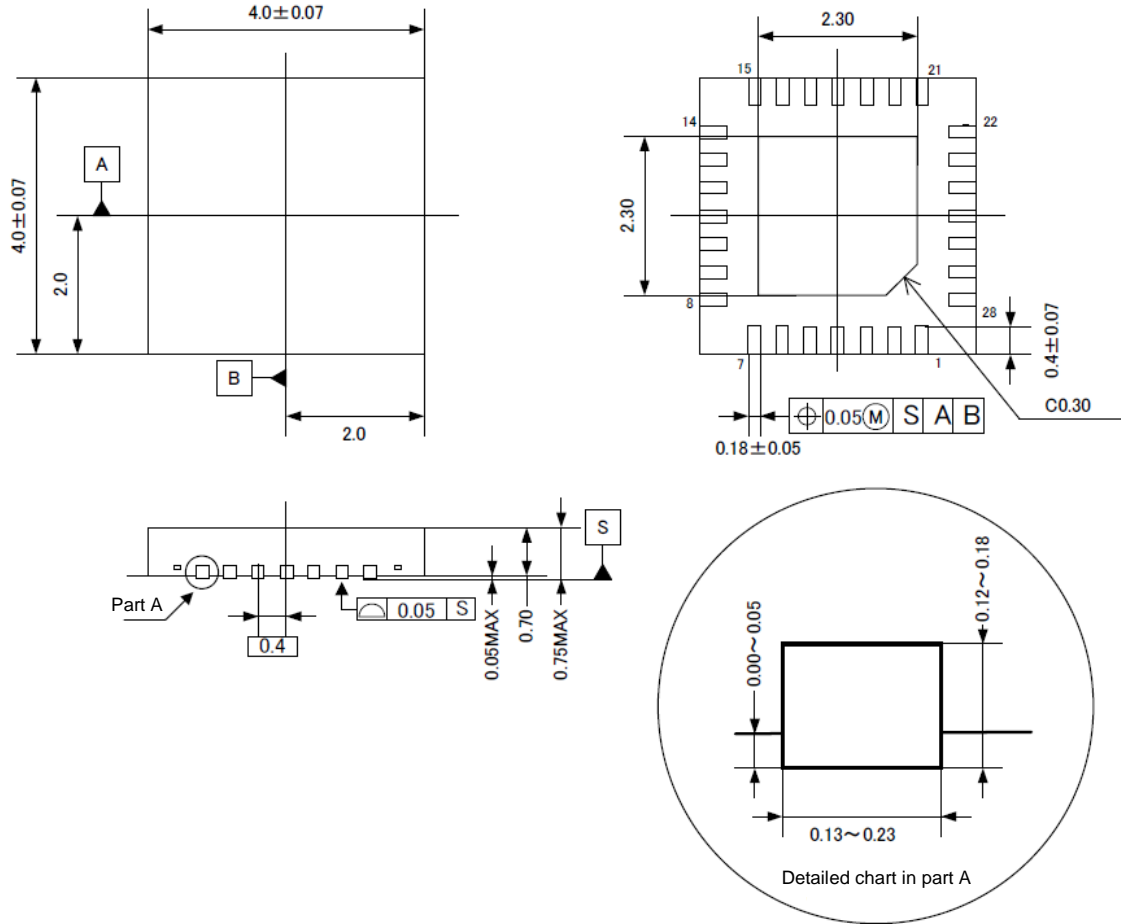


Figure 26 Package outer dimension

Note 1 Leave the exposed pad on the bottom surface of the package open.

16.2. Marking

- a. Style : QFN
- b. Number of pins : 28pins
- c. A1 pin marking : Circle
- d. Product number : 1594
- e. Date code : XXXX (4 digits)

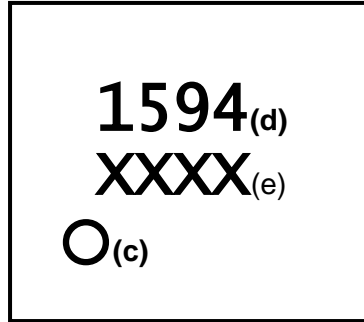


Figure27 Marking

17. Ordering Guide

-AK1594 28-pin QFN (4.0mm x 4.0mm x 0.70mm, 0.4mm pitch)

18. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
18/3/XX	00	First Edition		

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