# DSLVDS1002 3.3-V LVDS Single Channel High Speed Differential Receiver

## 1 Features

- Designed for Signaling Rates up to 400-Mbps
- Single 3.3V Power Supply Design (3.0-V to 3.6-V Range)
- 100-ps Typical Differential Skew
- 3.5-ns Maximum Propagation Delay
- Accepts Small Swing (±350-mV Typical) Differential Signal Levels
- Power Off Protection (High Impedance on LVDS Inputs)
- Flow-Through Pinout Simplifies PCB Layout
- Low Power Dissipation (10 mW typical@ 3.3 V static)
- LVDS Receiver Inputs Accept LVDS/BLVDS/LVPECL Inputs
- Failsafe Protection for Open, Short and Terminated Inputs
- SOT-23 5-lead package
- Meets or Exceeds ANSI TIA/EIA-644-A Standard
- Industrial temperature operating range (−40°C to +85°C)

## 2 Applications

- Board to Board Communication
- Test and Measurement
- Motor Drive
- Wireless Infrastructure
- Telecom Infrastructure
- Printer
- Multi Function Printer
- Professional Video Cameras
- Enterprise and Cinema Projectors
- LED Video Wall
- NIC Card
- Rack Server
- Ultrasound Scanners

## 3 Description

The DSLVDS1002 is a single channel Low Voltage Differential Signaling (LVDS) receiver designed for applications requiring low power dissipation, low noise and high data rates. In addition, the short circuit fault current is also minimized. The DSLVDS1002 device is designed to support data rates that are at least 400 Mbps (200 MHz) utilizing LVDS technology.

The DSLVDS1002 accepts low voltage (±350-mV typical) differential input signals and outputs a 3.3-V CMOS/TTL signal. The receivers also support open, shorted, and terminated (100 Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DSLVDS1002 is in a 5-lead SOT-23 package that is designed for easy PCB layout.

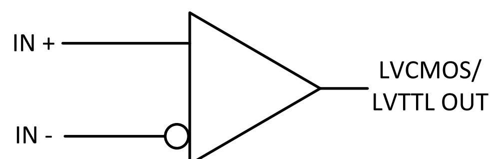
The DSLVDS1002 can be paired with its companion single line driver, DSLVDS1001, or with any LVDS driver, to provide a high-speed LVDS Interference.

**Device Information(1)**

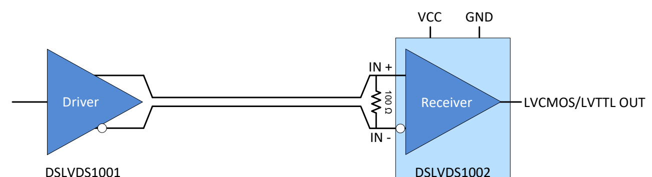
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
| --- | --- | --- |
| DSLVDS1002 | SOT-23 DBV | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Functional Block Diagram**




**Typical Application**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| July 2018 | * | Initial release. |


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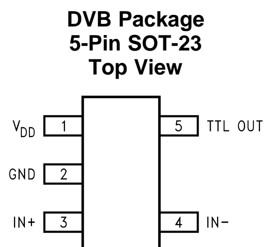
# 5 Pin Configuration and Functions

**DVB Package**
**5-Pin SOT-23**
**Top View**




**Pin Functions**

| Package Pin Number | Pin Name | Description |
|---|---|---|
| SOT-23 | | |
| 1 | $V_{DD}$ | Power Supply Pin, +3.3V ± 0.3V |
| 2 | GND | Ground Pin |
| 3 | IN + | Non-Inverting Receiver Input Pin |
| 4 | IN - | Inverting Receiver Input Pin |
| 5 | LVCMOS/LVTTL OUT | LVTTL/LVCMOS Receiver Output Pin |

# 6 Truth Table

| INPUTS | OUTPUT |
|---|---|
| $V_{ID}$ = [IN+] − [IN−] | TTL OUT |
| $V_{ID} \geq 0V$ | H |
| $V_{ID} \leq -0.1V$ | L |
| Full Fail-safe OPEN/SHORT or Terminated | H |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage ($V_{DD}$) | -0.3 | 4 | V |
| Input Voltage (IN+, IN−) | -0.3 | 3.9 | V |
| Output Voltage (TTL OUT) | -0.3 | VDD + 0.3 | V |
| Output Short Circuit Current | | -100 | mA |
| Package Power Dissipation | | 25 | °C |
| DBV Package | | 902 | mW |
| Derate DBV Package | 7.22 | 25 | mW/°C |
| Lead Temperature Soldering (4 sec.) | | 260 | °C |
| Junction Temperature | | 150 | °C |
| Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | +2.7 | +3.3 | +3.6 | V |
| Operating Free Air Temperature ($T_A$) | −40 | 25 | +85 | °C |

## 7.4 Thermal Information (3-pkg option) [delete me if not used]

| THERMAL METRIC[1] | | DSLVDS1002 | UNIT |
|---|---|---|---|
| | | SOT-23 (DVB) | |
| | | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 189.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 101.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 17.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 49 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 7.5 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. [1]

| PARAMETER | | TEST CONDITIONS | | PIN | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{TH}$ | Differential Input High Threshold | Valid across the specified common mode voltage ($V_{CM}$) range. | | IN+, IN− | | | 100 | mV |
| $V_{TL}$ | Differential Input Low Threshold | | | | −100 | −30 | | mV |
| $V_{CM}$ | Common-Mode Voltage | $V_{DD}$ = 2.7V, $V_{ID}$ = 100mV | | | 0.05 | | 2.35 | V |
| | | $V_{DD}$ = 3.0V to 3.6V, $V_{ID}$ = 100mV | | | 0.05 | | $V_{DD}$ - 0.3V | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = +2.8V | $V_{DD}$ = 3.6V or 0V | | −15 | 1 | 15 | µA |
| | | $V_{IN}$ = 0V | | | −15 | 1 | 15 | µA |
| | | $V_{IN}$ = +3.6V | $V_{DD}$ = 0V | | −20 | | +20 | µA |
| $\Delta I_{IN}$ | Change in Magnitude of $I_{IN}$ | $V_{IN}$ = +2.8V | $V_{DD}$ = 3.6V or 0V | | | 4 | | µA |
| | | $V_{IN}$ = 0V | | | | 4 | | µA |
| | | $V_{IN}$ = +3.6V | $V_{DD}$ = 0V | | | 4 | | µA |
| $I_{IND}$ | Differential Input Current | $V_{IN+}$ = +0.4V, $V_{IN-}$ = +0V | | | 3 | 3.9 | 4.4 | mA |
| $C_{IN}$ | Input Capacitance | IN+ = IN− = GND | | | | 3 | | pF |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −0.4 mA, $V_{ID}$ = +200 mV | | TTL OUT | 2.4 | 3.1 | | V |
| | | $I_{OH}$ = −0.4 mA, Inputs terminated | | | 2.4 | 3.1 | | V |
| | | $I_{OH}$ = −0.4 mA, Inputs shorted | | | 2.4 | 3.1 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2 mA, $V_{ID}$ = −200 mV | | | | 0.3 | 0.5 | V |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V [2] | | | −15 | −50 | −100 | mA |
| $V_{CL}$ | Input Clamp Voltage | $I_{CL}$ = −18 mA | | | −1.5 | −0.7 | | V |
| $I_{DD}$ | No Load Supply Current | Inputs Open | | $V_{DD}$ | | 5.4 | 9 | mA |

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as $V_{ID}$).
(2) Output short circuit current ($I_{OS}$) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

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## 7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHLD}$ | Differential Propagation Delay High to Low | $C_L$ = 15 pF | 1.0 | 1.8 | 3.5 | ns |
| $t_{PLHD}$ | Differential Propagation Delay Low to High | $V_{ID}$ = 200 mV | 1.0 | 1.7 | 3.5 | ns |
| $t_{SKD1}$ | Differential Pulse Skew $\|t_{PHLD} − t_{PLHD}\|$ [(1)] | (Figure 1 and Figure 2) | 0 | 100 | 400 | ps |
| $t_{SKD3}$ | Differential Part to Part Skew [(2)] | | 0 | 0.3 | 1.0 | ns |
| $t_{SKD4}$ | Differential Part to Part Skew [(3)] | | 0 | 0.4 | 1.5 | ns |
| $t_{TLH}$ | Rise Time | | | 500 | | ps |
| $t_{THL}$ | Fall Time | | | 500 | | ps |
| $f_{MAX}$ | Maximum Operating Frequency [(4)] | | 200 | 250 | | MHz |

(1) $t_{SKD1}$ is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(2) $t_{SKD3}$, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same $V_{DD}$ and within 5°C of each other within the operating temperature range.
(3) $t_{SKD4}$, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. $t_{SKD4}$ is defined as |Max − Min| differential propagation delay.
(4) $f_{MAX}$ generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, $V_{OL}$ (max 0.4V), $V_{OH}$ (min 2.4V), load = 15 pF (stray plus probes). The parameter is ensured by design. The limit is based on the statistical analysis of the device over the PVT range by the transition times ($t_{TLH}$ and $t_{THL}$).

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# 8 Parameter Measurement Information

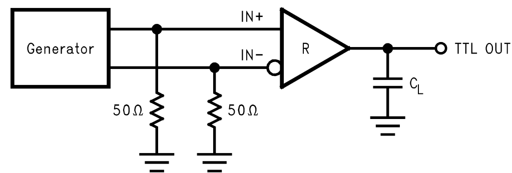


**Figure 1. Receiver Propagation Delay and Transition Time Test Circuit**

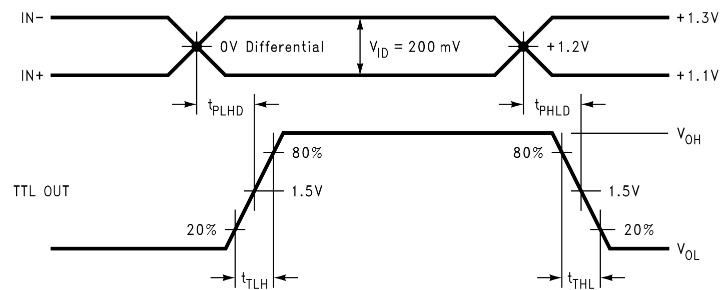


**Figure 2. Receiver Propagation Delay and Transition Time Waveforms**

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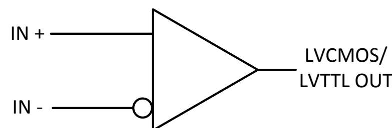
# 9 Detailed Description

## 9.1 Overview

The DSLVDS1002 is a single channel, low voltage differential signaling (LVDS) line receiver. It operates from a single power supply that is nominally 3.3-V, but can be as low as 3.0-V and as high as 3.6-V. The input to the DSLVDS1002 is a differential signal complying with the LVDS Standard (TIA/EIA-644) and the output is a 3.3-V LVCMOS/LVTTL signal. The differential input signal operates with a signal level of 340 mV, nominally, at common-mode voltage of 1.2-V. The differential nature of the inputs provides immunity to common-mode coupled signals that the driven signal may experience. A termination resistor of 100-Ω should be selected to match the media, and should be located as close to the receiver as possible.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

The DSLVDS1002 is capable of detecting signals as low as 100-mV, over a ±1-V common-mode range centered around 1.2-V. The AC parameters of the input pins are optimized for a recommended operating input voltage range of 0-V to 2.4-V (measured from each pin to ground). The device will operate for receiver input voltages up to $V_{DD}$, but exceeding $V_{DD}$ will turn on the ESD protection circuitry which will clamp the bus voltages.

## 9.4 Device Functional Modes

### 9.4.1 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

### 9.4.2 Threshold

The LVDS Standard (ANSI/TIA/EIA-644-A) specifies a maximum threshold of ±100mV for the LVDS receiver. The DSLVDS1002 supports an enhanced threshold region of −100mV to 0V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in Figure 4. The typical DSLVDS1002 LVDS receiver switches at about −30mV. Note that with $V_{ID}$ = 0V, the output will be in a HIGH state. With an external fail-safe bias of +25mV applied, the typical differential noise margin is now the difference from the switch point to the bias point. In the example below, this would be 55mV of Differential Noise Margin (DNM) (+25mV − (−30mV)). With the enhanced threshold region of −100mV to 0V, this small external fail-safe biasing of +25mV (with respect to 0V) gives a DNM of a comfortable 55mV. With the standard threshold region of ±100mV, the external fail-safe biasing would need to be +25mV with respect to +100mV or +125mV, giving a DNM of 155mV which is stronger fail-safe biasing than is necessary for the DSLVDS1002. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

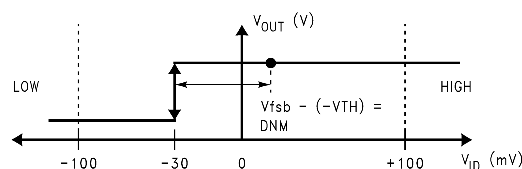



**Figure 3. VTC of the DSLVDS1002 LVDS Receiver**

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## Device Functional Modes (continued)

### 9.4.3 Fail-Safe Feature

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to LVCMOS/LVTTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** It is not required to tie the receiver inputs to ground or any supply voltage. Internal failsafe circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

The DSLVDS1002 is compliant to the original ANSI EIA/TIA-644 specification and is also compliant to the new ANSI EIA/TIA-644-A specification with the exception the newly added $\Delta I_{IN}$ specification. Due to the internal fail-safe circuitry, $\Delta I_{IN}$ cannot meet the 6μA maximum specified. This exception will not be relevant unless more than 10 receivers are used.

Additional information on fail-safe biasing of LVDS devices may be found in AN-1194 Failsafe Biasing of LVDS Interfaces (SNLA051).

### 9.4.4 Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

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## Device Functional Modes (continued)

### 9.4.5 Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

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# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The DSLVDS1002 device is a single-channel LVDS receiver. The functionality of this device is simple, yet extremely flexible, leading to its use in designs ranging from wireless base stations to desktop computers. The varied class of potential applications share features and applications discussed in the paragraphs below.

## 10.2 Typical Application

### 10.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 4.

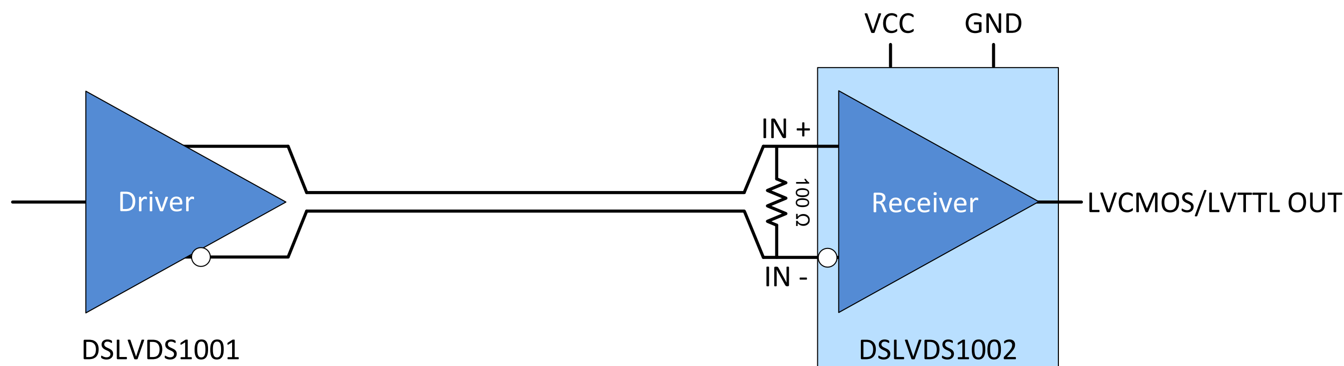


**Figure 4. Typical Application**

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 4 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

### 10.2.2 Design Requirements

| DESIGN PARAMETERS | EXAMPLE VALUE |
| --- | --- |
| Receiver Supply Voltage ($V_{CC}$) | 3.0 to 3.6 V |
| Receiver Output Voltage | 0 to 3.6 V |
| Signaling Rate | 0 to 400 Mbps |
| Interconnect Characteristic Impedance | 100 Ω |
| Termination Resistance | 100 Ω |
| Number of Receiver Nodes | 1 |
| Ground shift between driver and receiver | ±1 V |

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### 10.2.3 Detailed Design Procedure

#### *10.2.3.1 Receiver Bypass Capacitance*

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson[(1)], equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. [(1)]

$$C_{chip} = \left( \frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \tag{1}$$

$$C_{LVDS} = \left( \frac{1A}{0.2V} \right) \times 200\ \text{ps} = 0.001\ \mu F \tag{2}$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.001 μF). You should place the smallest value of capacitance as close as possible to the chip.

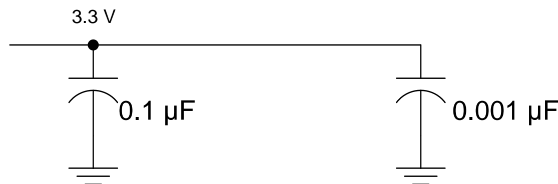


**Figure 5. Recommended LVDS Bypass Capacitor Layout**

#### *10.2.3.2 Interconnecting Media*

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

#### *10.2.3.3 PCB Transmission Lines*

As per SNLA187, Figure 6 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.


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When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 6 shows examples of edge-coupled microstrip lines, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

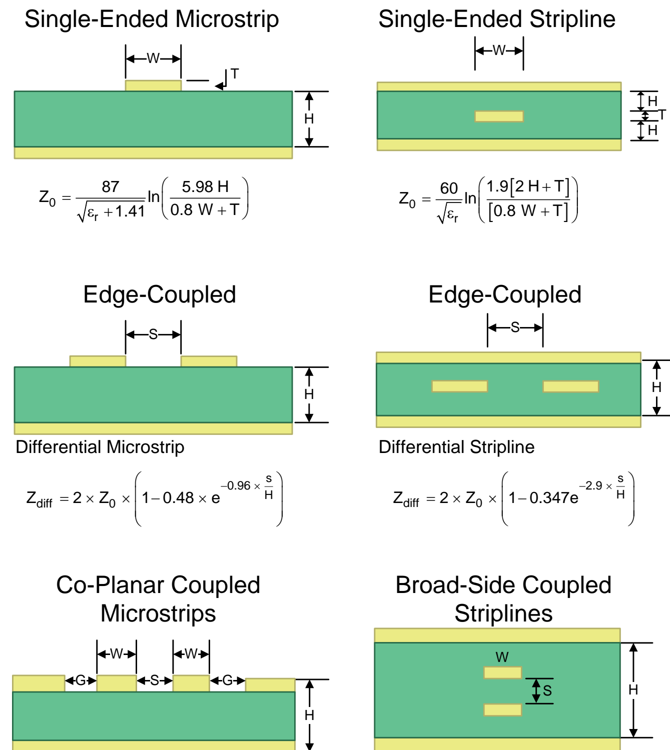


**Figure 6. Controlled-Impedance Transmission Lines**

ADVANCE INFORMATION

# 11 Power Supply Recommendations

## 11.1 Power Supply Considerations

The DSLVDS1001 driver is designed to operate from a single power supply with supply voltage in the range of 3.0 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used.

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# 12 Layout

## 12.1 Layout Guidelines

### 12.1.1 Layout Guidelines

#### *12.1.1.1 Microstrip vs. Stripline Topologies*

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 7.

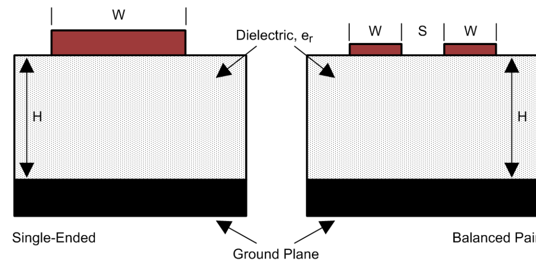


**Figure 7. Microstrip Topology**

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for $Z_O$ based on the overall noise budget and reflection allowances. Footnotes 1[(2)], 2[(3)], and 3[(4)] provide formulas for $Z_O$ and $t_{PD}$ for differential and single-ended traces. [(2)] [(3)] [(4)]

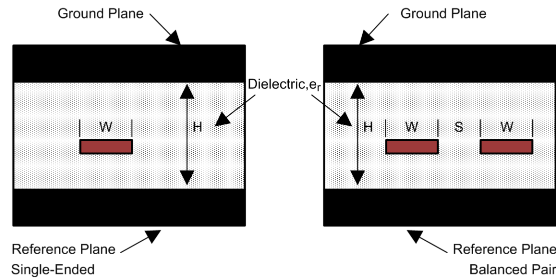


**Figure 8. Stripline Topology**

#### *12.1.1.2 Dielectric Type and Board Construction*

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of LVCMOS/LVTTL signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

(2) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(3) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(4) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

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## Layout Guidelines (continued)

### *12.1.1.3 Recommended Stack Layout*

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the LVCMOS/LVTTL to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 9.

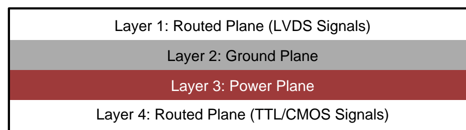


**Figure 9. Four-Layer PCB Board**

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**NOTE**

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

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One of the most common stack configurations is the six-layer board, as shown in Figure 10.

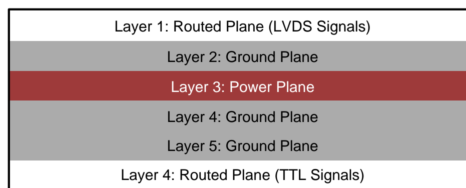


**Figure 10. Six-Layer PCB Board**

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

### *12.1.1.4 Separation Between Traces*

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

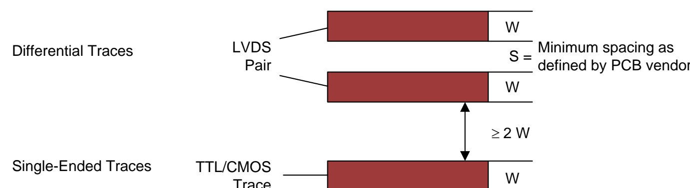


**Figure 11. 3-W Rule for Single-Ended and Differential Traces (Top View)**


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ADVANCE INFORMATION

## Layout Guidelines (continued)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

#### 12.1.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

#### 12.1.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

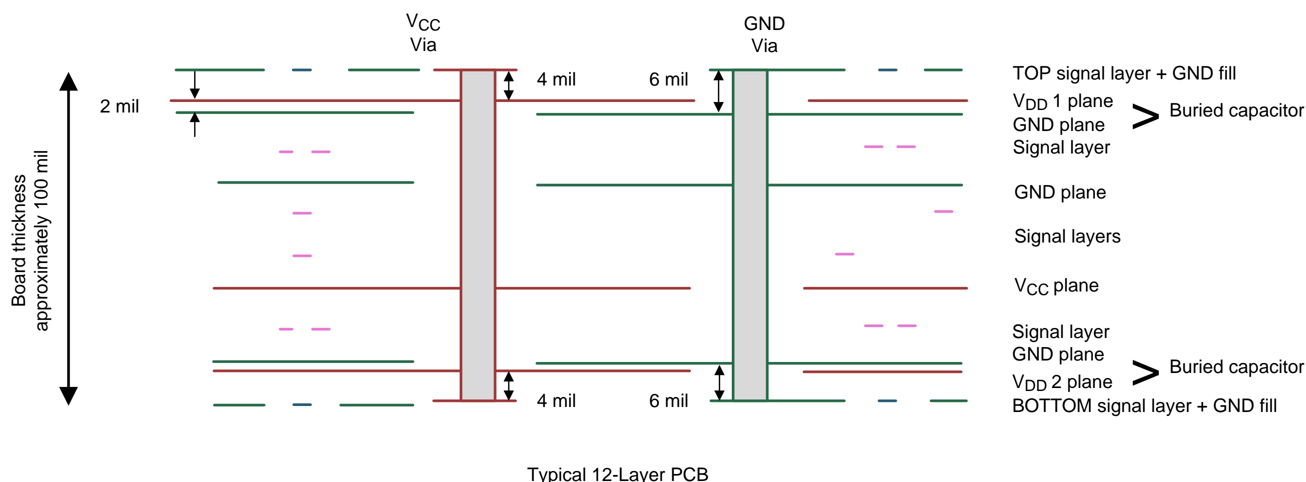


**Figure 12. Low Inductance, High-Capacitance Power Connection**

Bypass capacitors should be placed close to $V_{DD}$ pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 13(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 5-1 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 6) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so

ADVANCE INFORMATION

## Layout Guidelines (continued)

important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in Figure 13(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the $V_{DD}$ via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

**Figure 13. Typical Decoupling Capacitor Layouts**

ADVANCE INFORMATION

## 12.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 14.

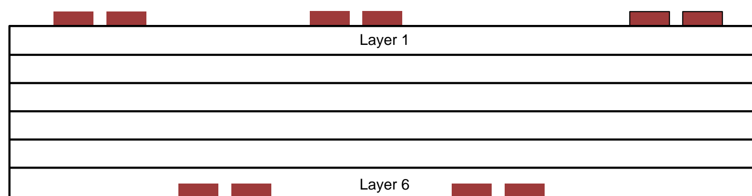


**Figure 14. Staggered Trace Layout**

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 15. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

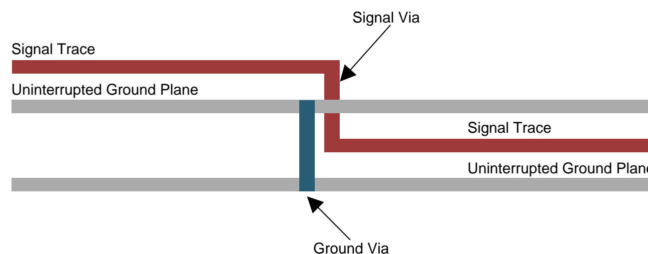


**Figure 15. Ground Via Location (Side View)**

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.


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# 13 Device and Documentation Support

## 13.1 Receiving Notification of Documentation Updates

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DSLVDS1002DBVR | PREVIEW | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 85 | | |
| DSLVDS1002DBVT | PREVIEW | SOT-23 | DBV | 5 | 250 | TBD | Call TI | Call TI | -40 to 85 | | |
| PDSLVDS1002DBVT | ACTIVE | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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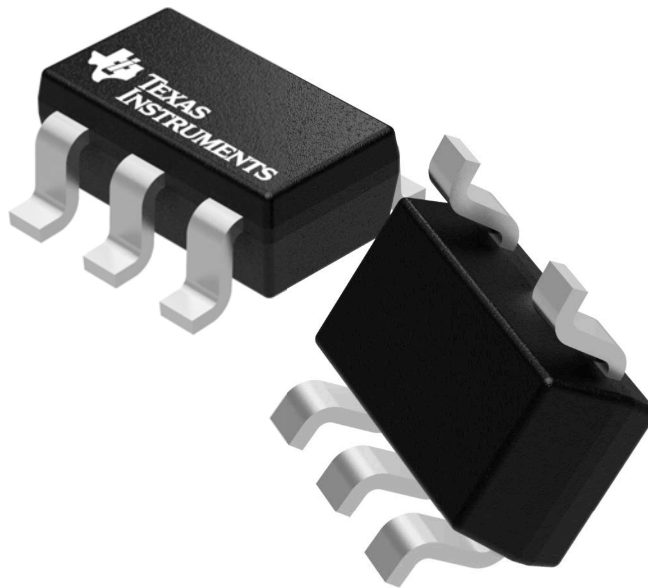
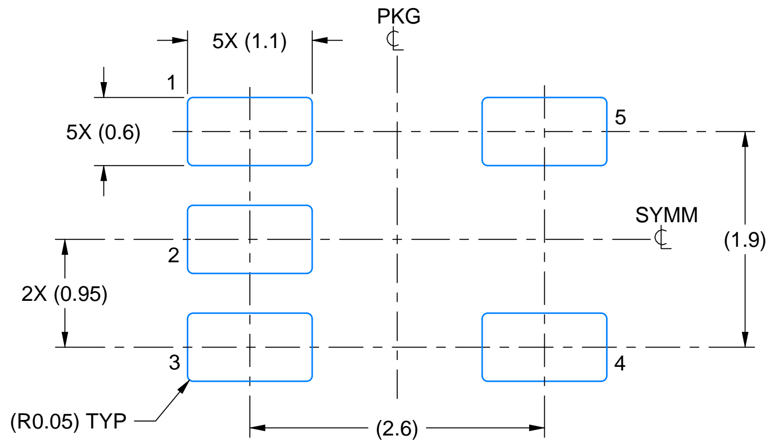


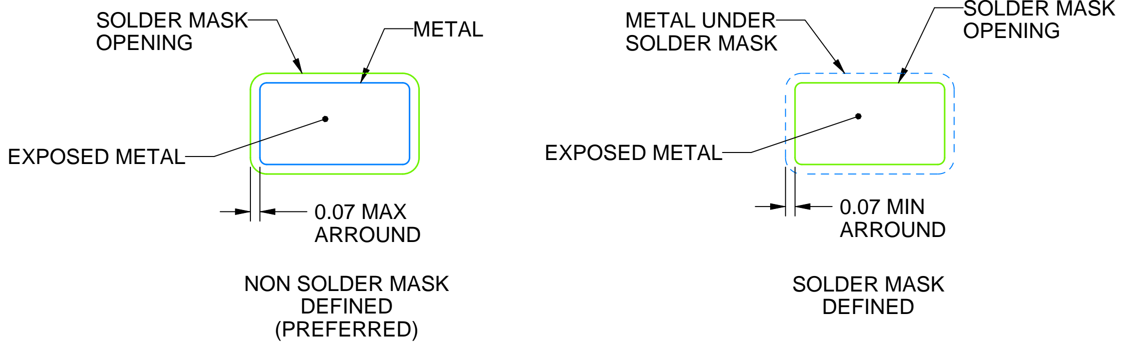

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




NON SOLDER MASK DEFINED (PREFERRED)

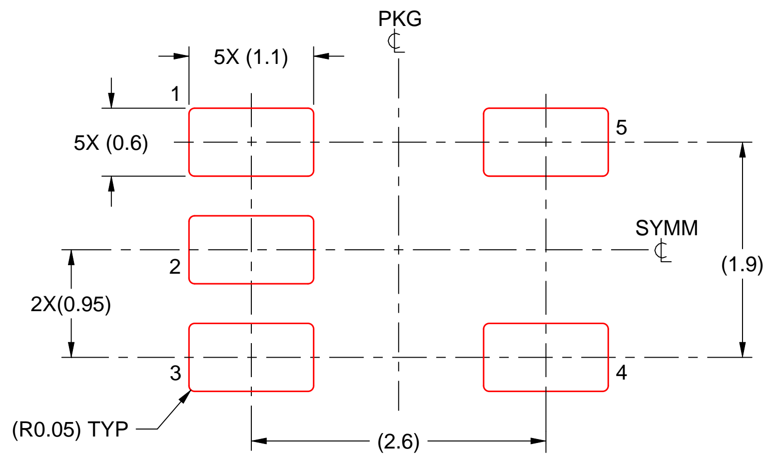
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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