MP8712

High-Efficiency, 12A, 3V-18V, Synchronous Step-Down Converter with Power Good, External Soft Start and OVP

The Future of Analog IC Technology

DESCRIPTION

The MP8712 is a high-frequency, synchronous, rectified, step-down, switch-mode converter. The MP8712 offers a fully integrated solution that achieves 12A of continuous and 15A of peak output current with excellent load and line regulation over a wide input supply range.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good pin (PG) indicates that the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8712 is available in a QFN-14 (3mmx4mm) package.

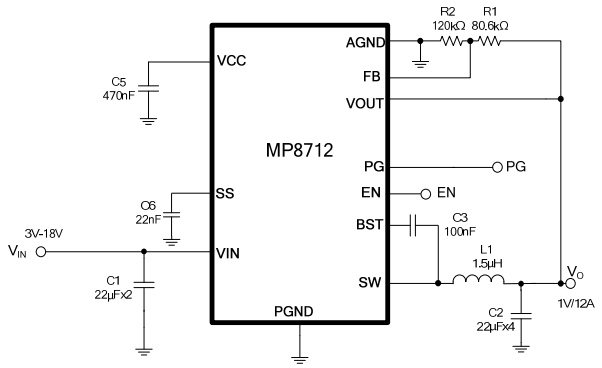
FEATURES

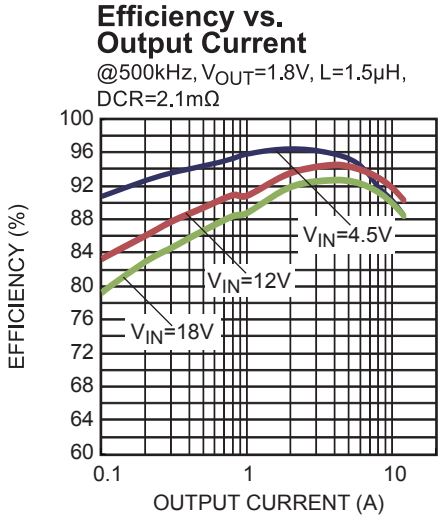
- Wide 3V to 18V Operating Input Range
- 12A Continuous/15A Peak Output Current
- 1% Internal Reference Accuracy
- Output Adjustable from 0.6V
- 15mΩ High-Side, 4.5mΩ Low-Side $R_{DS(ON)}$ for Internal Power MOSFETs
- 500kHz Switching Frequency
- External Soft Start (SS)
- Open-Drain Power Good (PG) Indication
- Output Over-Voltage Protection (OVP)
- Hiccup Over-Current Protection (OCP)
- Thermal Shutdown
- Available in a QFN-14 (3mmx4mm) Package

APPLICATIONS

- Solid-State Drives (SSD)
- Flat-Panel Televisions and Monitors
- Set-Top Boxes
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8712GL	QFN-14 (3mmx4mm)	*See Below*

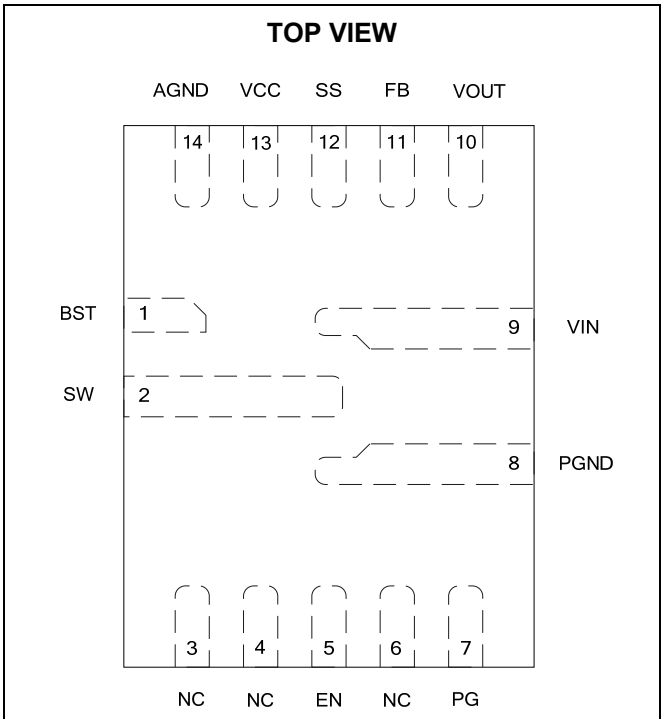
* For Tape & Reel, add suffix –Z (e.g. MP8712GL–Z)

TOP MARKING

MPYW
8712
LLL

MP: Product code of MP8712GL
Y: Year code
W: Week code
8712: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -0.3V to 19V
V_{SW} ..... -0.6V (-7V for <10ns) to VIN + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
VOUT 7V
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) (2)
QFN-14 (3mmx4mm) 2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 3V to 18V
Output voltage (VOUT) ..... 0.6V to 5.5V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance

QFN-14 (3mmx4mm)	***θ_{JA}***	***θ_{JC}***	
EV8712-L-00A	30	6	°C/W
JESD51-7 (4)	48	11	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Highly effective thermal conductivity test board for leaded surface-mount packages.

ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C [5], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2.1	4	μA
Supply current (quiescent)	I_Q	No switching, FB = 105% V_{REF}		420	600	μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		15		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 3.3V		4.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V, T_J = +25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}			14		A
Low-side negative current limit	I_{LIMIT_LN}	OVP state		-3		A
Low-side ZCD threshold	I_{ZCD}	T_J = +25°C		200		mA
Switching frequency	f_{SW1}	VIN = 12V, VOUT = 1V	400	500	600	kHz
	f_{SW2}	VIN = 12V, VOUT = 5V	400	500	600	kHz
Minimum off time [6]	T_{OFF_MIN}			185		ns
Minimum on time [6]	t_{ON_MIN}	VOUT = 0.6V		50		ns
Reference voltage	V_{ref}	T_J = 25°C	594	600	606	mV
		-40°C < T_J < 125°C [5]	591	600	609	
FB current	I_{FB}	VOUT = 620mV		10	50	nA
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}			1.5		MΩ
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		2.7	2.8	2.92	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			300		mV
Power good UV threshold rising	PGVth-Hi	Good	0.86	0.9	0.94	V_{OUT}
power good UV threshold falling	PGVth-Lo	Fault	0.81	0.85	0.89	V_{OUT}
Power good OV threshold rising	PGVth-Hi	Fault	1.11	1.15	1.19	V_{OUT}
Power good OV threshold falling	PGVth-Lo	Good	1.01	1.05	1.09	V_{OUT}
Power good deglitch time	PGTd			30		μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
OVP rising threshold	V_{OVP_Rise}	FB	121%	125%	129%	V_{REF}
OVP falling threshold	$V_{OVP\_Falling}$	FB	106%	110%	114%	V_{REF}
OVP delay	T_{OVP}			3.7		μs
Output pin absolute OV	V_{OVP2}		6.0	6.5	7.0	V
UVP threshold	$V_{FB\_UV\_th}$	Hiccup entry	55%	60%	65%	V_{REF}
UVP delay [6]	T_{UVP}			10		μs
Soft-start current	I_{SS}		5	7	9	μA

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to +125°C [5], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC voltage	V_{CC}			3.5		V
VCC load regulation	$V_{CC\ reg}$	I_{CC} = 20mA			3	%
Thermal shutdown [6]	T_{TSD}			160		°C
Thermal hysteresis [6]	$T_{TSD\ HYS}$			20		°C

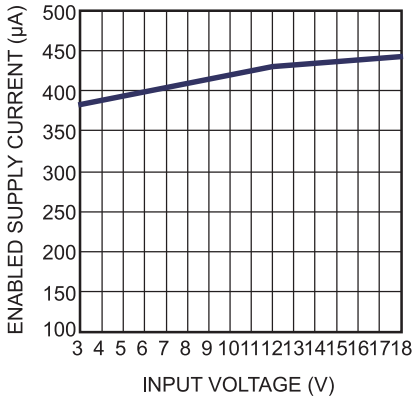
NOTES:

5) Not tested in production, guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization tests.

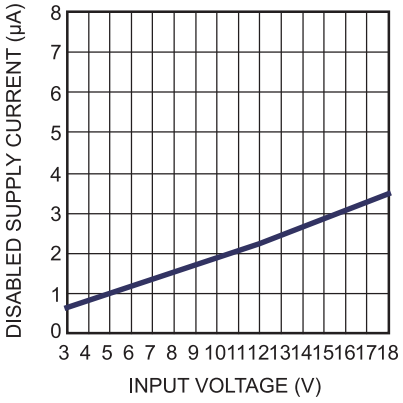
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

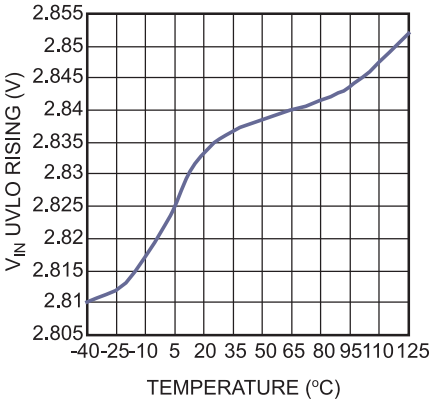
Enabled Supply Current vs. Input Voltage



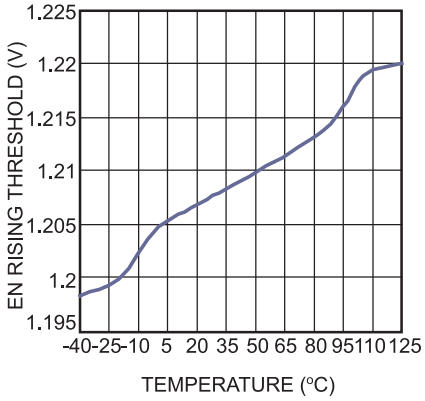
Disabled Supply Current vs. Input Voltage



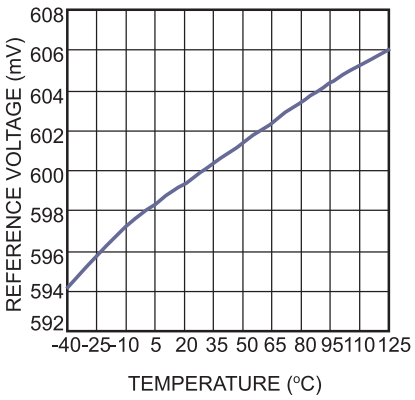
VIN UVLO Rising vs. Temperature



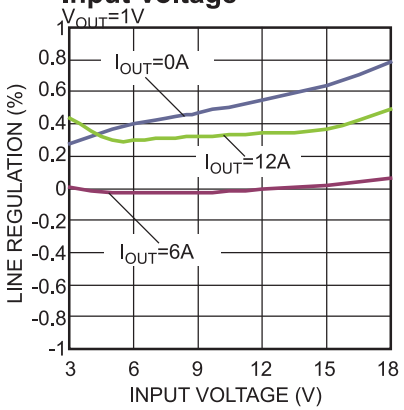
EN Rising Threshold vs. Temperature



Reference Voltage vs. Temperature

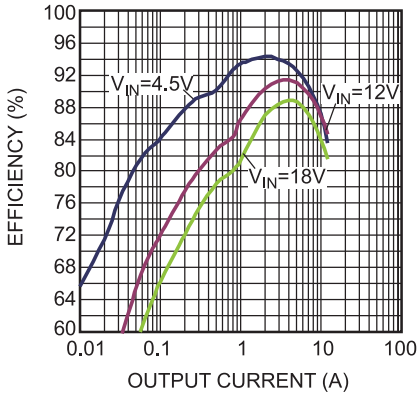


Line Regulation vs. Input Voltage



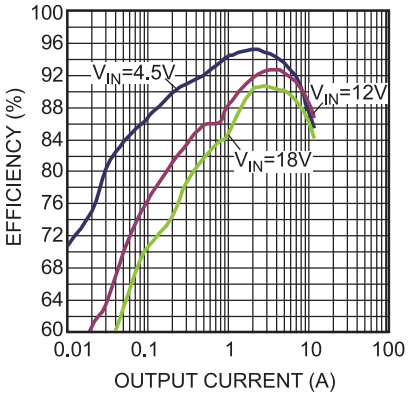
Efficiency vs. Output Current

V_{OUT}=1V, L=1.5µH, DCR=2.1mΩ



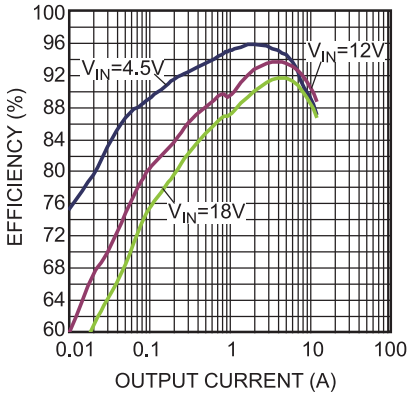
Efficiency vs. Output Current

V_{OUT}=1.2V, L=1.5µH, DCR=2.1mΩ



Efficiency vs. Output Current

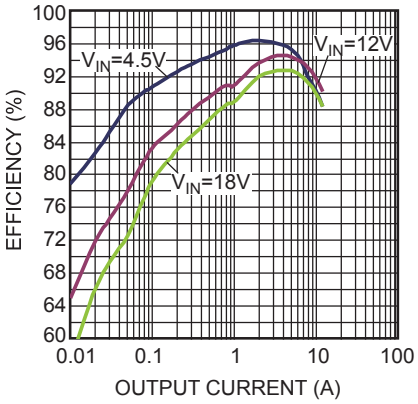
V_{OUT}=1.5V, L=1.5µH, DCR=2.1mΩ



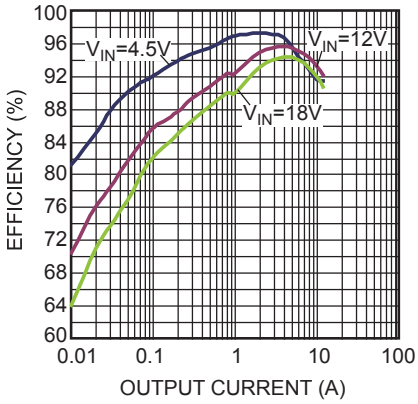
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

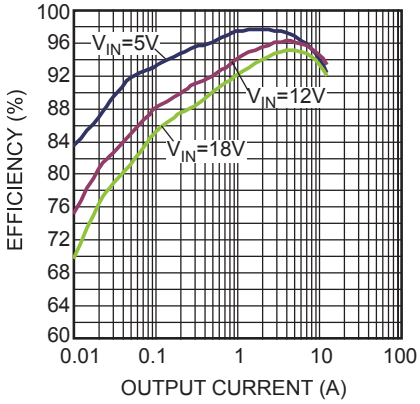
Efficiency vs. Output Current
V_{OUT}=1.8V, L=1.5µH, DCR=2.1mΩ



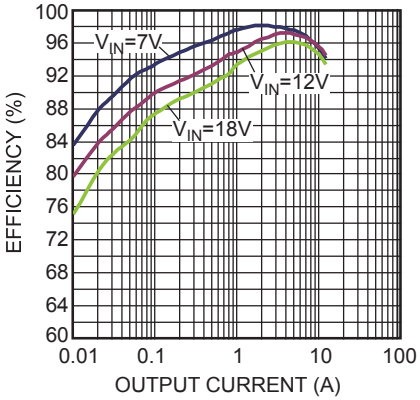
Efficiency vs. Output Current
V_{OUT}=2.5V, L=2.2µH, DCR=3mΩ



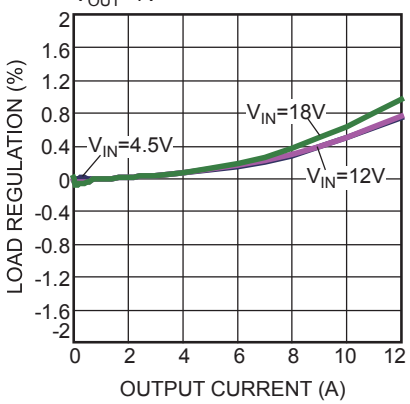
Efficiency vs. Output Current
V_{OUT}=3.3V, L=2.2µH, DCR=3mΩ



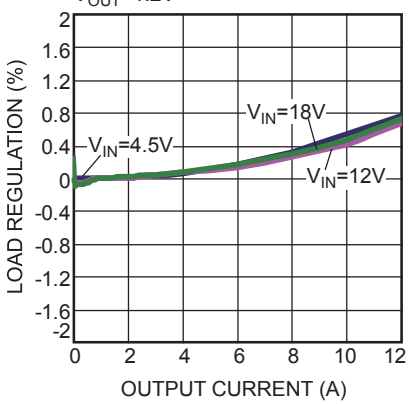
Efficiency vs. Output Current
V_{OUT}=5V, L=3.3µH, DCR=4.4mΩ



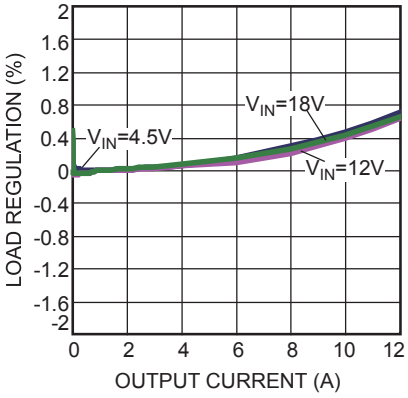
Load Regulation vs. Output Current
V_{OUT}=1V



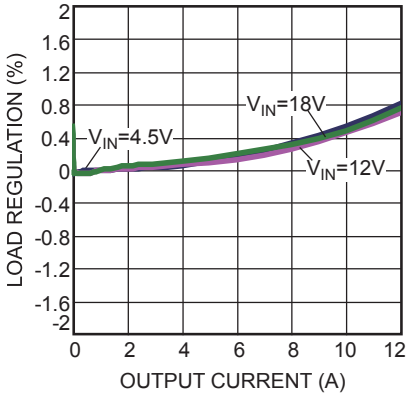
Load Regulation vs. Output Current
V_{OUT}=1.2V



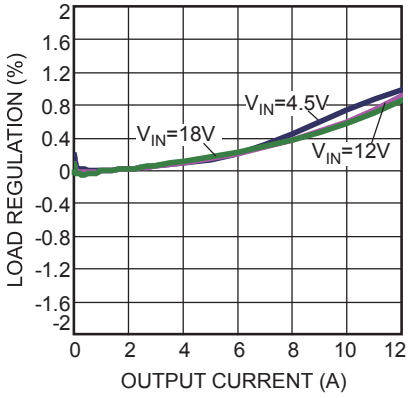
Load Regulation vs. Output Current
V_{OUT}=1.5V



Load Regulation vs. Output Current
V_{OUT}=1.8V



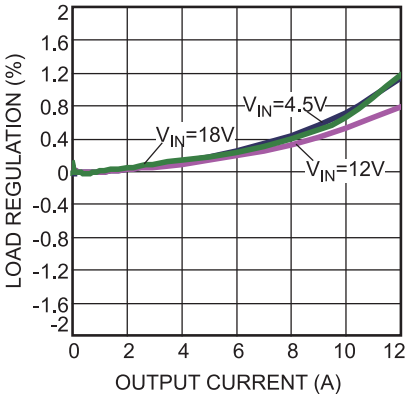
Load Regulation vs. Output Current
V_{OUT}=2.5V



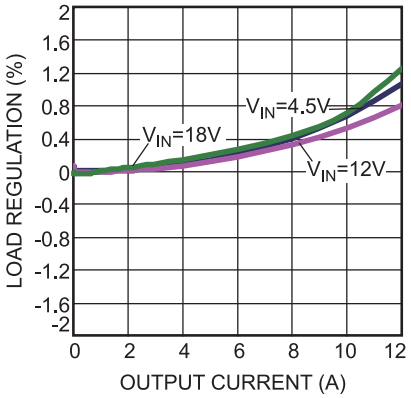
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

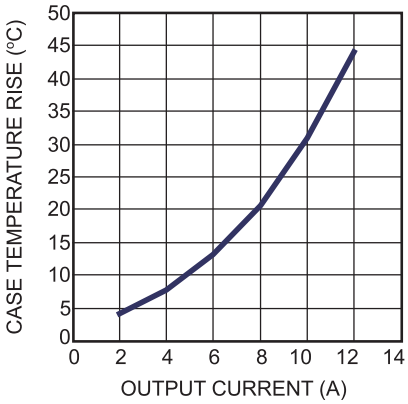
Load Regulation vs. Output Current
V_{OUT}=3.3V



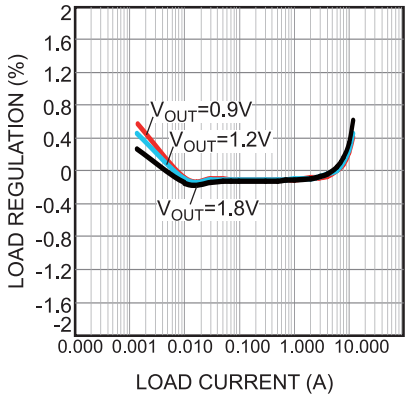
Load Regulation vs. Output Current
V_{OUT}=5V



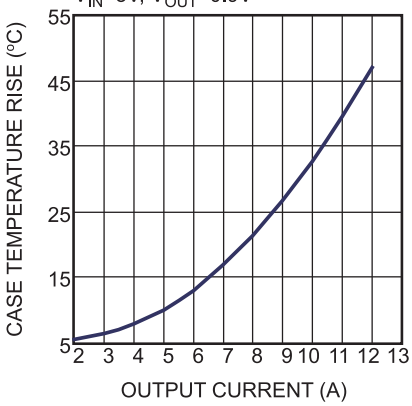
Case Temperature Rise vs. Output Current



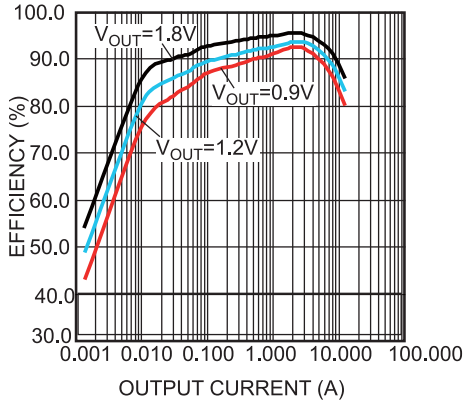
Load Regulation (%)
V_{IN}=3V, V_{OUT}=0.9V



Case Temperature Rise vs. Output Current
V_{IN}=3V, V_{OUT}=0.9V



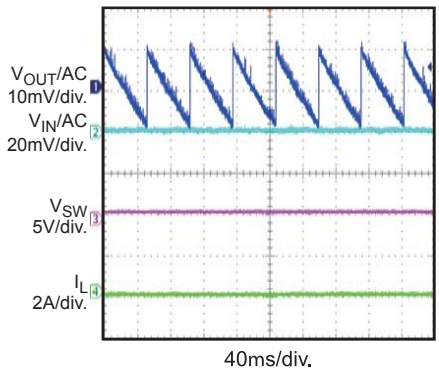
Efficiency Curve
V_{IN}=3V



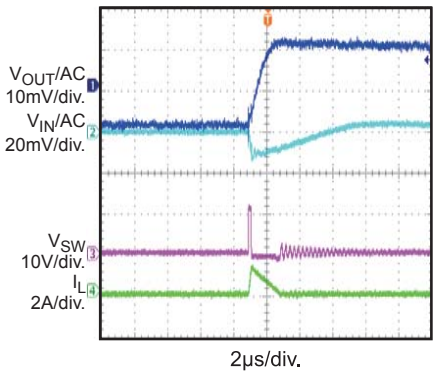
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

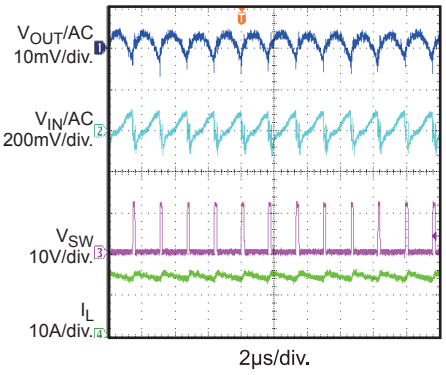
Input/Output Ripple
I_{OUT} = 0A



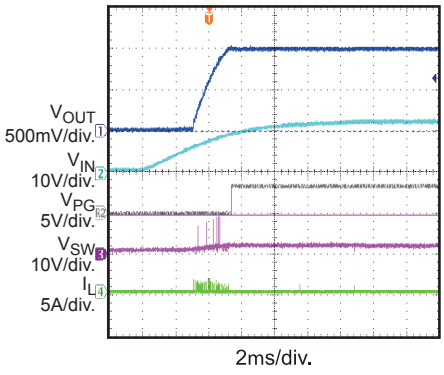
Input/Output Ripple
I_{OUT} = 0A



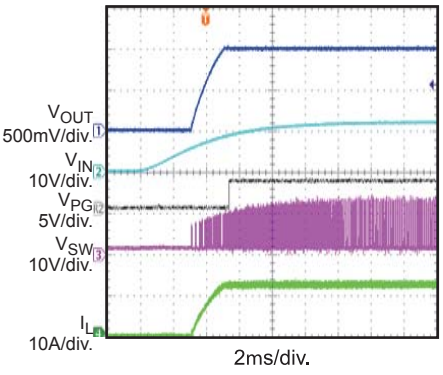
Input/Output Ripple
I_{OUT} = 12A



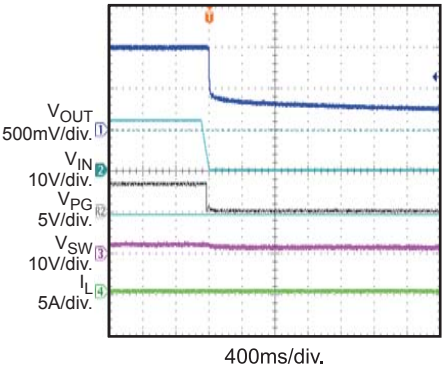
Start-Up through Input Voltage
I_{OUT} = 0A



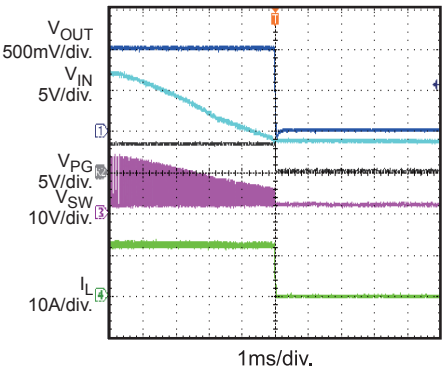
Start-Up through Input Voltage
I_{OUT} = 12A



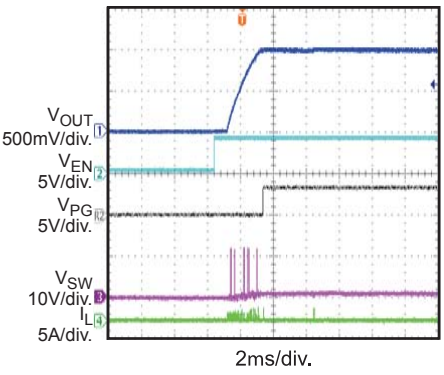
Shutdown through Input Voltage
I_{OUT} = 0A



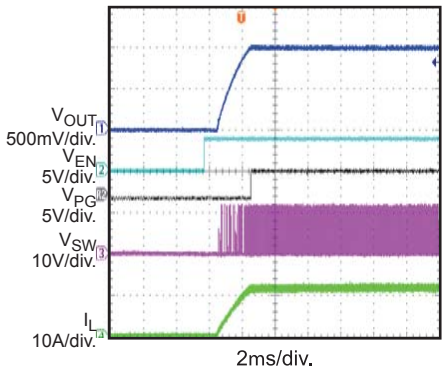
Shutdown through Input Voltage
I_{OUT} = 12A



Start-Up through EN
I_{OUT} = 0A



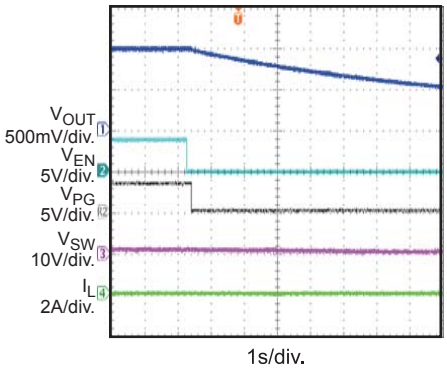
Start-Up through EN
I_{OUT} = 12A



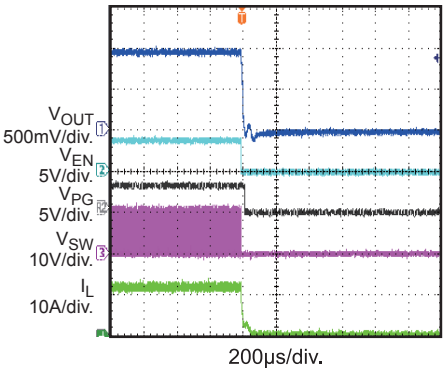
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

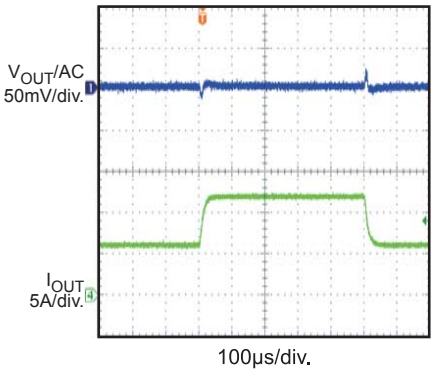
Shutdown through EN
I_{OUT} = 0A



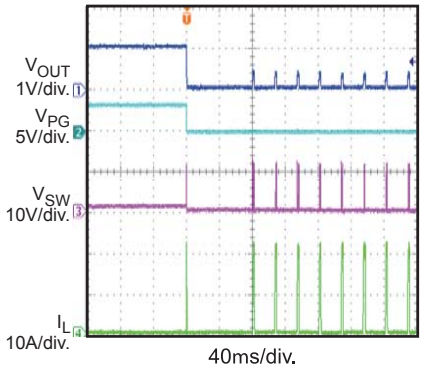
Shutdown through EN
I_{OUT} = 12A



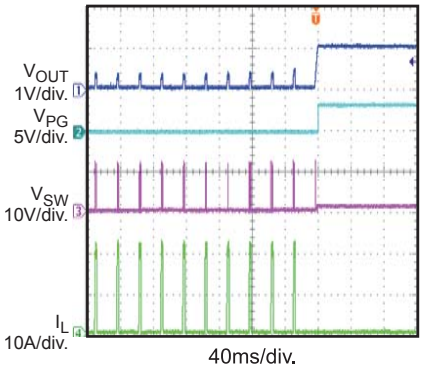
Load Transient
I_{OUT} = 6A-12A



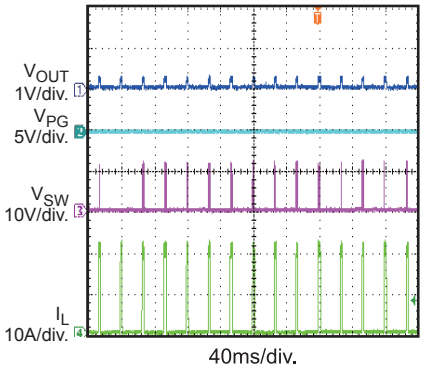
Short-Circuit Protection Entry
I_{OUT} = 0A



Short-Circuit Protection Recovery
I_{OUT} = 0A



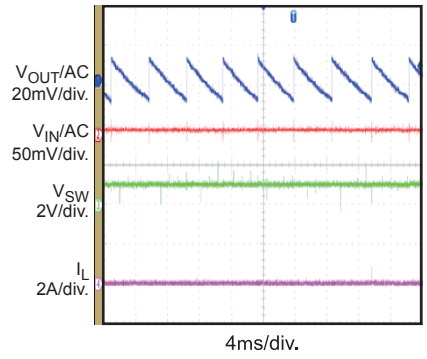
Short-Circuit Protection Steady State
Short Output to GND



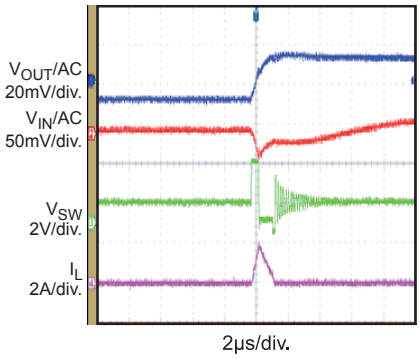
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 3V, VOUT = 0.9V, L = 0.47µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

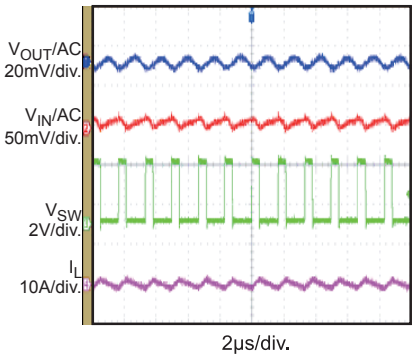
Input/Output Ripple
I_{OUT} = 0A



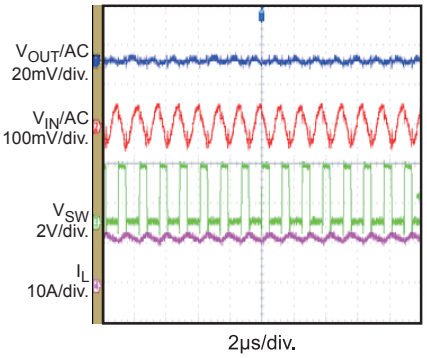
Input/Output Ripple
I_{OUT} = 0A



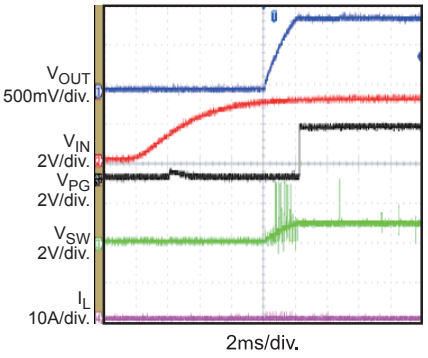
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



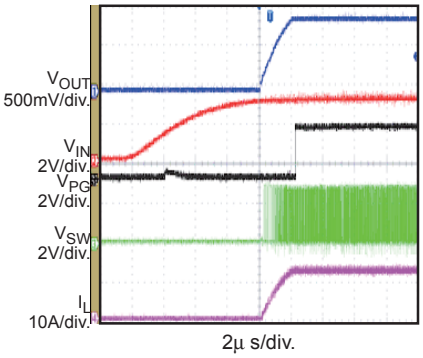
Input/Output Ripple
I_{OUT} = 12A



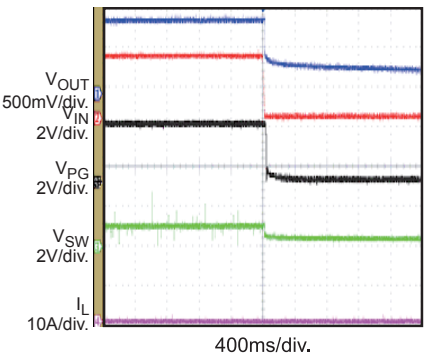
Start-Up through Input Voltage
I_{OUT} = 0A



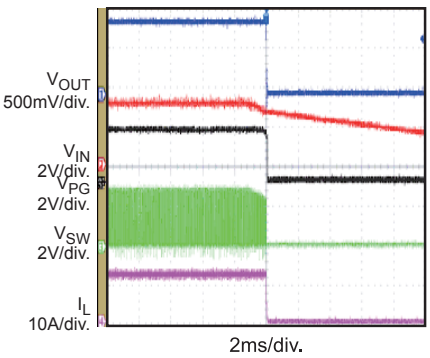
Start-Up through Input Voltage
I_{OUT} = 12A



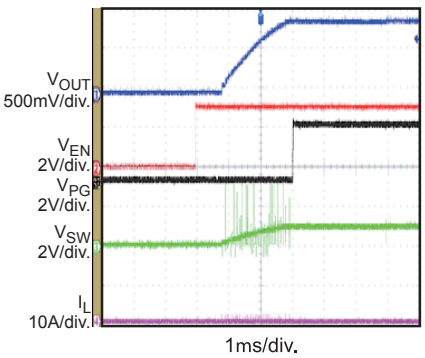
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



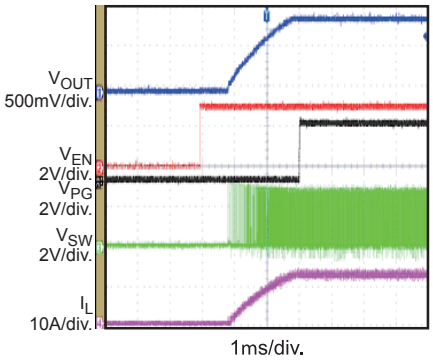
Start-Up through EN
I_{OUT} = 0A



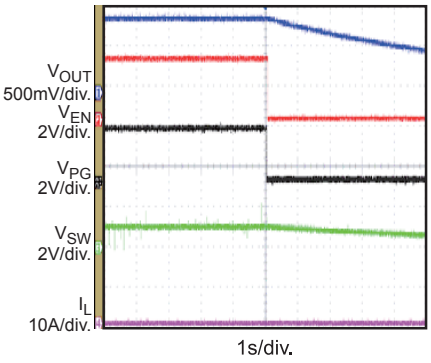
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 3V, VOUT = 0.9V, L = 0.47µH, F_S = 500kHz, T_A = 25°C, unless otherwise noted.

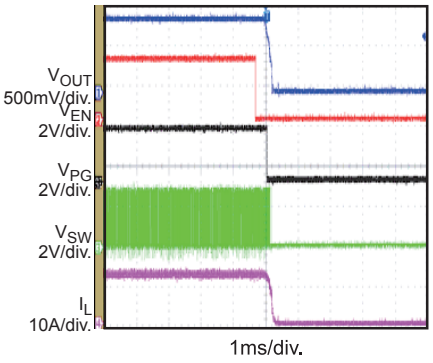
Start-Up through EN
I_{OUT} = 12A



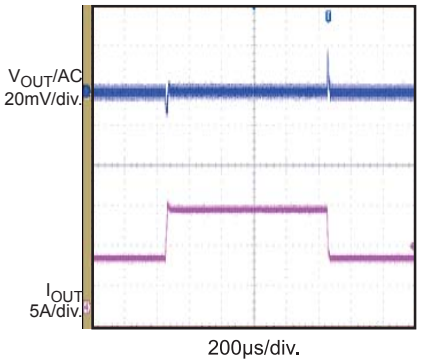
Shutdown through EN
I_{OUT} = 0A



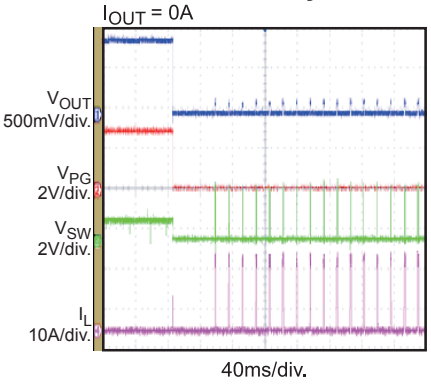
Shutdown through EN
I_{OUT} = 12A



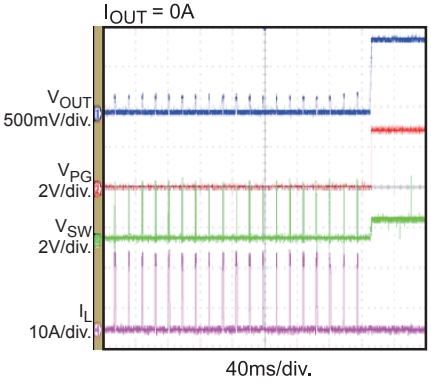
Load Transient
I_{OUT} = 6A-12A



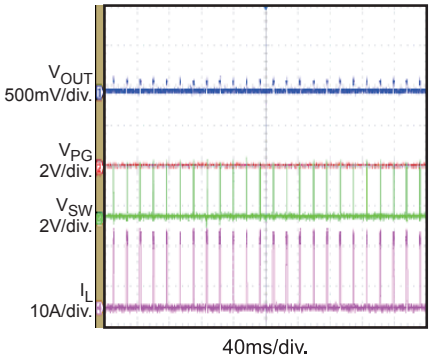
Short-Circuit Protection Entry
I_{OUT} = 0A



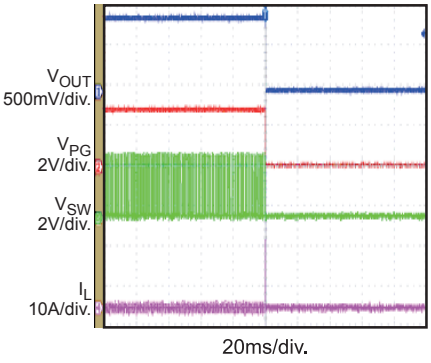
Short-Circuit Protection Recovery
I_{OUT} = 0A



Short-Circuit Protection Steady State
Short Output to GND



Short-Circuit Protection Entry, Latch Off Mode
I_{OUT}=0A



PIN FUNCTIONS

QFN-14 Pin#	Name	Description
1	BST	**Bootstrap.** A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output.** Connect using a wide PCB trace.
3, 4, 6	NC	**No connection.** Leave NC floating.
5	EN	**Enable.** Drive EN high to enable the MP8712. EN has a 1.5MΩ internal pull-down resistor to GND. EN is a high-voltage pin and can be connected to VIN directly for auto start-up.
7	PG	**Power good indication.** PG is an open-drain structure. PG is de-asserted if the output voltage is out of the regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage. PGND requires special consideration during the PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8712 operates from a 3V to 18V input rail. VIN requires a ceramic capacitor to decouple the input rail. Connect VIN using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive terminal of the load.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.
12	SS	**Soft start set-up.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple VCC with a 0.47μF capacitor.
14	AGND	**Signal ground.** AGND is not connected to PGND internally. Ensure that AGND is connected to PGND in the PCB layout.

BLOCK DIAGRAM

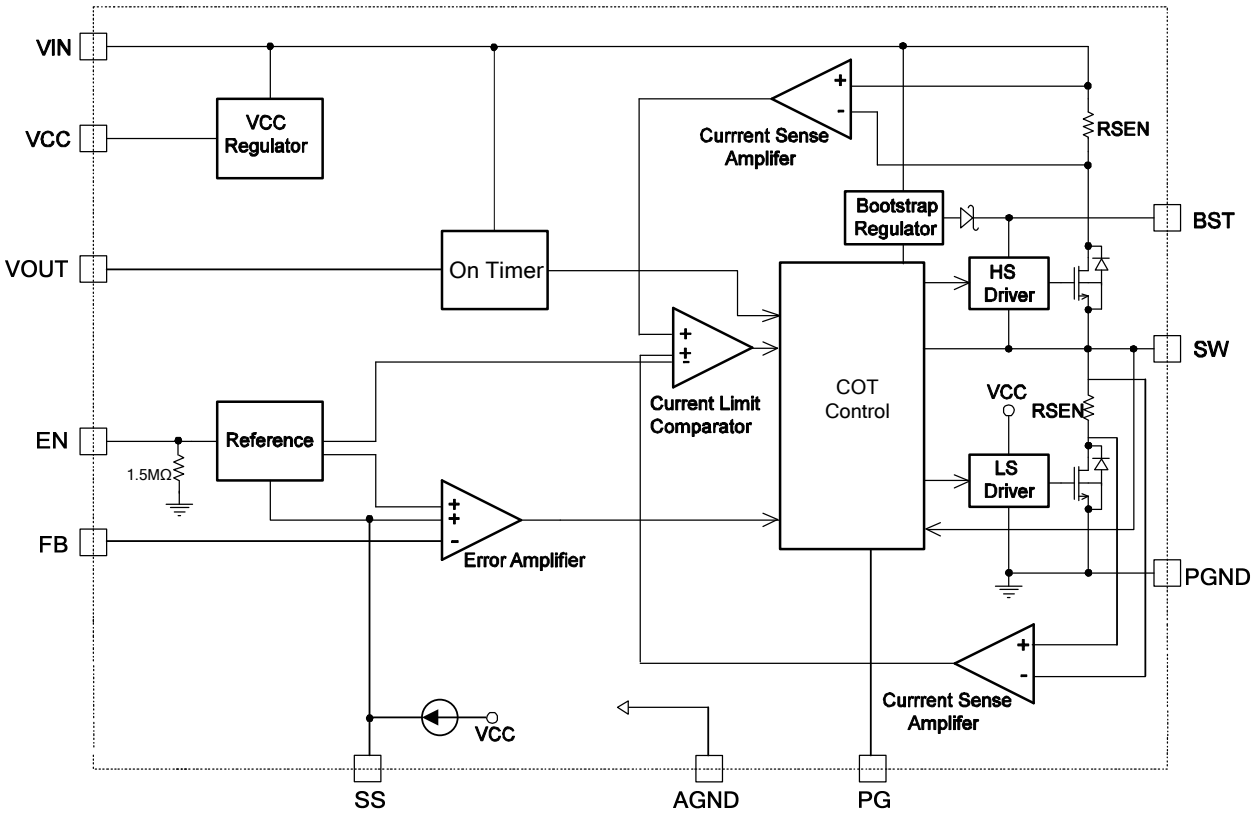


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The MP8712 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The MP8712 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 2 shows the simplified ramp compensation block. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{RAMP}) is lower than the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between the input and GND. Shoot-through reduces efficiency dramatically, so the MP8712 prevents this by generating a dead time (DT) internally between the HS-FET off and LS-FET on time and the LS-FET off and HS-FET on time. The MP8712 enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

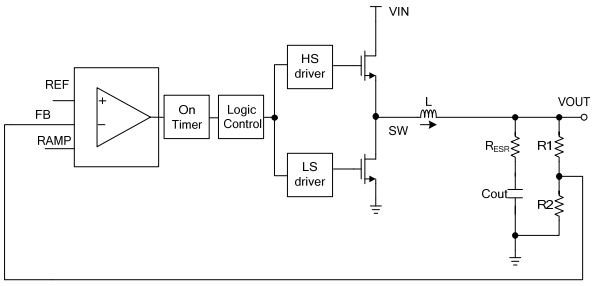


Figure 2: Simplified Compensation Block

Switching Frequency

The MP8712 uses COT control. There is no dedicated oscillator in the IC. The input voltage is forward fed to the one-shot on-timer through the internal frequency resistor. The duty ratio is kept as VOUT/VIN, and the switching frequency is a fairly constant 500kHz over the input voltage range.

Light-Load Operation

When the MP8712 works in light-load operation, the MP8712 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 3). The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when the output current is low.

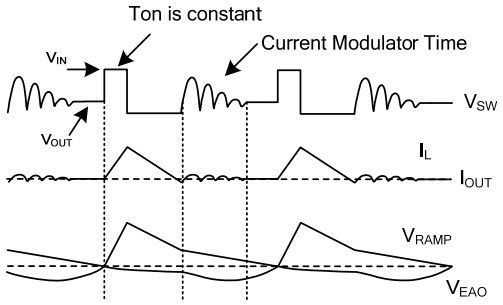


Figure 3: Light-Load Operation

Light-load operation is also called skip mode since the HS-FET does not turn on as frequently as it does during heavy-load condition. The HS-FET turn-on frequency is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases as well. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The MP8712 enters pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Operating without an External Ramp

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors

usually cannot be used as output capacitors. The MP8712 has built-in internal ramp compensation to ensure that the system is stable even without the help of the output capacitor's ESR. A pure ceramic capacitor solution can reduce output ripple, total BOM cost, and board area significantly.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 470nF decoupling capacitor is needed to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates in the full VIN range. After EN is pulled high and VIN is greater than 3.5V, the output of the regulator is in full regulation. When VIN is lower than 3.5V, the output voltage decreases and follows the input voltage. A 0.47μF ceramic capacitor is required for decoupling purposes.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage against the internal 0.6V reference (REF) and outputs a PWM signal. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be connected to VIN directly for automatic start-up.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8712 UVLO comparator monitors both the input voltage (VIN) and the output voltage (VOUT) of the VCC regulator. The MP8712 is active when both voltages exceed the UVLO rising threshold.

Soft Start (SS) and Pre-Bias Start-Up

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The approximate typical soft-start time can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{V_{ref}(V) \times C_{ss}(nF)}{7\mu A} \quad (2)$$

If the output of the MP8712 is pre-biased to a certain voltage during start-up, the IC disables the switching of the high-side and low-side until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at FB.

Over-Current Protection (OCP)

The MP8712 has hiccup, cycle-by-cycle, and over-current limiting control. The current-limit circuit employs both the high-side current limit and the low-side (valley) current-sensing algorithm. The MP8712 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal is above the current-limit threshold, the PWM on pulse is terminated, and the low side is turned on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until VOUT is below the under-voltage (UV) threshold, typically 60% below the reference. Once UV is triggered, the MP8712 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP8712 exits hiccup mode once the over-current condition is removed.

Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is needed. During power-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current at start-up.

When the output voltage is between 90% and 115% of the nominal voltage and the soft start is finished, the PG signal is pulled high. When the output voltage is lower than 85% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the nominal voltage, PG is switched low. The PG signal rises high again after the output voltage drops below 105% of the nominal voltage.

PG uses a deglitch time whenever VOUT crosses the UV/OV rising and falling threshold. The PG output is pulled low immediately when either EN UVLO, input UVLO, OCP, or OTP is triggered.

Input Over-Voltage Protection (VIN OVP)

The MP8712 monitors VIN to detect an input over-voltage (OV) event. This function is only active when the output is in OV. When the output is in an over-voltage protection (OVP) state, output discharge is enabled, charging the input voltage high. When the input voltage exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MP8712 monitors FB to detect an over-voltage event. When the FB voltage becomes higher than 125% of the internal reference voltage, the controller enters dynamic regulation mode, and the input voltage may be charged up during this time. When input OVP is triggered, the IC stops switching. Once the input voltage drops below the VIN OVP recovery threshold, the IC begins switching. OVP auto-retry mode occurs only if the soft start finishes.

Dynamic regulation mode is defined as turning on the low side until the low-side negative current limit is triggered, and then the body diode of the HS-FET freewheels the current. The output power charges to the input, which may trigger a VIN OVP function. In VIN OVP, neither the HS-FET or LS-FET turn on and stop charging VIN to a higher voltage. If the output is still over-voltage and the input voltage has dropped below the VIN OVP threshold, repeat dynamic regulation mode. If the output voltage is lower than 110% of the internal reference voltage, then output OVP is exited.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MP8712 monitors VOUT to detect absolute over-voltage protection. When VOUT is larger than 6.5V, the controller enters dynamic regulation mode. Absolute OVP can work once both the input voltage and EN are higher than their rising thresholds. Therefore, this function can work even in a soft-start period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (typically 140°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.4V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1, and C2 (see Figure 4). If V_{BST} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

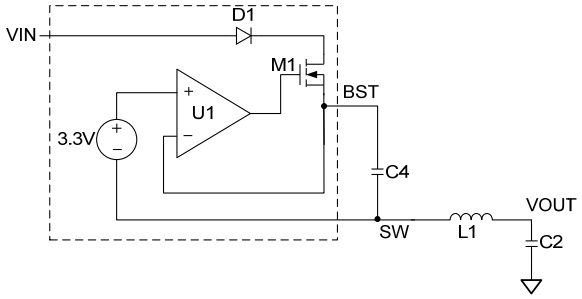


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries. Several events can shut down the chip: EN low, VIN low, VCC low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to prevent any fault triggering. V_{EAO} and the internal supply rail are then pulled down.

APPLICATION INFORMATION

Setting the Output Voltage

The MP8712 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.6V.

The feedback network is shown in Figure 5.

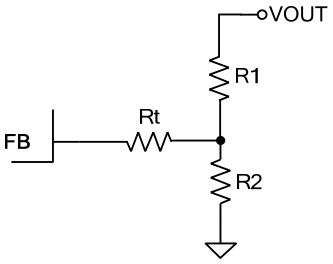


Figure 5: Feedback Network

Choose R1 and R2 using Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	L (μH)
1.0	80.6	120	10	1.5
1.2	80.6	80.6	10	1.5
1.5	80.6	53.6	10	1.5
1.8	80.6	40.2	10	1.5
2.5	80.6	25.5	10	2.2
3.3	80.6	17.8	10	2.2
5	80.6	11	10	3.3

NOTE:

7) The recommended parameters are based on a 12V input voltage and 22μFx4 output capacitor. Different input voltage and output capacitor values may affect the selection of R1 and R2. For other component parameters, please refer to the Typical Application Circuits on page 22 to page 25.

Selecting the Inductor

For most applications, use a 0.47μH to 5μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a DC resistance less than 5mΩ.

For most designs, the inductance value can be derived from Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22μF capacitors. Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8712 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- VOUT is 5V or 3.3V
- Duty cycle is high: D > 50%

In these cases, add an external BST diode from VCC to BST (see Figure 6).

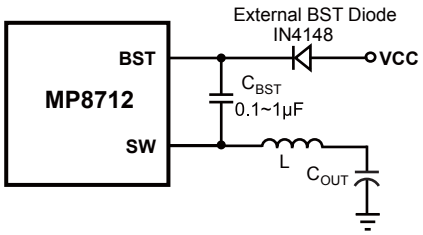


Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is 1N4148, and the recommended BST capacitor value is 0.1μF to 1μF.

Connecting VCC to VIN at a Low Input Voltage

VCC can be connected to VIN directly when VIN is lower than 3.5V. This helps improve the MP8712's low input voltage efficiency performance. To use this application set-up, the VIN spike voltage must be limited below 4V; otherwise, VCC could be damaged.

PCB Layout Guidelines [8]

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 7 and follow the guidelines below.

1. Place the high current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large coppers.
3. Use at least two layers for the VIN and PGND trace to achieve better thermal performance.
4. Add several vias close to the VIN and PGND pads to help with thermal dissipation.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Place the external feedback resistors next to FB.
8. Ensure that there is no via on the FB trace.
9. Keep the switching node (SW) short and away from the feedback network.
10. Keep the BST voltage path (BST, C3, and SW) as short as possible.

NOTE:

8) The recommended layout is based on the Typical Application Circuits on page 22 to page 25.

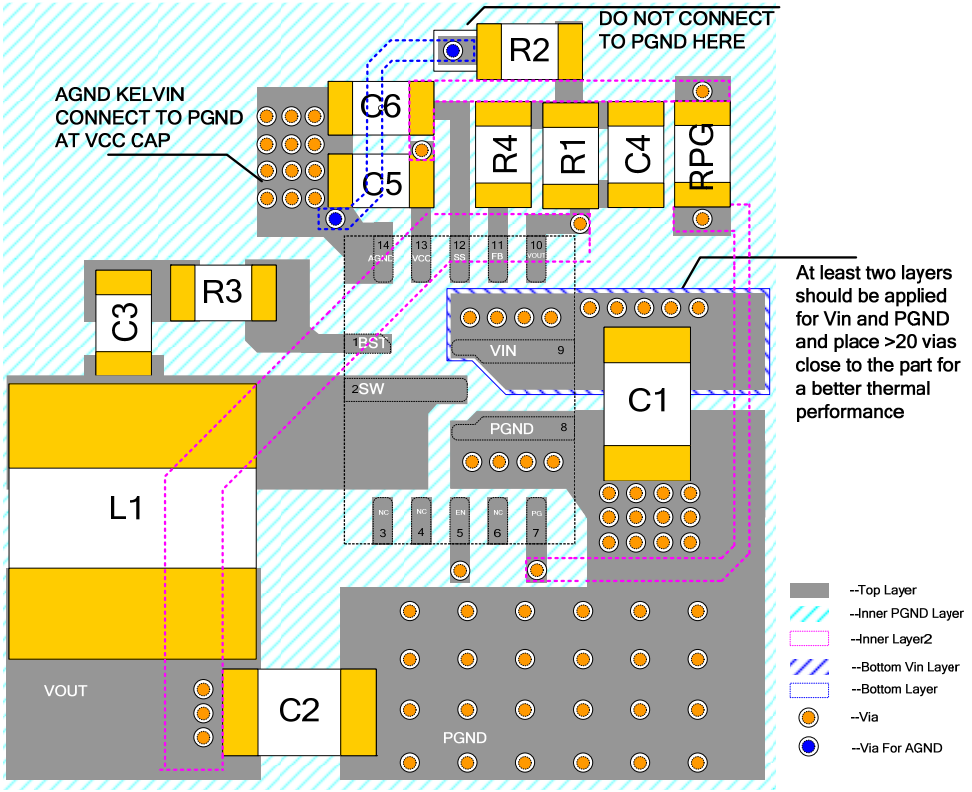


Figure 7: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications.

Table 2: Design Example

V_{IN}	12V, 3V
V_{OUT}	1V
I_{OUT}	12A

The detailed application schematics are shown in Figure 8 through Figure 17. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

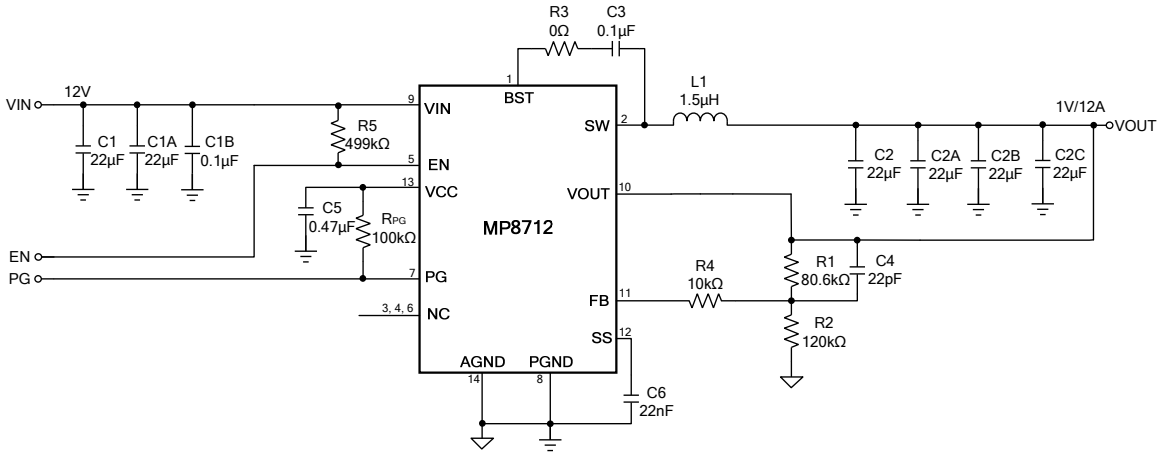


Figure 8: VIN = 12V, VOUT = 1V, I_{OUT} = 12A

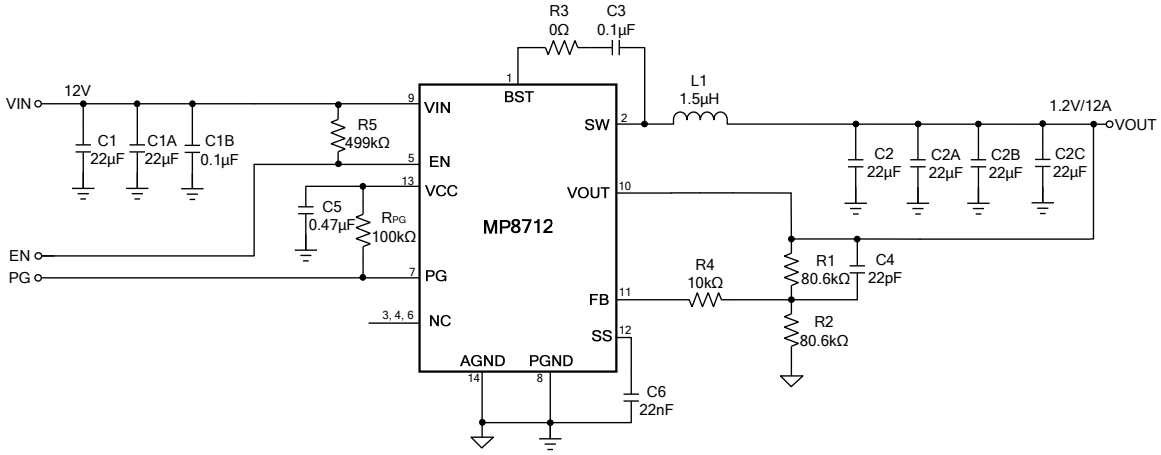


Figure 9: VIN = 12V, VOUT = 1.2V, I_{OUT} = 12A

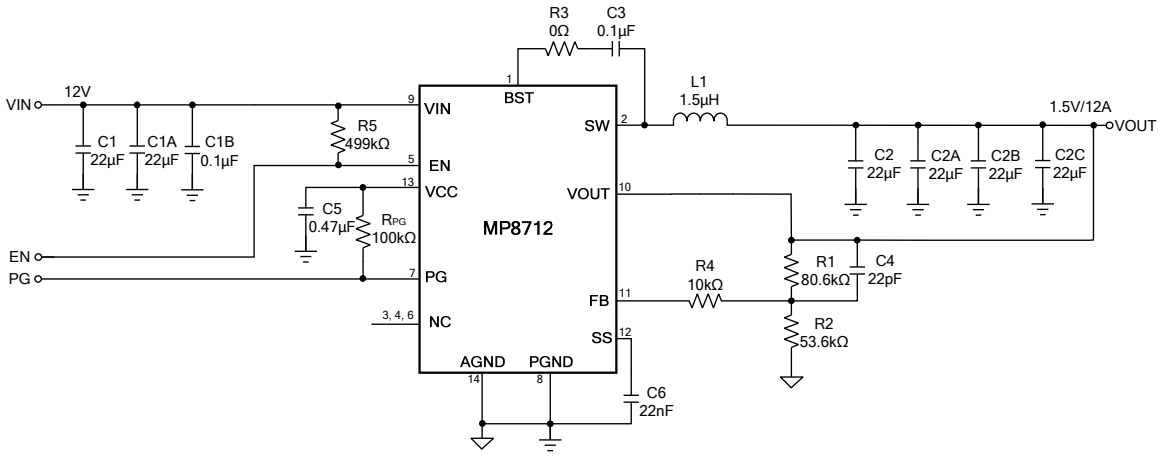


Figure 10: VIN = 12V, VOUT = 1.5V, I_{OUT} = 12A

TYPICAL APPLICATION CIRCUITS *(continued)*

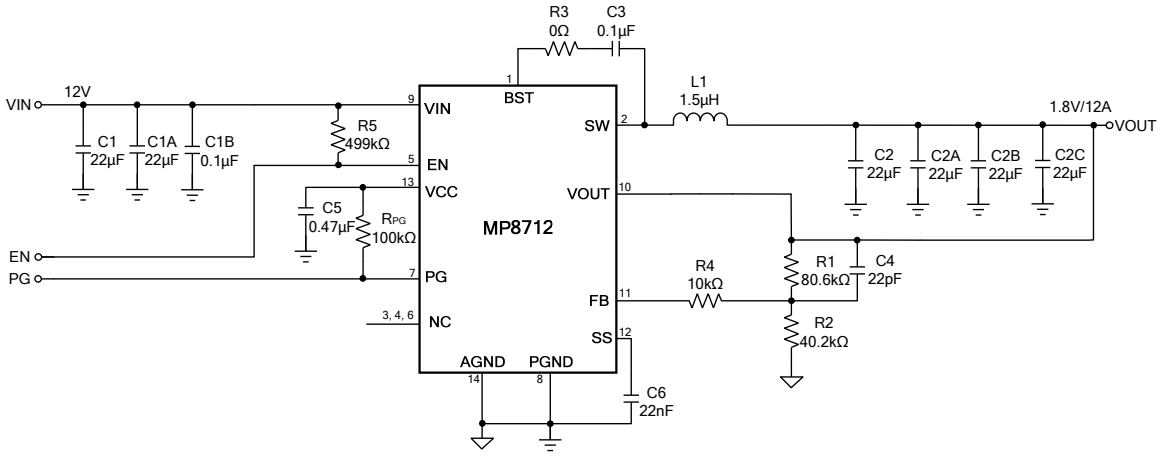


Figure 11: VIN = 12V, VOUT = 1.8V, I_{OUT} = 12A

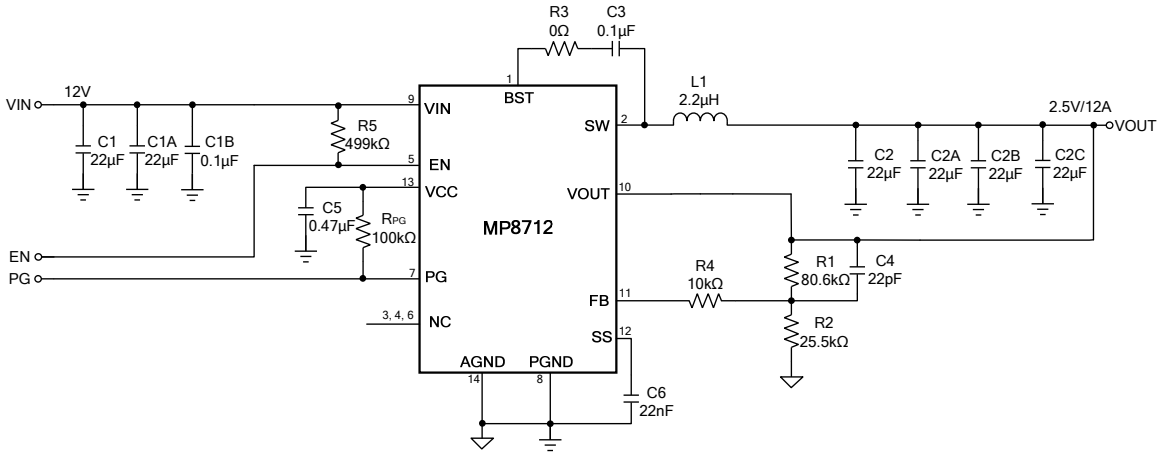


Figure 12: VIN = 12V, VOUT = 2.5V, I_{OUT} = 12A

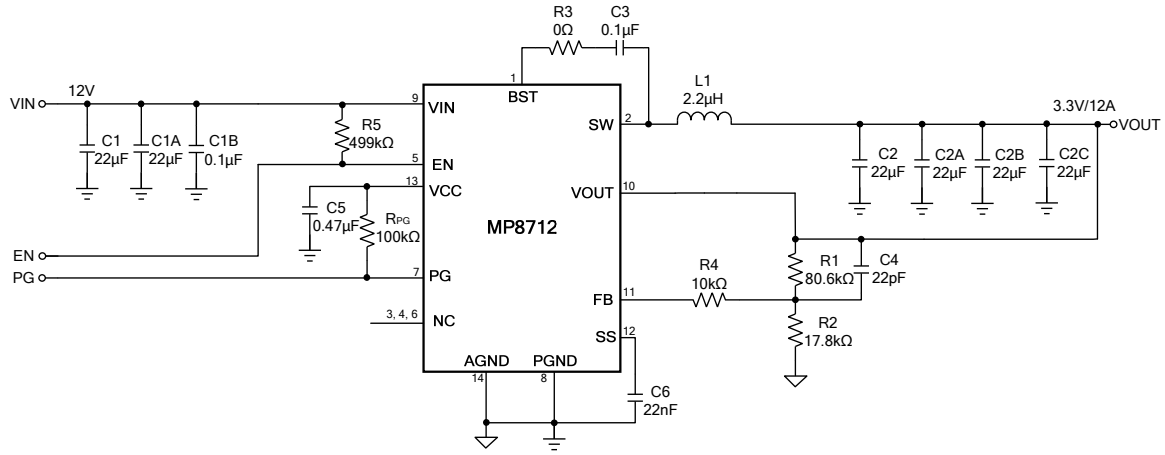


Figure 13: VIN = 12V, VOUT = 3.3V, I_{OUT} = 12A

TYPICAL APPLICATION CIRCUITS *(continued)*

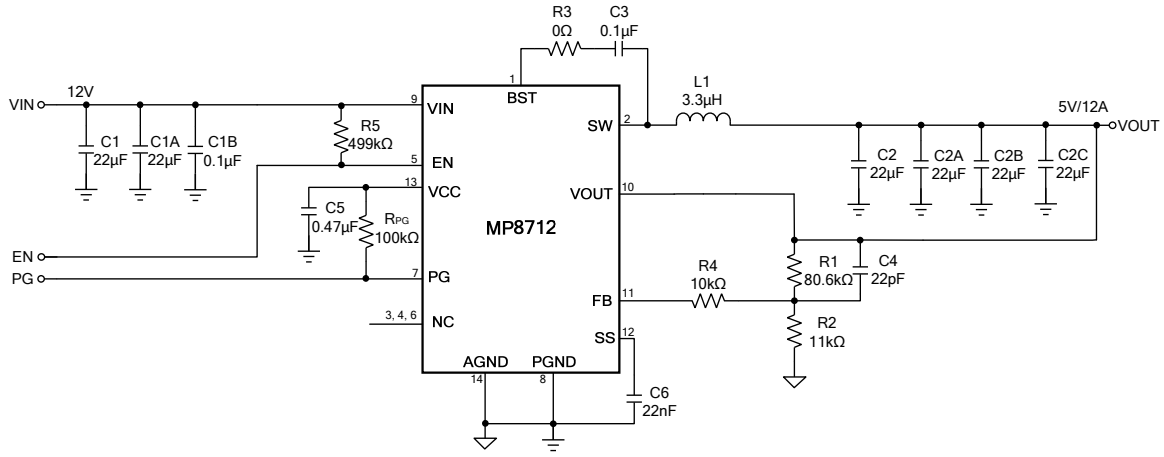


Figure 14: VIN = 12V, VOUT = 5V, I_{OUT} = 12A [9]

NOTE:

9) Based on the evaluation board test result at 25°C ambient temperature. A lower input voltage will trigger over-temperature protection with full load.

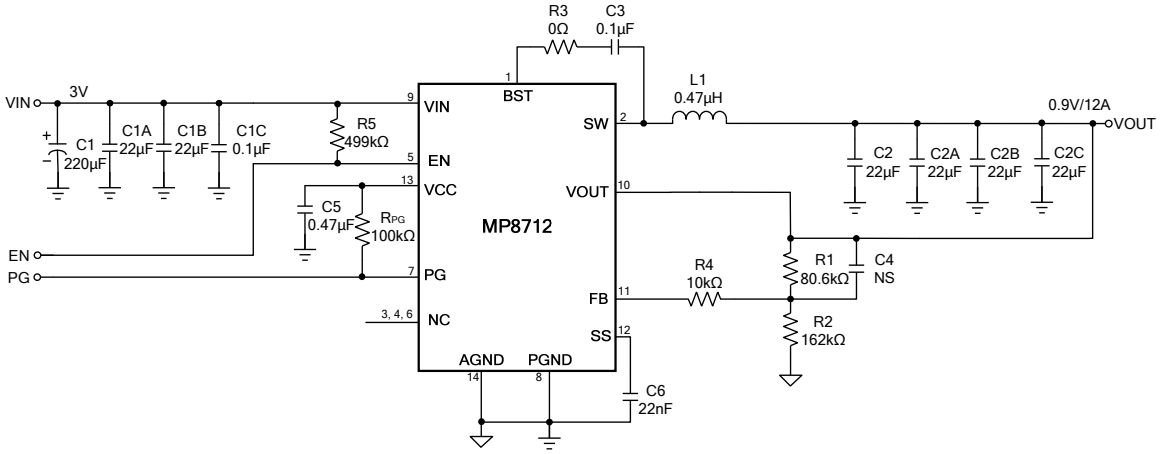


Figure 15: VIN = 3V, VOUT = 0.9V, I_{OUT} = 12A

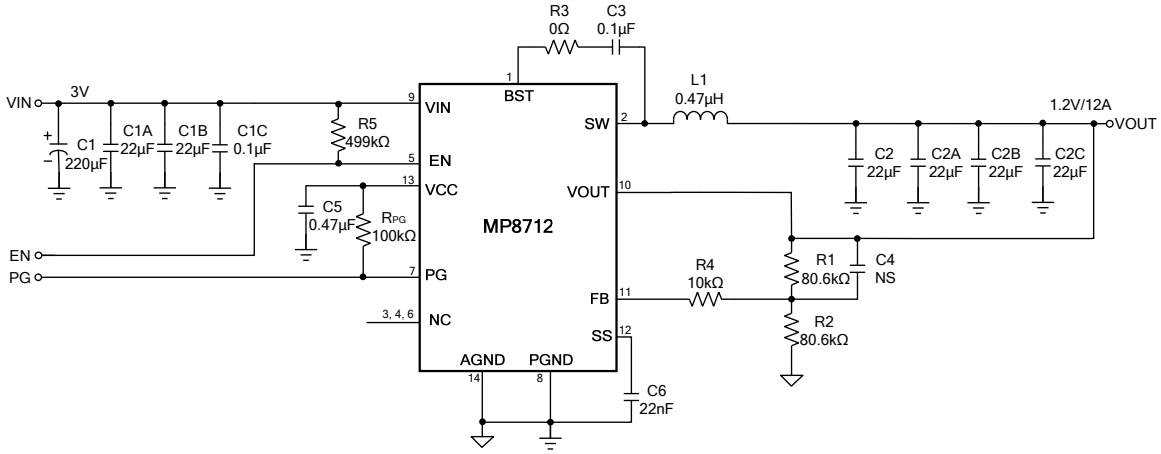


Figure 16: VIN = 3V, VOUT = 1.2V, I_{OUT} = 12A

TYPICAL APPLICATION CIRCUITS *(continued)*

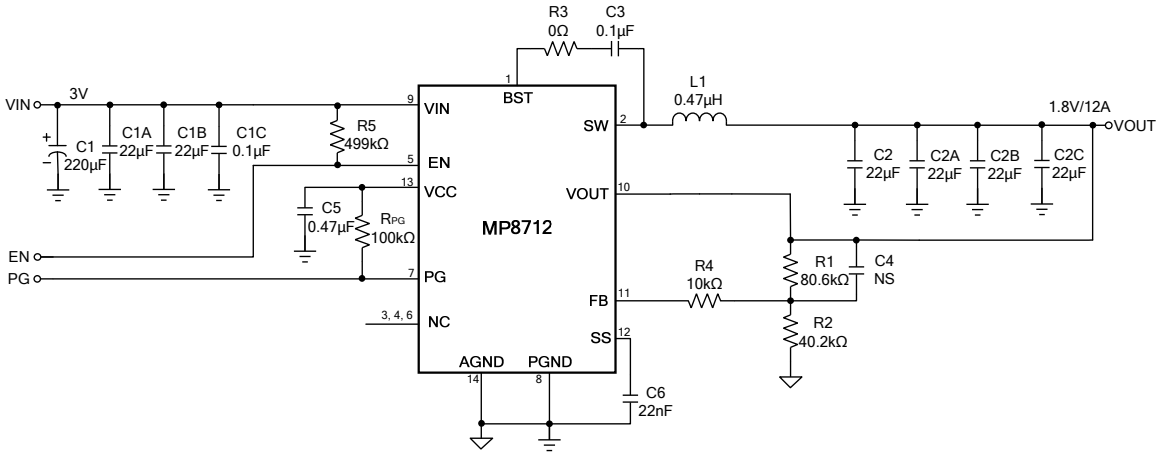
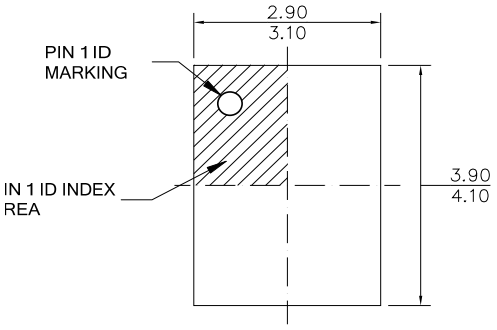


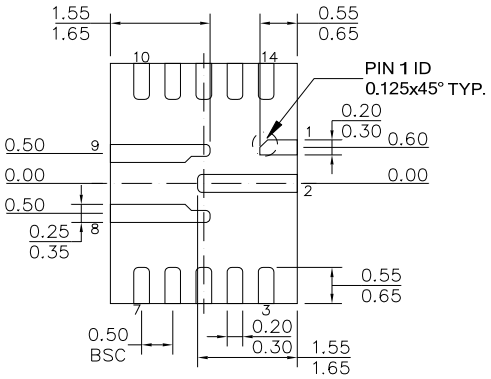
Figure 17: VIN = 3V, VOUT = 1.8V, I_{OUT} = 12A

PACKAGE INFORMATION

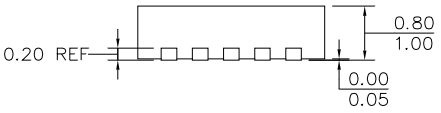
QFN-14 (3mmx4mm)



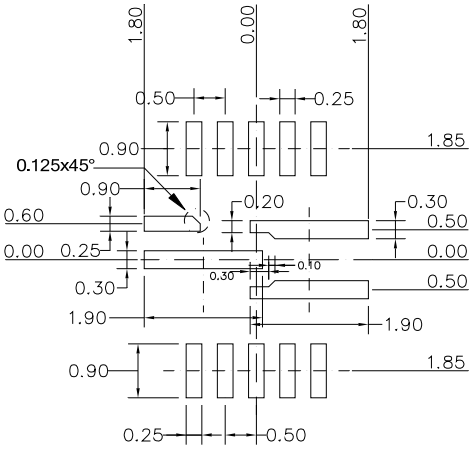
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.