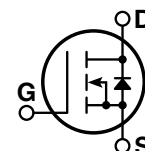
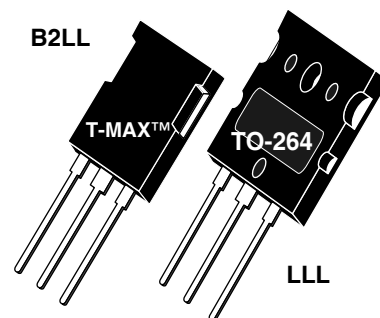


POWER MOS 7® MOSFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- Popular T-MAX™ or TO-264 Package



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT50M75B2LL_LLL	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	57	Amps
I_{DM}	Pulsed Drain Current ^①	228	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	570	Watts
	Linear Derating Factor	4.56	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	57	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	2500	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 28.5A$)			0.075	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 500V, V_{GS} = 0V$)			100	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 400V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 2.5mA$)	3		5	Volts



CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT50M75B2LL LLL(G)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		5590		pF
C_{oss}	Output Capacitance			1180		
C_{rss}	Reverse Transfer Capacitance			85		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 250V$ $I_D = 57A @ 25^\circ C$		125		nC
Q_{gs}	Gate-Source Charge			33		
Q_{gd}	Gate-Drain ("Miller") Charge			65		
$t_{d(on)}$	Turn-on Delay Time	RESISTIVE SWITCHING $V_{GS} = 15V$ $V_{DD} = 250V$ $I_D = 57A @ 25^\circ C$ $R_G = 0.6\Omega$		8		ns
t_r	Rise Time			19		
$t_{d(off)}$	Turn-off Delay Time			21		
t_f	Fall Time			3		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C $V_{DD} = 333V, V_{GS} = 15V$ $I_D = 57A, R_G = 5\Omega$		755		μJ
E_{off}	Turn-off Switching Energy			725		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C $V_{DD} = 333V, V_{GS} = 15V$ $I_D = 57A, R_G = 5\Omega$		1240		
E_{off}	Turn-off Switching Energy			845		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			57	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			228	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -57A$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -57A, di_S/dt = 100A/\mu s$)		655		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -57A, di_S/dt = 100A/\mu s$)		13.5		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			8	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.22	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_J = +25^\circ C, L = 1.54mH, R_G = 25\Omega, \text{Peak } I_L = 57A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 57A, di/dt \leq 700A/\mu s, v_R \leq v_{DSS}, T_J \leq 150^\circ C$

⑥ E_{on} includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

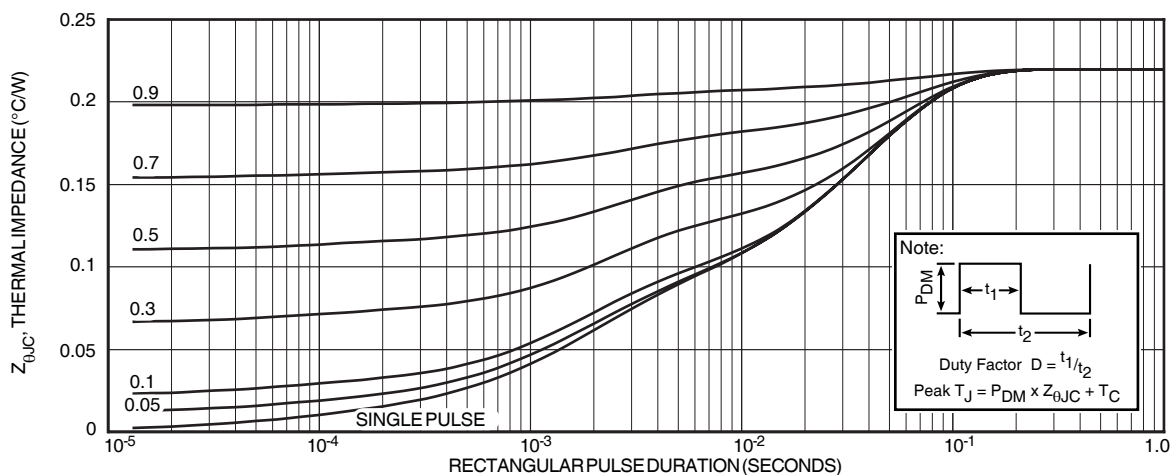


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT50M75B2LL_LLL(G)

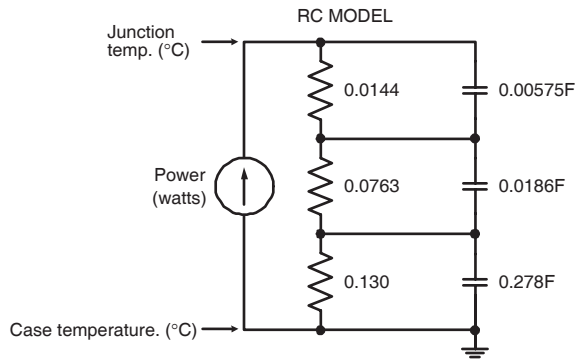


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

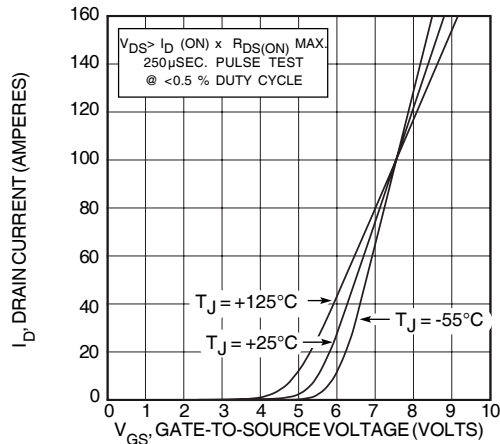


FIGURE 4, TRANSFER CHARACTERISTICS

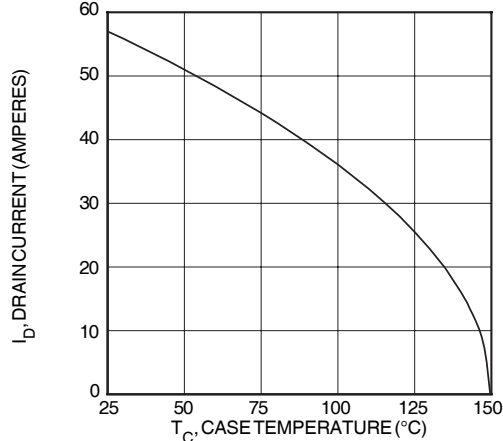


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

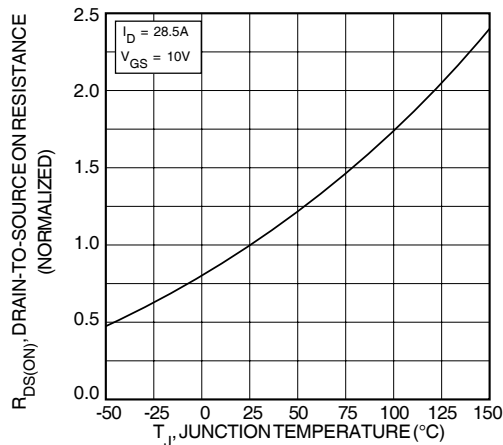


FIGURE 8, $R_{DS(\text{ON})}$ vs. TEMPERATURE

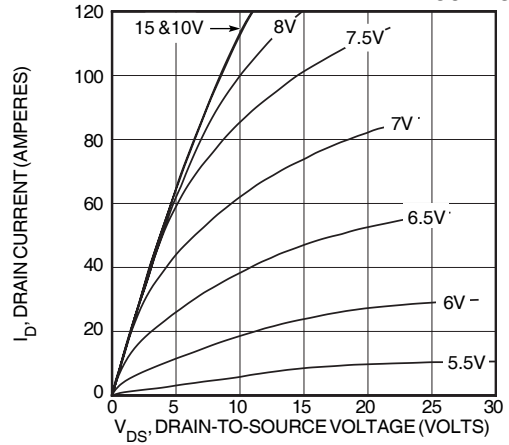


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

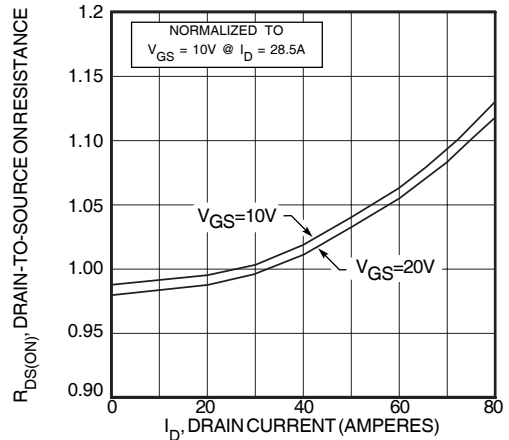


FIGURE 5, $R_{DS(\text{ON})}$ vs DRAIN CURRENT

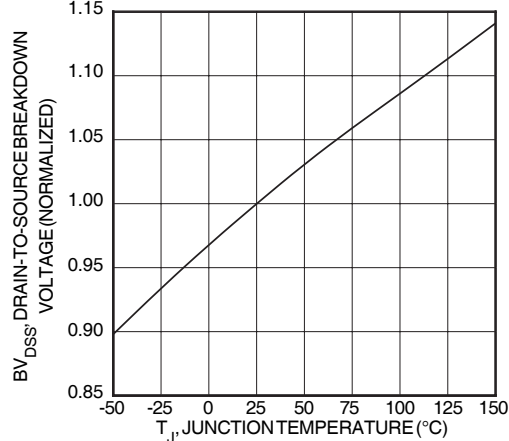


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

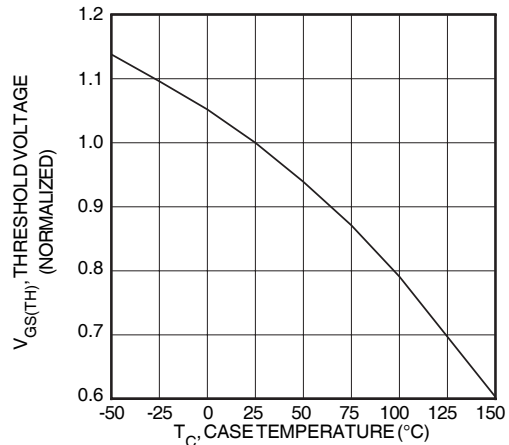


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

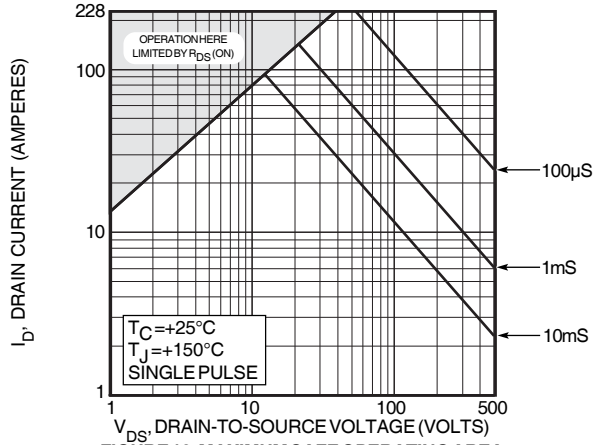


FIGURE 10, MAXIMUM SAFE OPERATING AREA

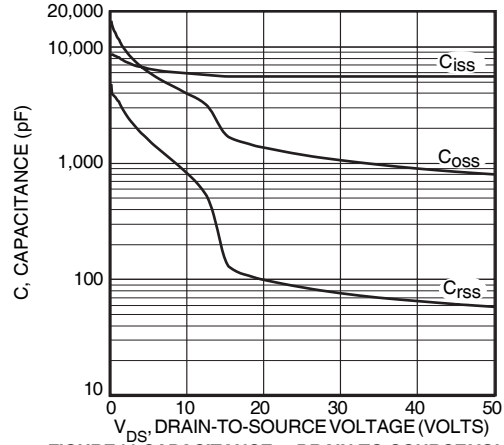


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

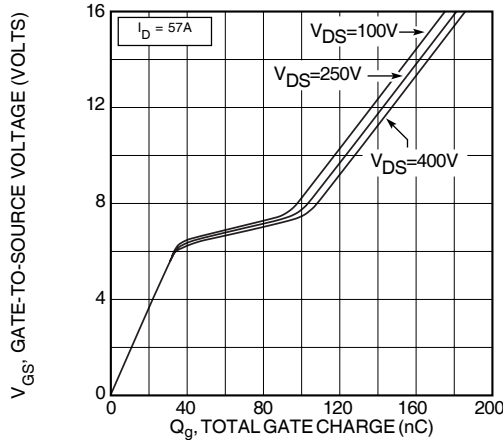


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

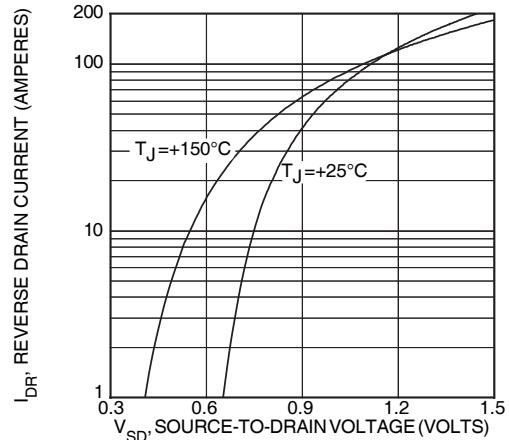


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

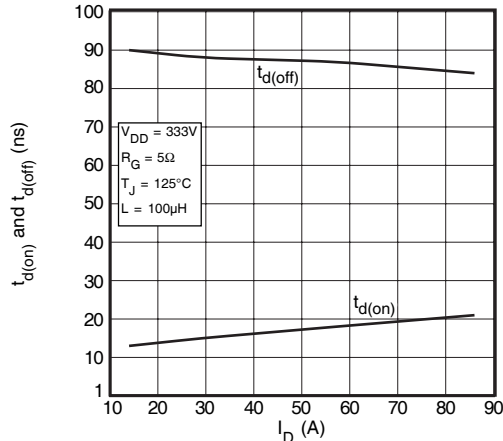


FIGURE 14, DELAY TIMES vs CURRENT

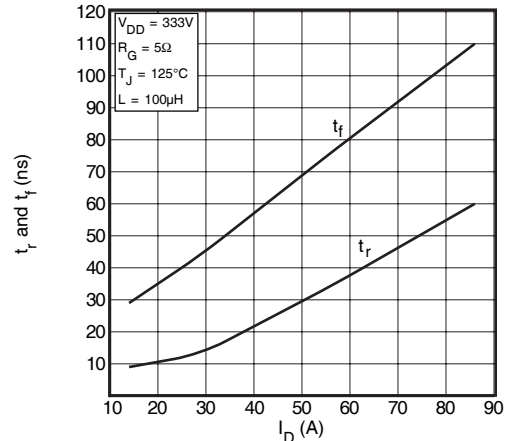


FIGURE 15, RISE AND FALL TIMES vs CURRENT

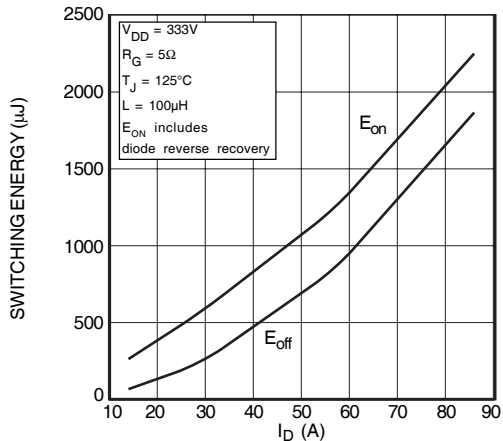


FIGURE 16, SWITCHING ENERGY vs CURRENT

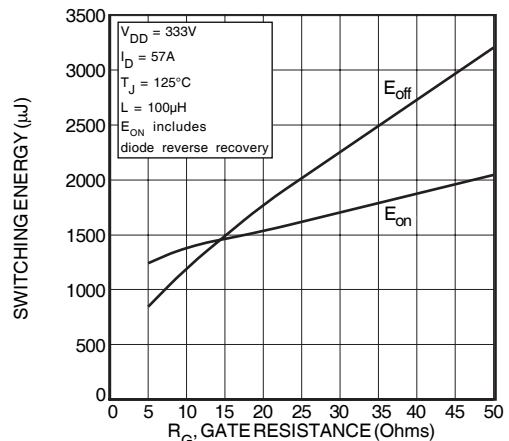


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

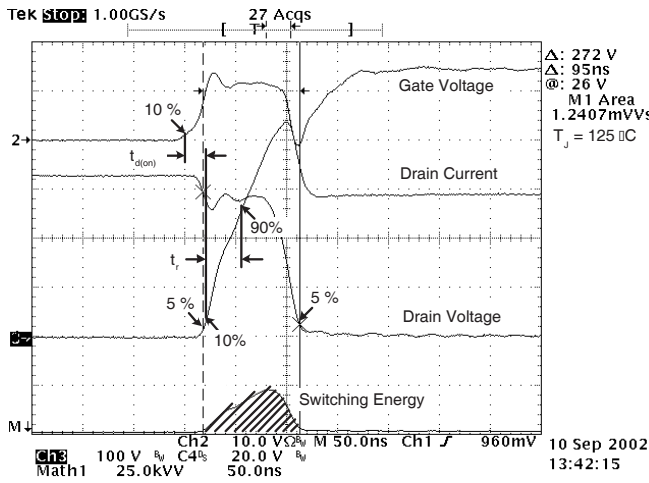


Figure 18, Turn-on Switching Waveforms and Definitions

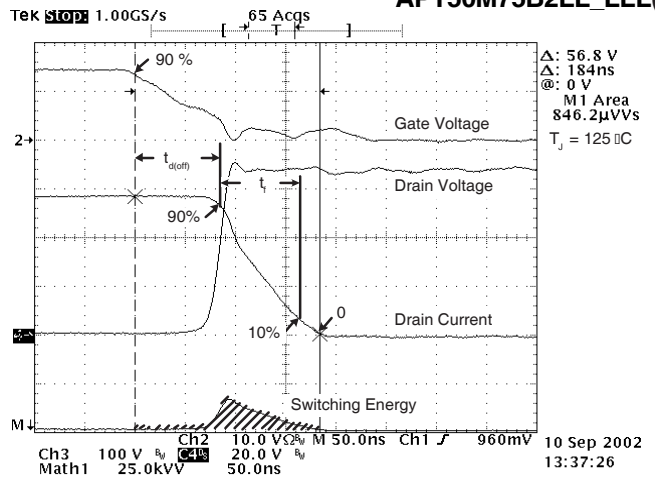


Figure 19, Turn-off Switching Waveforms and Definitions

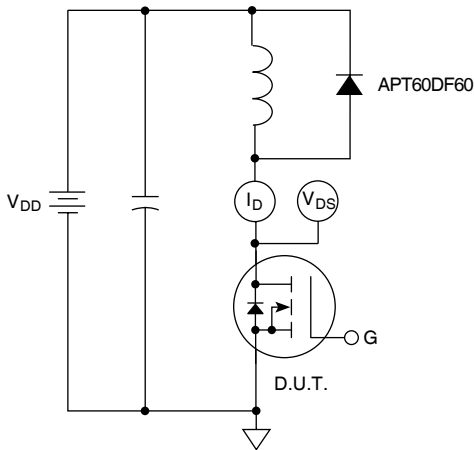
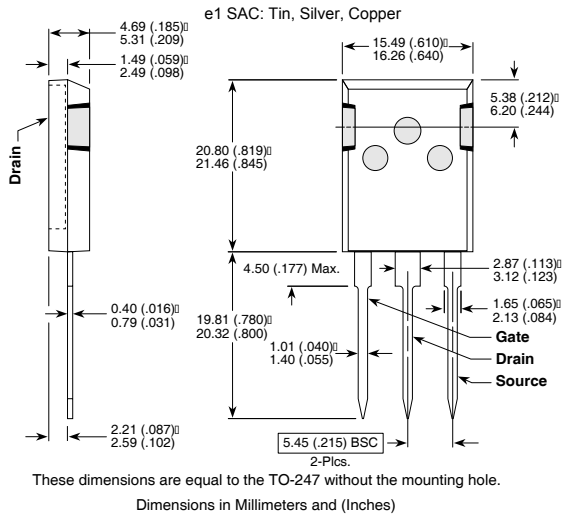


Figure 20, Inductive Switching Test Circuit

T-MAX™ (B2) Package Outline



TO-264 (L) Package Outline

