

N-channel 600 V, 0.175 Ω typ., 18 A MDmesh™ DM2 Power MOSFET in a TO-220FP package

Datasheet – production data

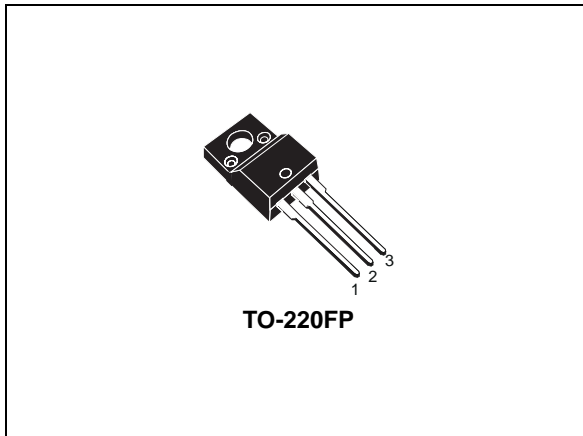
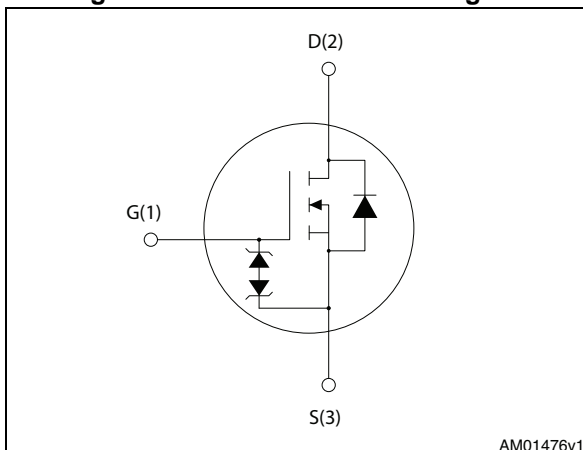


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STF24N60DM2	650 V	0.20 Ω	18 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh DM2 fast recovery diode series. It offers very low recovery charge and time (Q_{rr} , t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STF24N60DM2	24N60DM2	TO-220FP	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	12

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	18 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	11 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	72 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)	2500	V
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature		

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 18\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$; $V_{DD}=400\text{ V}$.
4. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ °C}$, $I_D = I_{AR}$; $V_{DD}=50$)	180	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$			1.5	μA
		$V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$		0.175	0.200	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1055	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	2.4	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0$	-	259	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0$	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 18\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14 and 19)	-	15	-	ns
t_r	Rise time		-	8.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 18 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 16)	-	155		ns
Q_{rr}	Reverse recovery charge		-	956		nC
I_{RRM}	Reverse recovery current		-	12.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 18 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16)	-	200		ns
Q_{rr}	Reverse recovery charge		-	1450		nC
I_{RRM}	Reverse recovery current		-	13		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

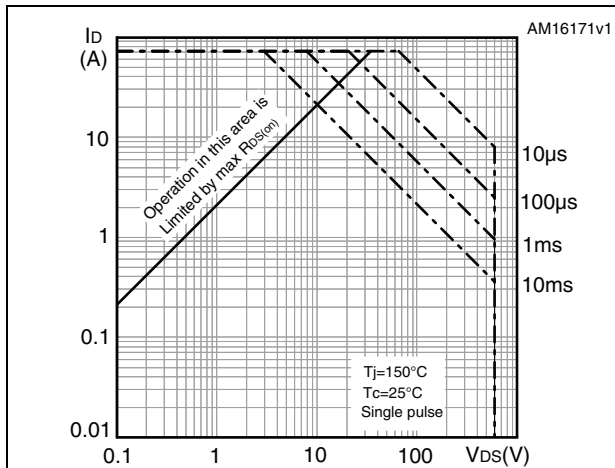


Figure 3. Thermal impedance

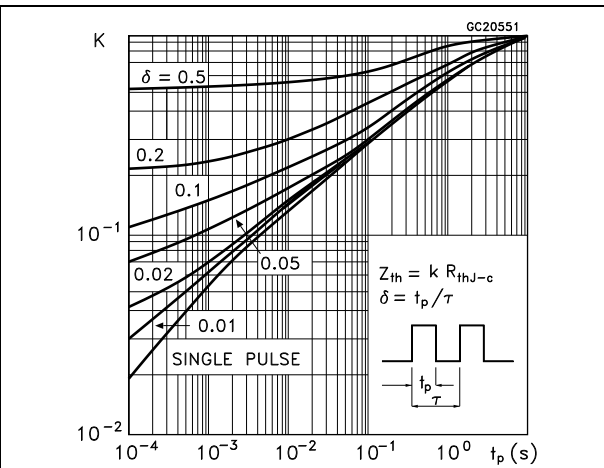


Figure 4. Output characteristics

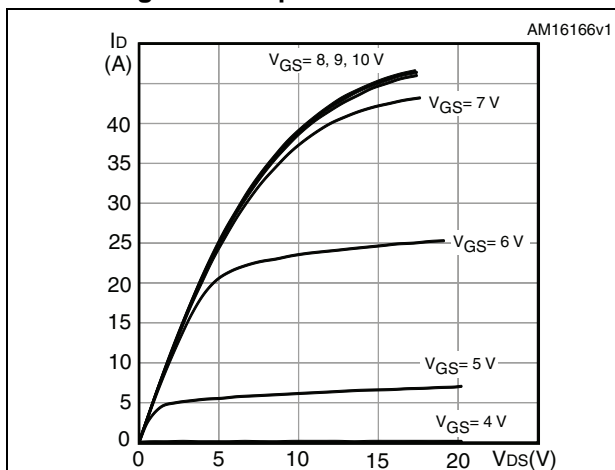


Figure 5. Transfer characteristics

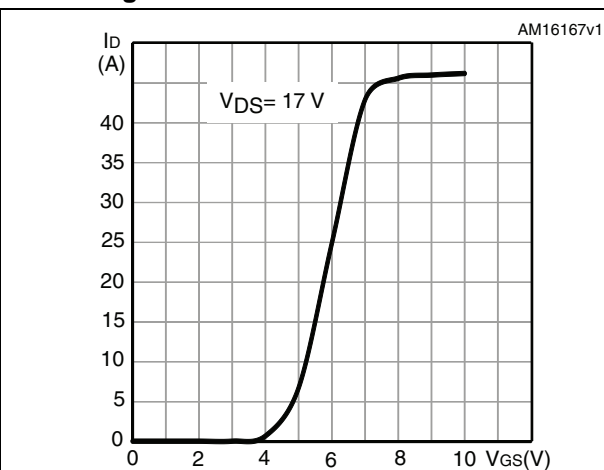


Figure 6. Gate charge vs gate-source voltage

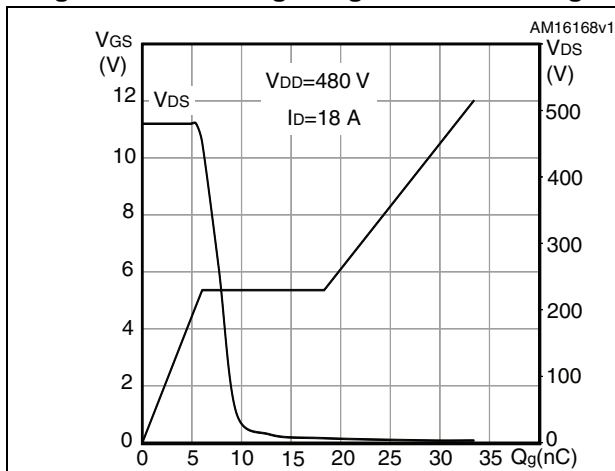


Figure 7. Static drain-source on-resistance

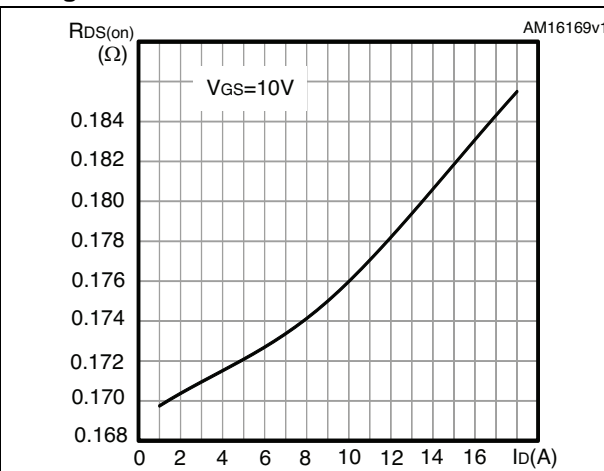


Figure 8. Capacitance variations

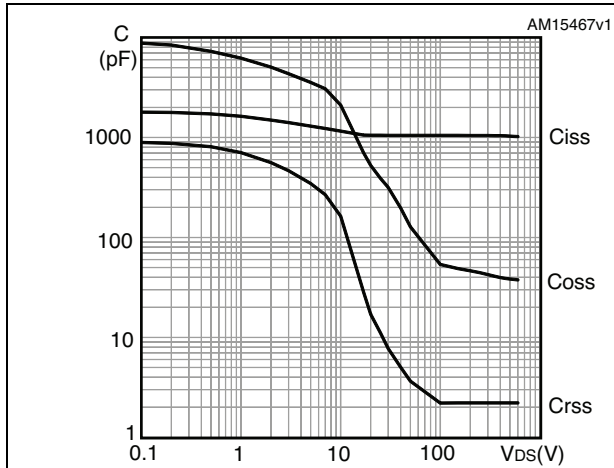


Figure 9. Output capacitance stored energy

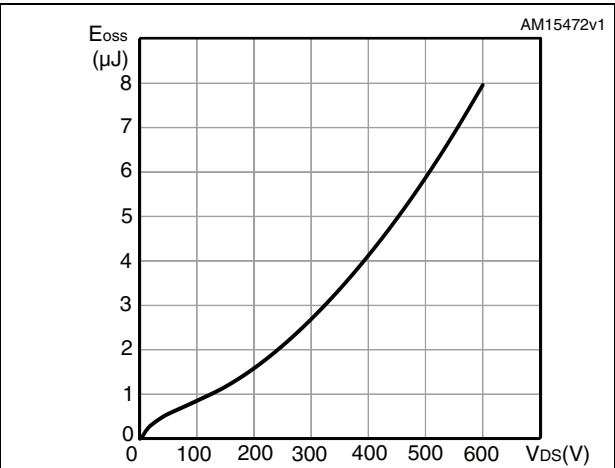


Figure 10. Normalized gate threshold voltage vs temperature

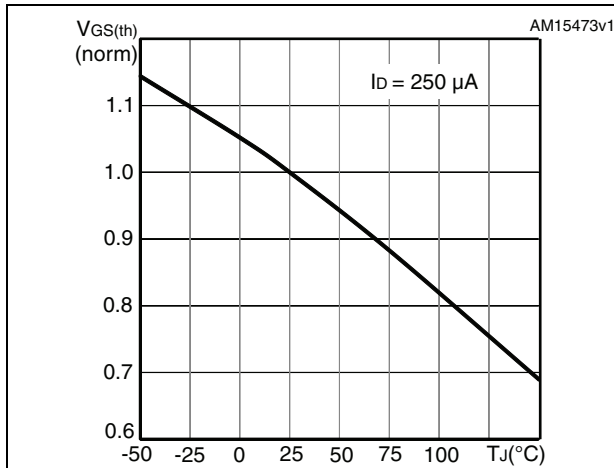


Figure 11. Normalized on-resistance vs temperature

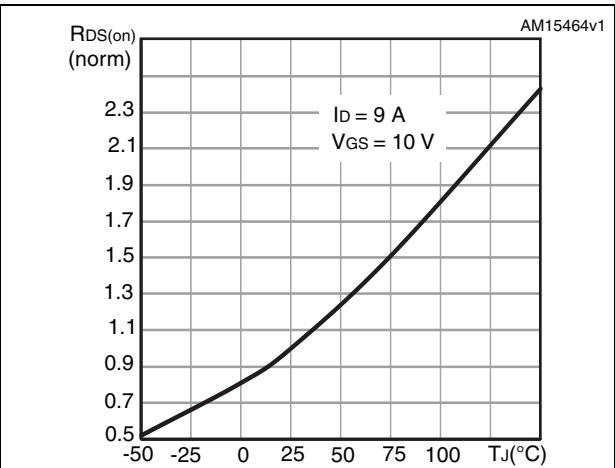


Figure 12. Source-drain diode forward characteristics

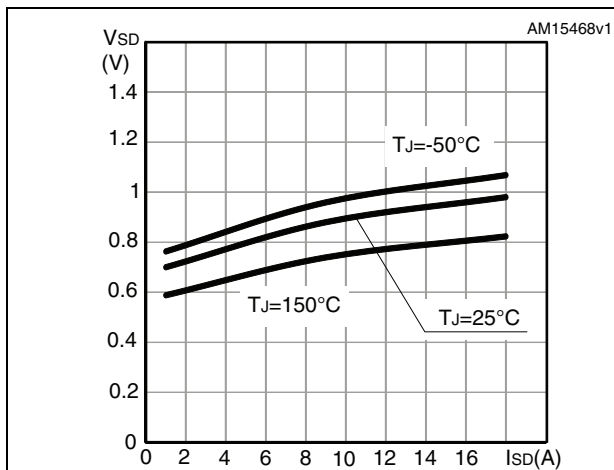
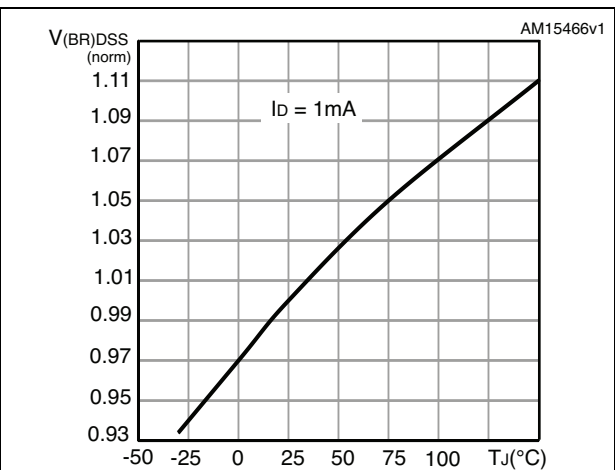


Figure 13. Normalized V(BR)DSS vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit

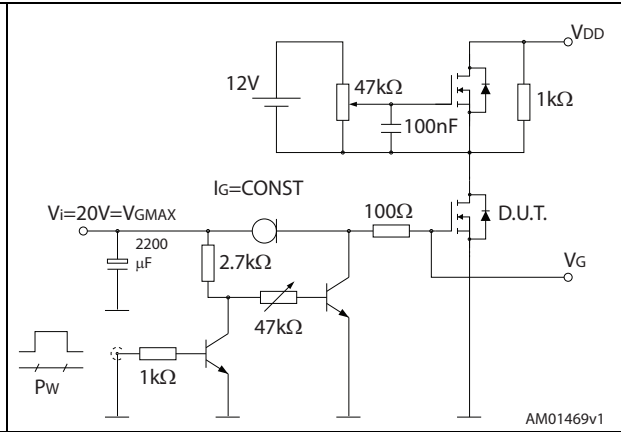


Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped inductive load test circuit



Figure 18. Unclamped inductive waveform

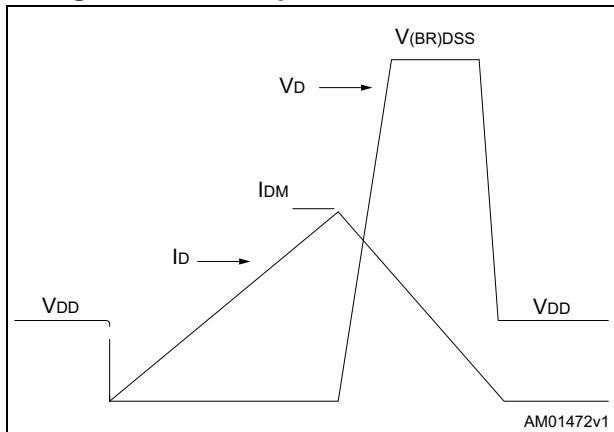


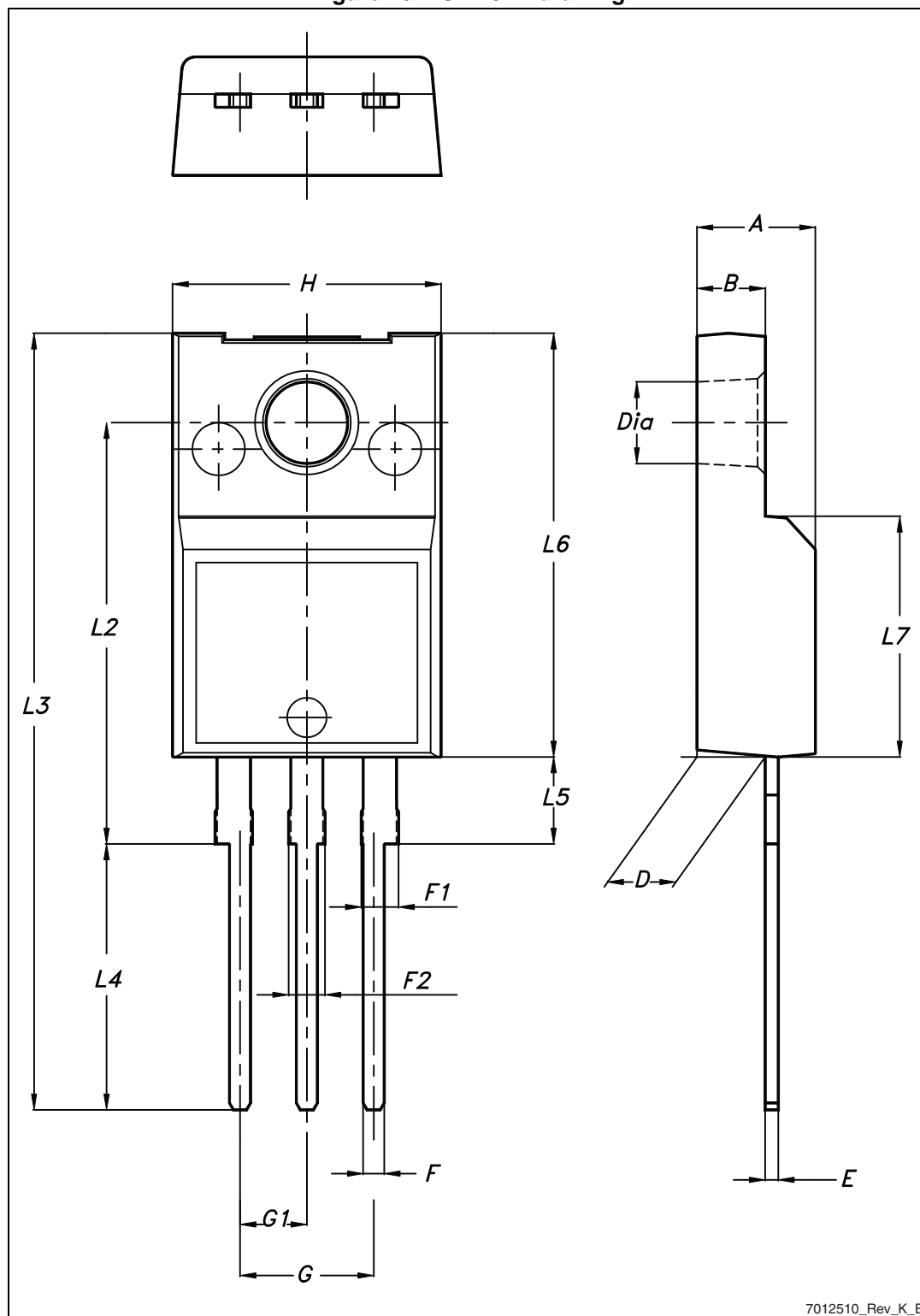
Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 20. TO-220FP drawing



7012510_Rev_K_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Nov-2013	1	First release.
21-Jan-2014	2	<ul style="list-style-type: none"> – Modified: dv/dt value in Table 2 – Modified: I_{AR} value in Table 4 – Modified: I_{DSS} and $V_{GS(th)}$ in Table 5 – Minor text changes
03-Mar-2014	3	<ul style="list-style-type: none"> – Modified: Figure 1 – Modified: P_{TOT} value and note 1 in Table 2 – Modified: $R_{thj-case}$ value in Table 3 – Modified: I_{AR} value in Table 4 – Minor text changes
05-Mar-2015	4	<ul style="list-style-type: none"> – Document status promoted from preliminary to production data. – Updated title, features and description in cover page.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

