Multilayer Ceramic Chip Capacitors

1 of 3 Creation Date : April 05, 2017 (GMT)

C1005JB0J225M050BC



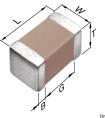






TDK item description C1005JB0J225MT****

Applications	Commercial Grade
Feature	General (Up to 50V)
Series	C1005 [EIA 0402]
Status	Production



limensions in mm

Size	
Length(L)	1.00mm ±0.05mm
Width(W)	0.50mm ±0.05mm
Thickness(T)	0.50mm ±0.05mm
Terminal Width(B)	0.10mm Min.
Terminal Spacing(G)	0.30mm Min.
Recommended Land Pattern (PA)	0.30mm to 0.50mm
Recommended Land Pattern (PB)	0.35mm to 0.45mm
Recommended Land Pattern (PC)	0.40mm to 0.60mm

Electrical Characteristics		
Capacitance	2.2μF ±20%	
Rated Voltage	6.3VDC	
Temperature Characteristic	JB(±10%)	
Dissipation Factor (Max.)	10%	
Insulation Resistance (Min.)	45ΜΩ	

Other		
Soldering Method	Reflow	
AEC-Q200	No	
Packing	Punched (Paper)Taping [180mm Reel]	
Package Quantity	10000pcs	

[!] Images are for reference only and show exemplary products.

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[!] All specifications are subject to change without notice.

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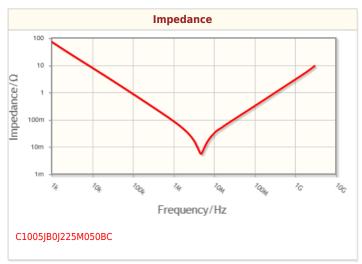


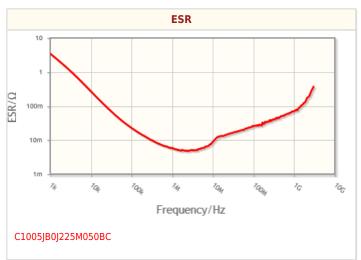


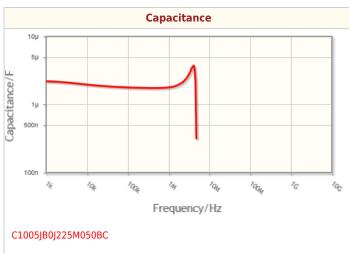


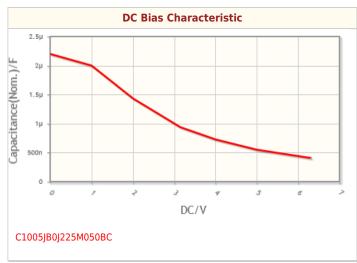


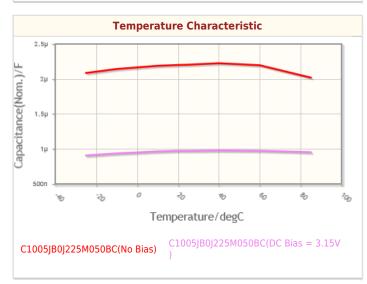
Characteristic Graphs(This is reference data, and does not guarantee the products characteristics.)













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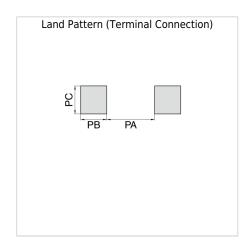








Associated Images



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