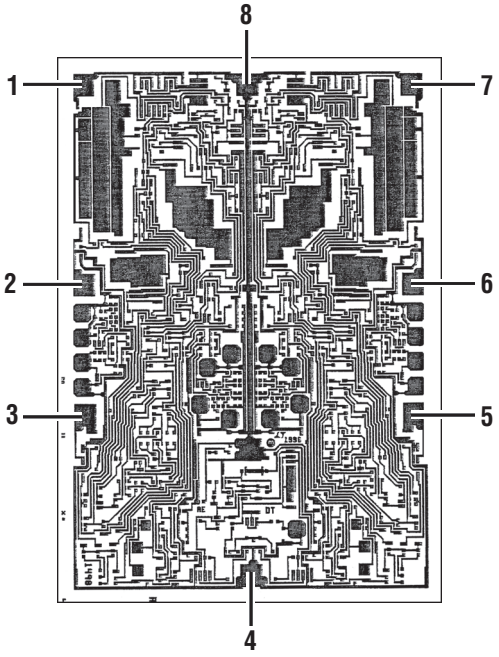
DICE/DWF SPECIFICATION

RH1498
10MHz, 6V/µs Rail-to-Rail Input and Output Precision C-Load Op Amp



117mils × 82mils,
12mils thick.
Backside (substrate) is an alloyed gold layer.
Connect backside to V^+.

PAD FUNCTION

1. OUTPUT A
2. –INA
3. +INA
4. $V^–$
5. +INB
6. –INB
7. OUTPUT B
8. V^+

DIE CROSS REFERENCE

LTC Finished Part Number	Order Part Number
RH1498	RH1498DICE
RH1498	RH1498DWF*

Please refer to LTC standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

DICE/DWF ELECTRICAL TEST LIMITS

(Pre-Irradiation) V_S = ±15V; V_{CM} = V_{OUT} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+, $V^–$		800	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+ to $V^–$		1400	µV
I_B	Input Bias Current	V_{CM} = V^+ V_{CM} = $V^–$	0 –715	715 0	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+, $V^–$	0	200	nA
I_{OS}	Input Offset Current	V_{CM} = V^+, $V^–$		70	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R1 = 10k V_O = –10V to 10V, R1 = 2k	1000 500		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^+ to $V^–$	90		dB
	CMRR Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+ to $V^–$	84		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±16V	90		dB
	PSRR Match (Channel-to-Channel) (Note 1)	V_S = ±2V to ±16V	83		dB
V_{OL}	Output Voltage Swing (Low) (Note 2)	No Load I_{SINK} = 1mA I_{SINK} = 10mA		30 100 500	mV mV mV

DICE/DWF ELECTRICAL TEST LIMITS (Pre-Irradiation) V_S = ±15V; V_{CM} = V_{OUT} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OH}	Output Voltage Swing (High) (Note 2)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 10mA		10 150 800	mV mV mV
I_{SC}	Short-Circuit Current		±15		mA
I_S	Supply Current per Amplifier			2.5	mA
GBW	Gain-Bandwidth Product	f = 100kHz	6.8		MHz
SR	Slew Rate	A_V = –1, R_L = 10k V_O = ±10V, Measure at V_O = ±5V	3.5		V/µs

DICE/DWF ELECTRICAL TEST LIMITS (Pre-Irradiation) V_S = 5V; V_{CM} = V_{OUT} = Half Supply, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+, V^-		800	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+ to V^-		1400	µV
I_B	Input Bias Current	V_{CM} = V^+ V_{CM} = V^-	0 –650	650 0	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 1)	V_{CM} = V^+, V^-	0	180	nA
I_{OS}	Input Offset Current	V_{CM} = V^+, V^-		65	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 75mV to 4.8V, R1 = 10k	600		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^+ to V^-	76		dB
	CMRR Match (Channel-to-Channel) (Note 1)	V_S = 5V, V_{CM} = V^+ to V^-	75		dB
PSRR	Power Supply Rejection Ratio	V_S = 4.5V to 12V; V_{CM} = V_O = 0.5V	88		dB
	PSRR Match (Channel-to-Channel) (Note 1)	V_S = 4.5V to 12V; V_{CM} = V_O = 0.5V	82		dB
V_{OL}	Output Voltage Swing (Low) (Note 2)	No Load I_{SINK} = 1mA I_{SINK} = 2.5mA		30 100 200	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 2)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 2.5mA		10 150 250	mV mV mV
I_{SC}	Short-Circuit Current		±12		mA
I_S	Supply Current per Amplifier			2.2	mA

Note 1: Matching parameters are the difference between amplifiers A and B.

Note 2: Output voltage swings are measured between the output and power supply rails.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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