1GB – 2x64Mx72 DDR SDRAM REGISTERED, w/PLL

FEATURES

- 200-pin SO-DIMM, dual in-line memory module
- Fast data transfer rates: PC2100 and PC2700
- Utilizes 266 and 333 Mb/s DDR SDRAM components
- $V_{CC} = V_{CCQ} = 2.5V \pm 0.2V$
- Bidirectional data strobe (DQS) option
- Differential clock inputs (CK and CK#)
- DLL to align DQ and DQS transitions with CK
- Programmable burst: length (2, 4, 8)
- Programmable READ# latency (CL): 2 and 2.5 (clock)
- Serial Presence Detect (SPD) with EEPROM
- Auto and self refresh: 64ms/ 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- Package option
  - 200 Pin SO-DIMM
  - PCB – 31.75mm (1.25") Max

DESCRIPTION

The WV3EG264M72ESFR is a 2x64Mx72 Double Data Rate DDR SDRAM high density module. This memory module consists of eighteen 64Mx8 bit with 4 banks DDR Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	DDR333@CL = 2.5	DDR266@CL = 2	DDR266@CL = 2.5
Clock Speed	166MHz	133MHz	133MHz
CL-t_{RCD}-t_{RP}	2.5-3-3	2-2-2	2.5-3-3

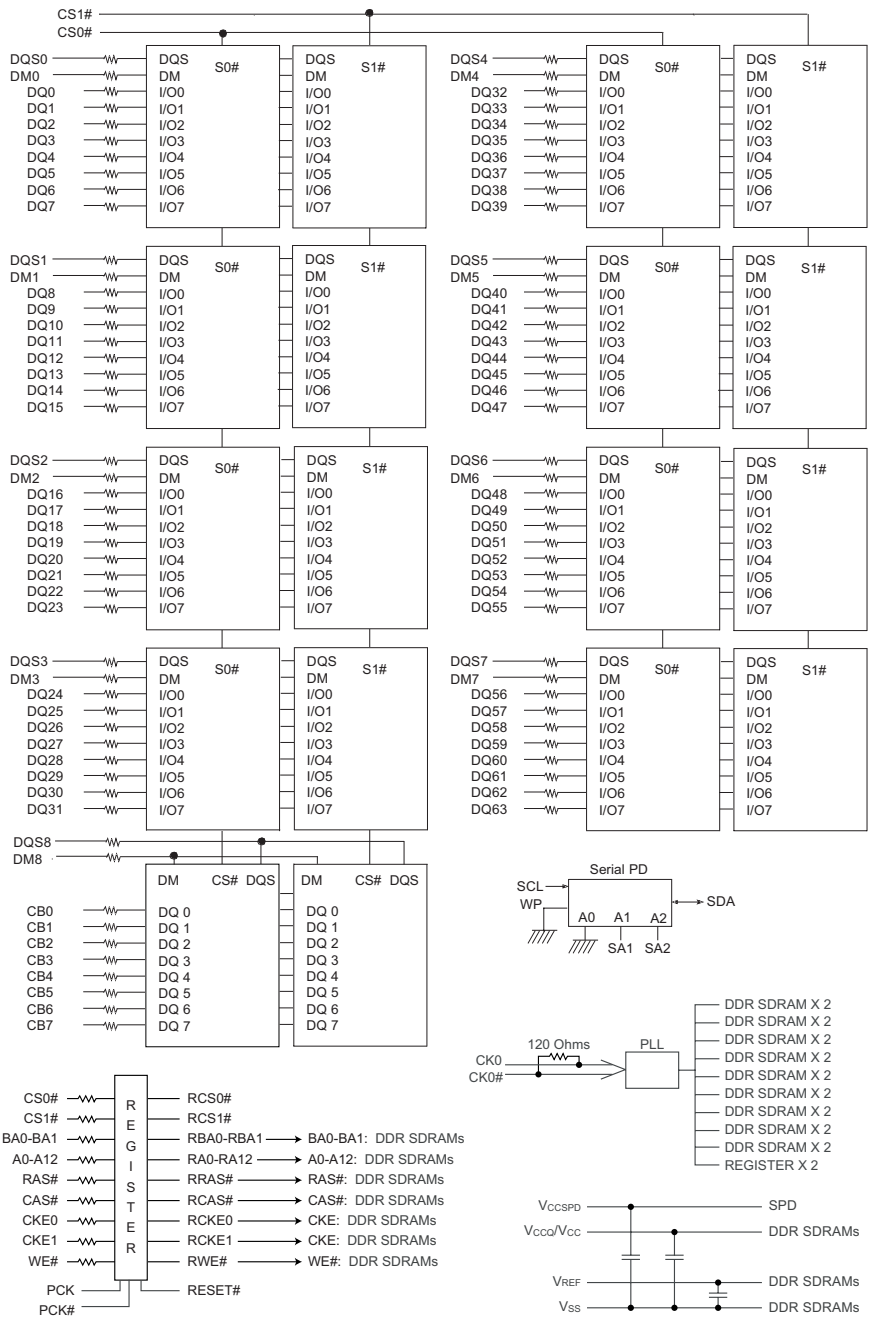
PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{CC}
6	DQ4	56	DQ28	106	A6	156	V_{CC}
7	DQ1	57	V_{CC}	107	A5	157	V_{CC}
8	DQ5	58	V_{CC}	108	A4	158	NC
9	V_{CC}	59	DQ25	109	A3	159	V_{SS}
10	V_{CC}	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	V_{SS}
12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{CC}	163	DQ48
14	DQ6	64	V_{SS}	114	V_{CC}	164	DQ52
15	V_{SS}	65	DQ26	115	A10/AP	165	DQ49
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{CC}
18	DQ7	68	DQ31	118	RAS#	168	V_{CC}
19	DQ8	69	V_{CC}	119	WE#	169	DQS6
20	DQ12	70	V_{CC}	120	CAS#	170	DM6
21	V_{CC}	71	CB0	121	CS0#	171	DQ50
22	V_{CC}	72	CB4	122	CS1#	172	DQ54
23	DQ9	73	CB1	123	NC	173	V_{SS}
24	DQ13	74	CB5	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	DQS8	127	DQ32	177	DQ56
28	V_{SS}	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	V_{CC}
30	DQ14	80	CB6	130	DQ37	180	V_{CC}
31	DQ11	81	V_{CC}	131	V_{CC}	181	DQ57
32	DQ15	82	V_{CC}	132	V_{CC}	182	DQ61
33	V_{CC}	83	CB3	133	DQS4	183	DQS7
34	V_{CC}	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}
36	V_{CC}	86	RESET#	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	NC	139	DQ35	189	DQ59
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V_{CC}
42	DQ20	92	V_{CC}	142	DQ44	192	V_{CC}
43	DQ17	93	V_{CC}	143	V_{CC}	193	SDA
44	DQ21	94	V_{CC}	144	V_{CC}	194	SA0
45	V_{CC}	95	CKE1	145	DQ41	195	SCL
46	V_{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V_{SS}	199	NC
50	DQ22	100	A11	150	V_{SS}	200	NC

PIN NAMES

Pin Name	Function
A0-A12	Address Inputs
BA0, BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
CK0,CK0#	Clock inputs, positive/negative
CKE0, CKE1	Clock enable input
CS0#, CS1#	Chip select input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
V_{CC}	Core Power
V_{CCQ}	I/O Power
V_{SS}	Ground
SA0-SA2	EEPROM address
SDA	Serial Data Input/Output
V_{REF}	Input/Output Reference
DM0-DM8	Data-in mask
V_{CCSPD}	Serial EEPROM power supply
SCL	Serial Presence Detect(SPD) Clock Input
RESET#	Reset enable
NC	Spare pins, No connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.

DC OPERATING CONDITIONS

0°C T_A 70°C

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (for device with a nominal V_{CC} of 2.5V)	V_{CC}	2.3	2.7		
I/O Supply voltage	V_{CCQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	0.49*V_{CCQ}	0.51*V_{CCQ}	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{CCQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and CK# inputs	V_{IN}(DC)	-0.3	V_{CCQ}+0.3	V	
Input Differential Voltage, CK and CK# inputs	V_{ID}(DC)	0.3	V_{CCQ}+0.6	V	3
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver); V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver); V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver); V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver); V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Notes:
1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled to V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHz.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.3	V
Voltage on V_{CC} & V_{CCQ} pin relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 3.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Operating Temperature	T_A	0 ~ +70	°C
Power dissipation – 1GB single mezzanine memory	P_D	18	W
Short circuit current	I_{OS}	50	mA

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

CAPACITANCE

V_{CC} 2.5V, V_{CCQ} = 2.5V ±0.2V, T_A = 25°C, f = 1MHz

Parameter	Symbol	Min	Max	Units
Input capacitance (A0 ~ A12, BA0 ~ BA1,RAS#,CAS#, WE#)	C_{IN1}	9	11	pF
Input capacitance (CKE0, CKE1)	C_{IN2}	9	11	pF
Input capacitance (CS0#, CS1#)	C_{IN3}	9	11	pF
Input capacitance (CLK0, CLK0#)	C_{IN4}	11	12	pF
Input capacitance (DM0 ~ DM8)	C_{IN5}	10	11	pF
Data & DQS input/output capacitance (DQ0~DQ63)	C_{OUT1}	10	11	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	10	11	pF

DDR I_{DD} SPECIFICATIONS AND CONDITIONS

0°C ≤ T_{CASE} < +70°C; V_{CCQ} = +2.5V ± 0.2V, V_{CC} = +2.5V ± 0.2V

Symbol	Conditions	335	262	265	Unit
I_{DD0}	Operating current - One bank Active-Precharge; t_{RC} = t_{RC}(min); t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,215	1,215	1,080	mA
I_{DD1}	Operating current - One bank operation; One bank open, BL = 4, Reads - Refer to the following page for detailed test condition	1,485	1,485	1,350	mA
I_{DD2P}	Percharge power-down standby current; All banks idle; power - down mode; CKE = <V_{IL}(max); t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; V_{IN} = V_{REF} for DQ, DQS and DM	90	90	90	mA
I_{DD2F}	Precharge Floating standby current; CS# > = V_{IH}(min);All banks idle; CKE > = V_{IH}(min); t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM	810	810	720	mA
I_{DD3P}	Active power - down standby current; one bank active; power-down mode; CKE = < V_{IL}(max); t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; V_{IN} = V_{REF} for DQ, DQS and DM	630	630	540	mA
I_{DD3N}	Active standby current; CS# > = V_{IH}(min); CKE> = V_{IH}(min); one bank active; active - precharge; t_{RC} = t_{RAS}max; t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	900	900	810	mA
I_{DD4R}	Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; CL = 2 at t_{CK} = 100Mhz for DDR200, CL = 2 at t_{CK} = 133Mhz for DDR266A, CL = 2.5 at t_{CK} = 133Mhz for DDR266B ; 50% of data changing at every burst; I_{OUT} = 0 m A	1.530	1.530	1,350	mA
I_{DD4W}	Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL = 2 at t_{CK} = 100Mhz for DDR200, CL = 2 at t_{CK} = 133Mhz for DDR266A, CL = 2.5 at t_{CK} = 133Mhz for DDR266B ; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	1,440	1,440	1,260	mA
I_{DD5}	Auto refresh current; t_{RC} = t_{RFC}(min) - 8*t_{CK} for DDR200 at 100Mhz, 10*t_{CK} for DDR266A & DDR266B at 133Mhz; distributed refresh	5,220	5,220	5,040	mA
I_{DD6}	Self refresh current; CKE = < 0.2V; External clock should be on; t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B	90	90	90	mA
I_{DD7A}	Orerating current - Four bank operation; Four bank interleaving with BL = 4 -Refer to the following page for detailed test condition	3,690	3,645	3,195	mA

Typical case: V_{CC} = 2.5V, T = 25°C
Worst case: V_{CC} = 2.7V, T = 10°C
Note: I_{DD} specifications are based on Micron components. Other DRAM manufacturers specificaitons may be different.

AC TIMING PARAMETERS

$0°C \le T_{CASE} < +70°C$; $V_{CCQ} = +2.5V \pm 0.2V$, $V_{CC} = +2.5V \pm 0.2V$

Parameter		Symbol	335		262		265		Unit
			Min	Max	Min	Max	Min	Max	
Row cycle time		t_{RC}	60		65		65		ns
Refresh row cycle time		t_{RFC}	72		75		75		ns
Row active time		t_{RAS}	42	70K	45	120K	45	120K	ns
RAS# to CAS# delay		t_{RCD}	18		20		20		ns
Row precharge time		t_{RP}	18		20		20		ns
Row active to Row active		t_{RRD}	12		15		15		ns
Write recovery time		t_{WR}	15		15		15		ns
Last data in to Read command		t_{WTR}	1		1		1		t_{CK}
Col. address to Col. address		t_{CCD}	1		1		1		t_{CK}
Clock cycle time	CL=2.0	t_{CK}	7.5	12	7.5	12	10	12	ns
	CL=2.5		6	12	7.5	12	7.5	12	ns
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DQS-out access time from		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns
Output data access time		t_{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Data strobe edge to ouput		t_{DQSQ}	—	0.4	—	0.5	—	0.5	ns
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
CK to valid DQS-in		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}
DQS-in setup time		t_{WPRE}	0		0		0		ns
DQS-in hold time		t_{WPRE}	0.25		0.25		0.25		t_{CK}
DQS falling edge to CK ris-		t_{DSS}	0.2		0.2		0.2		t_{CK}
DQS falling edge from CK		t_{DSH}	0.2		0.2		0.2		t_{CK}
DQS-in high level width		t_{DQSH}	0.35		0.35		0.35		t_{CK}
DQS-in low level width		t_{DQSL}	0.35		0.35		0.35		t_{CK}
DQS-in cycle time		t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
Address and Control Input		t_{IS}	0.75		0.9		0.9		ns
Address and Control Input		t_{IH}	0.75		0.9		0.9		ns
Address and Control Input		t_{IS}	0.8		1.0		1.0		ns
Address and Control Input		t_{IH}	0.8		1.0		1.0		ns
Data-out high impedence time from CK/CK#		t_{HZ}		+0.7		+0.75		+0.75	ns
Data-out low impedence time from CK/CK#		t_{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Input Slew Rate (for input)		$t_{SL(I)}$	0.5		0.5		0.5		V/ns
Input Slew Rate (for I/O pins)		$t_{SL(IO)}$	0.5		0.5		0.5		V/ns
Output Slew Rate (x4,x8)		$t_{SL(O)}$	1.0	4.5	1.0	4.5	1.0	4.5	V/ns
Output Slew Rate Matching		t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5	

Note: AC specifications are based on Micron components. Other DRAM manufacturers specificaitons may be different.

AC TIMING PARAMETERS

0°C ≤ T_{CASE} < +70°C; V_{CCQ} = +2.5V ± 0.2V, V_{CC} = +2.5V ± 0.2V

Parameter	Symbol	335		262		265		Unit
		Min	Max	Min	Max	Min	Max	
Mode register set cycle time	t_{MRD}	12		15		15		ns
DQ & DM setup time to DQS	t_{DS}	0.45		0.5		0.5		ns
DQ & DM hold time to DQS	t_{DH}	0.45		0.5		0.5		ns
Control & Address input	t_{IPW}	2.2		2.2		2.2		ns
DQ & DM input pulse width	t_{DIPW}	1.75		1.75		1.75		ns
Power down exit time	t_{PDEX}	6		7.5		7.5		ns
Exit self refresh to non-Read	t_{XSNR}	75		75		75		ns
Exit self refresh to read command	t_{XSRD}	200		200		200		tCK
Refresh interval time	t_{REFI}		7.8		7.8		7.8	us
Output DQS valid window	t_{QH}	t_{HP}-t_{QHS}	—	t_{HP}-t_{QHS}	—	t_{HP}-t_{QHS}	—	ns
Clock half period	t_{HP}	t_{CL}min or t_{CH}min	—	t_{CL}min or t_{CH}min	—	t_{CL}min or t_{CH}min	—	ns
Data hold skew factor	t_{QHS}		0.5		0.75		0.75	ns
DQS write postamble time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Active to Read with Auto precharge command	t_{RAP}	15		15		20		
Autoprecharge write recovery + Precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}

Note: AC specifications are based on Micron components. Other DRAM manufacturers specificaitons may be different.

SERIAL PRESENT DETECT INFORMATION

Byte #	Function described	Function Supported			Hex value		
		265	262	335	265	262	335
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes			80h		
1	Total # of Bytes of SPD memory device	256bytes (2K-bit)			08h		
2	Fundamental memory type	SDRAM DDR			07h		
3	# of row address on this assembly	13			0Dh		
4	# of column address on this assembly	11			0Bh		
5	# of module Rows on this assembly	2 Row			02h		
6	Data width of this assembly	64 bits			48h		
7	Data width of this assembly	—			00h		
8	VDDQ and interface standard of this assembly	SSTL 2.5V			04h		
9	DDR SDRAM cycle time at CAS Latency =2.5	7.5ns	7ns	6ns	75h	70h	60h
10	DDR SDRAM Access time from clock at CL=2.5	±0.75	±0.75	±0.7	75h	75h	70h
11	DIMM configuration type(Non-parity, Parity, ECC)	ECC			02h		
12	Refresh rate & type	7.8us & Self refresh			82h		

SERIAL PRESENT DETECT INFORMATION (cont'd)

Byte #	Function described	Function Supported			Hex value		
		265	262	335	265	262	335
13	Primary DDR SDRAM width	x8			08h		
14	Error checking DDR SDRAM data width	x8			08h		
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1t_{CLK}			01h		
16	DDR SDRAM device attributes: Burst lengths supported	2,4,8			0Eh		
17	DDR SDRAM device attributes: # of banks on each DDR SDRAM	4 banks			04h		
18	DDR SDRAM device attributes: CAS Latency supported	2,2.5			0Ch		
19	DDR SDRAM device attributes: CS Latency	0CLK			01h		
20	DDR SDRAM device attributes: WE Latency	1CLK			02h		
21	DDR SDRAM module attributes	Registered address & control inputs and On-card DLL			26h		
22	DDR SDRAM device attributes: General	+/-0.2V voltage tolerance			C0h		
23	DDR SDRAM cycle time at CL =2	10ns	7.5ns	7.5ns	A0h	75h	75h
24	DDR SDRAM Access time from clock at CL =2	±0.75	±0.75	±0.7	75h	75h	70h
25	DDR SDRAM cycle time at CL =1.5	—	—	—	00h		
26	DDR SDRAM Access time from clock at CL =1.5	—	—	—	00h		
27	Minimum row precharge time (=t_{RP})	20ns	20ns	18ns	50h	50h	48h
28	Minimum row activate to row active delay (=t_{RRD})	15ns	15ns	12ns	3Ch	3Ch	30h
29	Minimum RAS to CAS delay (=t_{RCD})	20ns	20ns	18ns	50h	50h	48h
30	Minimum active to precharge time (=t_{RAS})	45ns	45ns	42ns	2Dh	2Dh	2Ah
31	Module ROW density	512MB			80h		
32	Command and address signal input setup time	0.9ns	0.9ns	0.8ns	A0h	A0h	80h
33	Command and address signal input hold time	0.9ns	0.9ns	0.8ns	A0h	A0h	80h
34	Data signal input setup time	0.5ns	0.5ns	0.45ns	50h	50h	45h
35	Data signal input hold time	0.5ns	0.5ns	0.45ns	50h	50h	45h
36-40	Superset information (may be used in future)	—			00h		
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time (t_{RC})	65ns	65ns	60ns	41h	41h	3Ch
42	DDR SDRAM Minimim Auto-Refresh to Active/Auto-Refresh Commmand Period (t_{RFC})	75ns	75ns	72ns	4Bh	4Bh	48h
43	DDR SDRAM Maximum Device Cycle Time (t_{CK} max)	13ns	13ns	12ns	34h	34h	30h
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals ($t_{DQSQmax}$)	0.50ns	0.50ns	0.45ns	50h	50h	45h
45	DDR SDRAM Read Data Hold Skew Factor (t_{QHS})	0.75ns	0.75ns	0.50ns	75h	75h	50h
46	Reserved	00	00	00	00h	00h	00h
47	DIMM Height	Standard/Low profile			01h		
48-61	Superset information (may be used in future)	—			00h		
62	SPD data revision code	Initial release			10h		
63	Checksum for Bytes 0 ~ 62	—			69h	39h	6Fh
64 - 127	Manufacturer INFO	—			00h		

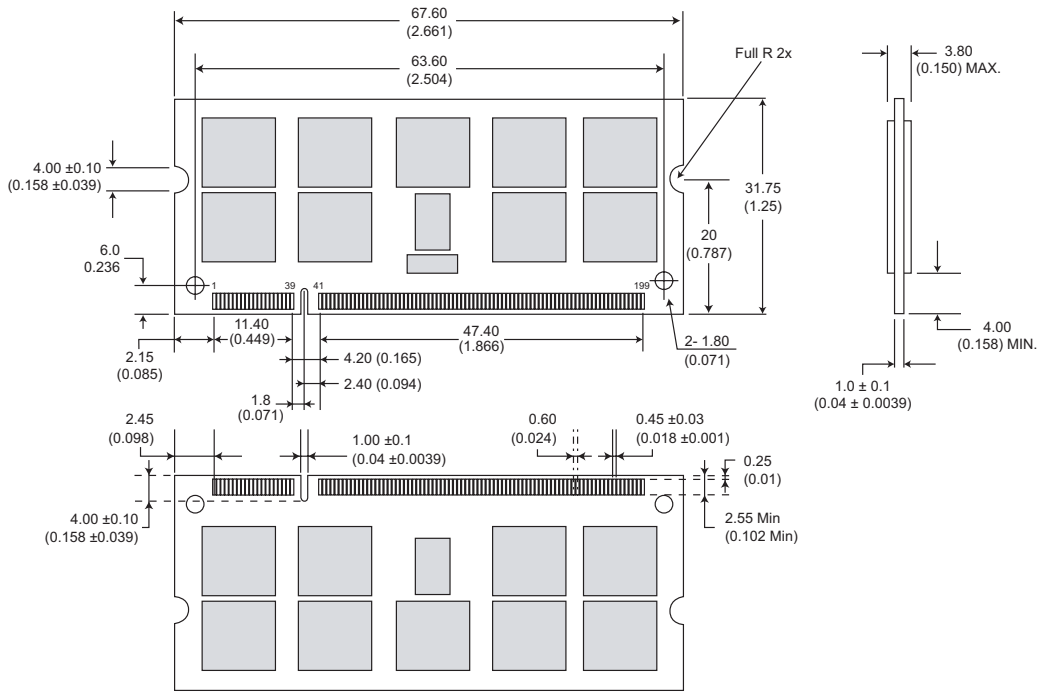
ORDERING INFORMATION FOR D4

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3EG264M72ESFR335D4-x	166MHz/333Mb/s	2.5	3	3	31.75mm (1.25")
WV3EG264M72ESFR262D4-x	133MHz/266Mb/s	2	2	2	31.75mm (1.25")
WV3EG264M72ESFR265D4-x	133MHz/266Mb/s	2.5	3	3	31.75mm (1.25")

NOTES:

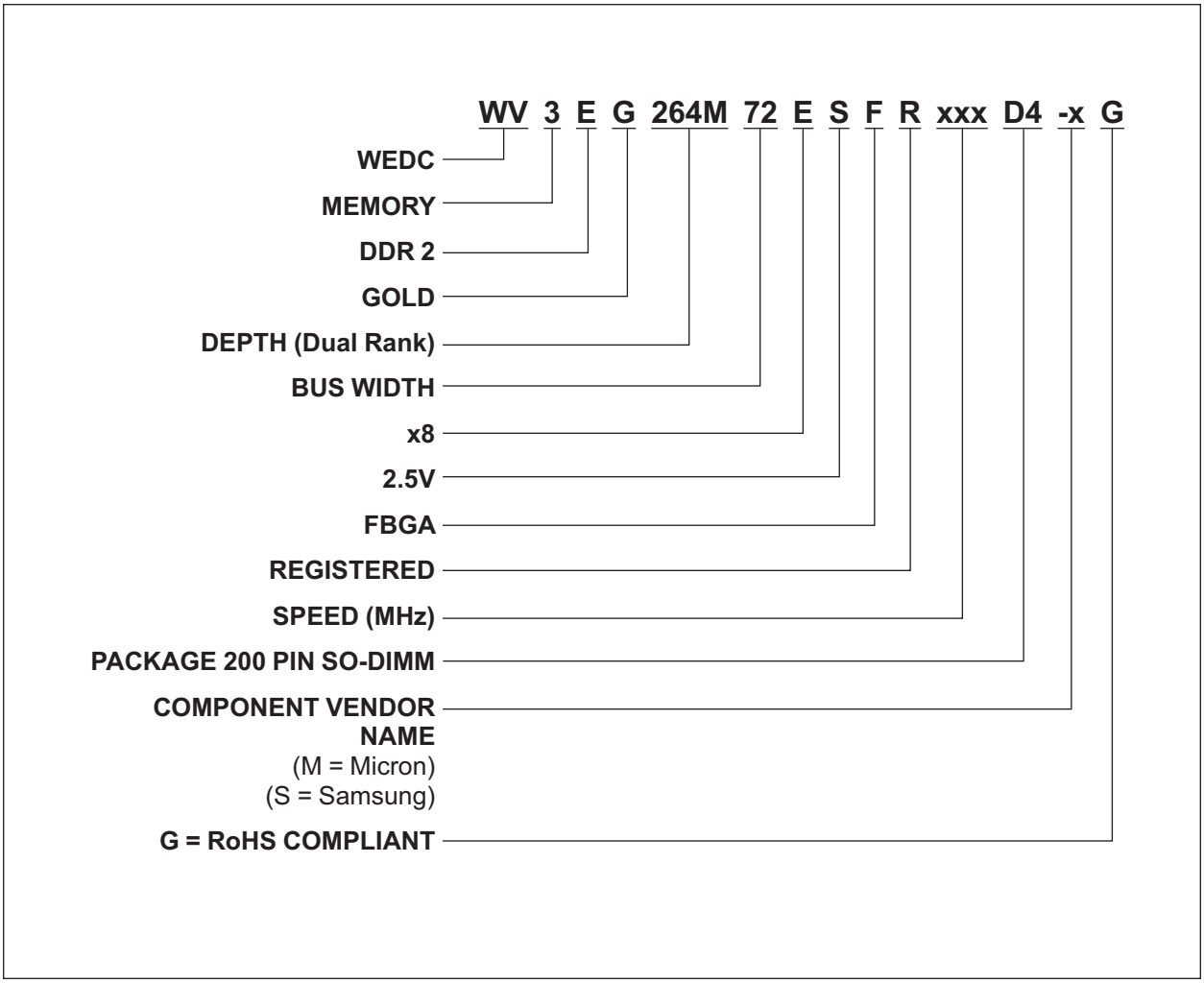
- Consult Factory for availability of RoHS compliant products. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "-x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
Tolerances: 0.15 (0.006) unless otherwise specified

PART NUMBERING GUIDE



Document Title

1GB – 2x64Mx72 DDR SDRAM REGISTERED, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	August 2005	Advanced