- **Supports Both FDM Full Rate (G.992.1) and G.lite (G.992.2) ADSL Applications**
- **Integrated Line Driver for TX and Line Receiver for RX**
- **Integrated TX/RX Filter, PGAs, and Equalizer**
- **Coexists with HPNA Devices (Version 1.0 and 2.0)**
- **14-Bit Integrated A/D and D/A Converters**
- **1.104 (G.lite)/2.208 (Full Rate) MHz Update Rate for the RX Channel**
- **276/552 kHz Update Rate for the TX Channel**
- **Integrated Voltage Compensated Crystal Oscillator (VCXO) DAC and Digital Phase-Lock Loop (DPLL)**
- **–150 dBm/Hz for Analog Input Referred Noise Floor**
- **Direct Single Serial Interface to TIs C5000 or C6000 DSP Families for Both Data and Control**
- **Two General-Purpose I/O Pins and Four General-Purpose Digital Outputs**
- **Integrated Auxiliary Amplifiers for System Flexibility**
- **Software and Hardware Power-Down Modes**
- **Power Dissipation**
  – 1.4 W With Line Driver Across 50-Ω Load
- **Delivering 12.3 dBm Power to the Line**
- **3.3-V and 12-V Supply (Line Driver) Power Supplies**
- **Industrial Temperature Range (–40°C to 85°C)**
- **64-Pin PAP Package (PowerPAD™)**

description

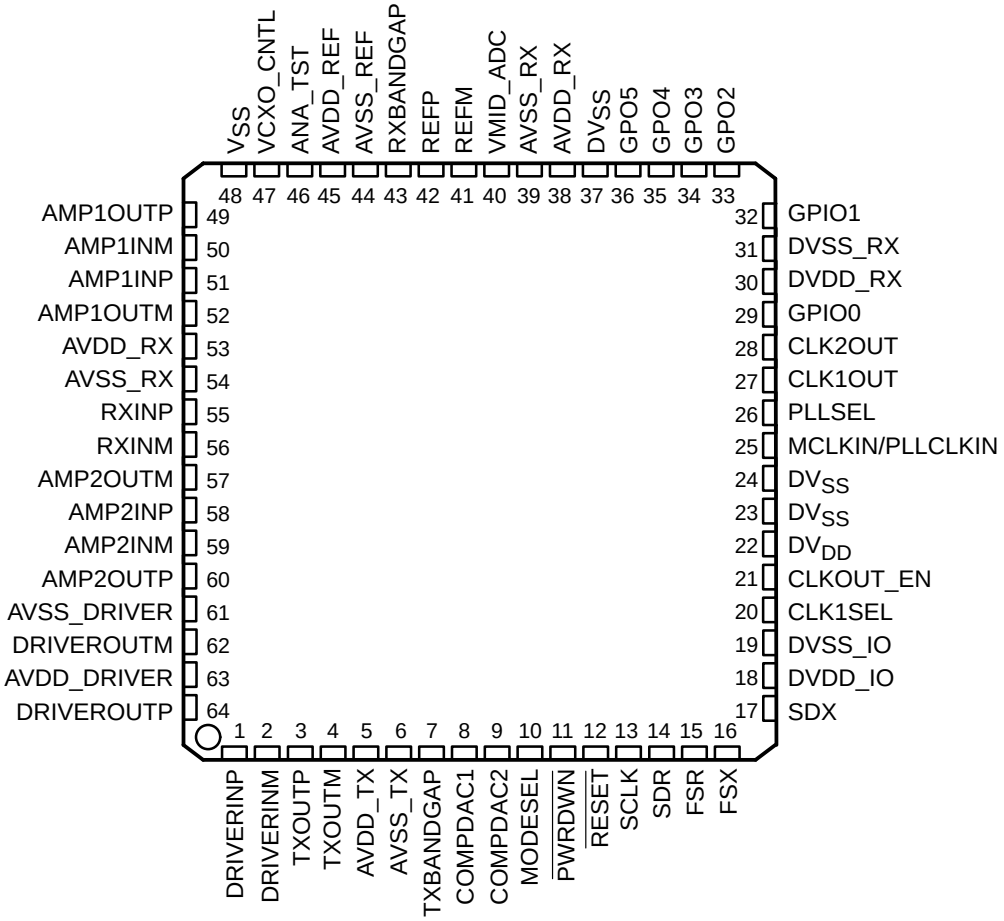
The TLFD600PAP is a high-speed, programmable, analog front end for customer premise equipment (CPE) modems that supports G.lite (G.992.2) and full rate (G.992.1) ADSL applications and incorporates both the codec and line drivers and receiver. The codec also coexists with home phoneline networking alliance (HPNA)-devices, with the ability to work together with up to three HPNA devices connected to the same line. The device performs transmit encoding (D/A conversion), receive decoding (A/D conversion), transmit and receive filtering functions, receive equalizer, and programmable gain amplifications (PGA). The device also incorporates a voltage compensated crystal oscillator (VCXO) DAC, DPLL, line driver, and receiver for TX and RX channels which reduces the number of system components. Two auxiliary amplifiers are provided, on-chip, for additional onboard filtering and amplification with additional off-chip passive components. The receive channel has an update rate of 1.104 Msps in the G.lite mode and 2.208 Msps in the full rate mode. The transmit channel has an update rate of 276 Ksps and 552 Ksps.

A simple serial interface on the digital side reduces system component count. Both data and control share the same serial port. The interface can connect directly to the TI C6000 and C5000 families of DSP chips.

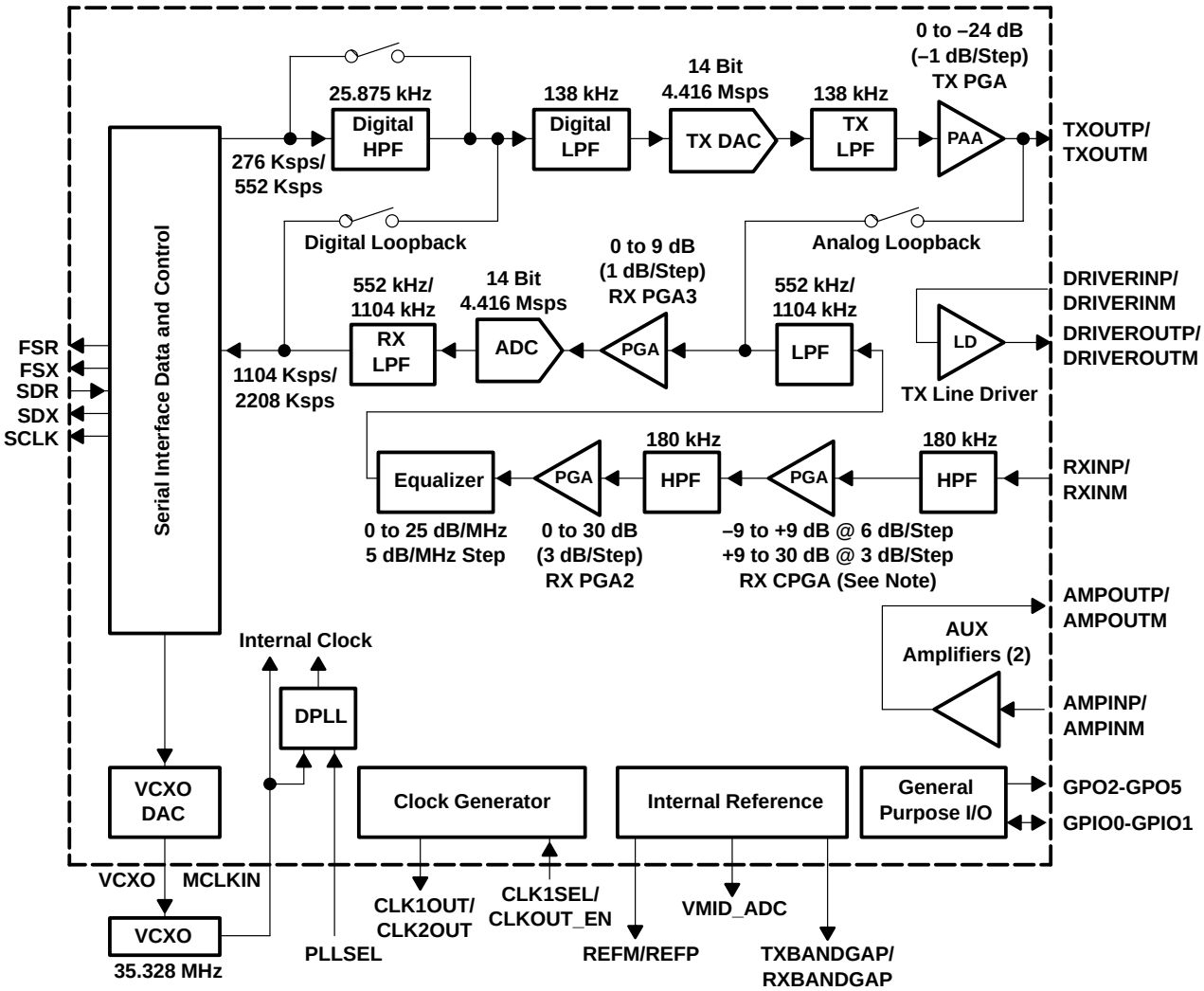
The device operates using 3.3-V and 12-V supply lines (12 V is used for the on-chip TX line driver) and is packaged in a single 64-pin PAP (PowerPAD™) package. It is characterized for operation from –40°C to 85°C.

pinout

PAP PACKAGE
(TOP VIEW)



functional block diagram



NOTE: The CPGA gain range setting is related to the external components (R and C) that are connected to RXINP/M. Refer to the receiver channel section for details.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AMP1INM AMP2INM	50 59	I	Auxiliary amplifier 1 and 2 negative input
AMP1INP AMP2INP	51 58	I	Auxiliary amplifier 1 and 2 positive input
AMP1OUTM AMP2OUTM	52 57	O	Auxiliary amplifier 1 and 2 negative output
AMP1OUTP AMP2OUTP	49 60	O	Auxiliary amplifier 1 and 2 positive output
ANA_TST	46	I	External resistor connection input. A 15-kΩ (±5%) resistor must be connected between ANA_TST and analog ground.
AVDD_DRIVER	63	I	Analog power supply for TX driver (12 V)
AVDD_REF	45	I	Reference analog supply
AVDD_RX	38, 53	I	RX channel filter analog supply
AVDD_TX	5	I	TX channel analog supply
AVSS_DRIVER	61	I	TX driver analog supply return (analog ground)
AVSS_REF	44	I	Reference analog supply return (analog ground)
AVSS_RX	39, 54	I	RX channel filter analog supply return (analog ground)
AVSS_TX	6	I	TX channel analog supply return (analog ground).
CLK1OUT	27	O	Generates clock of frequency MCLKx4/n, where n is 7 or 9. Value of n is selected by CLK1SEL.
CLK2OUT	28	O	Generates clock of frequency MCLKx4/34.5.
CLK1SEL	20	I	Selects whether n = 7 or 9 for CLK1OUT. For CLK1SEL = 0, n = 6.
CLKOUT_EN	21	I	Enable CLK1OUT and CLK2OUT when CLKOUT_EN is high. The default state of CLKOUT_EN is low.
COMPDAC1	8	I	TX channel decoupling cap input A. Add a 1-μF ceramic capacitor to analog power supply.
COMPDAC2	9	I	TX channel decoupling cap input B. Add a 1-μF ceramic capacitor to analog power supply.
DRIVERINM	2	I	TX channel driver negative input. A 0.1-μF capacitor is needed when it connects to TXOUTM.
DRIVERINP	1	I	TX channel driver positive input. A 0.1-μF capacitor is needed when it connects to TXOUTP.
DRIVEROUTM	62	O	TX channel driver negative output
DRIVEROUTP	64	O	TX channel driver positive output
DV_{DD}	22	I	Digital power supply
DVDD_IO	18	I	Power supply for digital I/O buffer
DVDD_RX	30	I	RX channel digital power supply
DV_{SS}	23, 24, 37	I	Digital ground
DVSS_IO	19	I	Digital I/O buffer supply return (digital ground)
DVSS_RX	31	I	RX channel digital supply return (digital ground)
FSX	16	O	Serial port frame sync transmit signal
FSR	15	O	Serial port frame sync receive signal
GPIO0 GPIO1	29 32	I/O	General-purpose I/O
GPO2–5	33–36	O	General-purpose output
MCLKIN/PLLCLKIN	25	I	Master clock input for normal mode (use off-chip VCXO) and DPLL (use fix input clock and change clock phase by control register) mode. The required input clock frequency is 35.328 MHz ±50 ppm.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MODESEL	10	I	Mode selection. MODESEL = 0 enable full rate mode. MODESEL = 1 enable G.lite mode. The default state of this pin is low. The chip goes with the setting of the register programming, if the configuration is different with this pin.
PLLSEL	26	I	DPLL mode selection. PLLSEL = 1 will enable DPLL mode. The default state of this pin is low.
$\overline{\text{PWRDWN}}$	11	I	Power-down pin. When $\overline{\text{PWRDWN}}$ is pulled low, the device goes into power-down mode.
REFM	41	O	Voltage reference filter negative output. There are two capacitors, with values of 10 μF and 0.1 μF, connected in parallel to analog ground. The nominal dc voltage at this terminal is 0.5 V.
REFP	42	O	Voltage reference filter positive output. There are two capacitors, with values of 10 μF and 0.1 μF, connected in parallel to analog ground. The dc voltage at this terminal is 2.5 V.
$\overline{\text{RESET}}$	12	I	Device reset input pin. Initializes all of the device's internal registers to their default values when $\overline{\text{RESET}}$ is pulled low.
RXBANDGAP	43	O	RX channel bandgap filter node. This terminal is provided for decoupling of the 1.5-V band gap reference. There are two capacitors, with values of 10 μF and 0.1 μF, connected in parallel to analog ground. This node should not be used as a voltage source.
RXINM	56	I	RX channel stage negative input. This pin should not be directly connected. Refer to *receive channel* for configuration.
RXINP	55	I	RX channel stage positive input. This pin should not be directly connected. Refer to *receive channel* for configuration.
SCLK	13	O	Serial port shift clock (for both transmit and receive)
SDR	14	I	Serial data receive
SDX	17	O	Serial data transmit
TXBANDGAP	7	O	TX channel band gap filter node. This terminal is provided for decoupling of the 1.5-V band gap reference. There are two capacitors, with values of 10 μF and 0.1 μF, connected in parallel to analog ground. This node should not be used as a voltage source.
TXOUTP	3	O	TX channel positive output
TXOUTM	4	O	TX channel negative output
VCXO_CNTL	47	O	DAC output to control off-chip VCXO
VMID_ADC	40	O	Decoupling VMID for ADC. Add a 10-μF and a 0.1-μF capacitor between this pin and analog ground.
V_{SS}	48	I	Substrate. Connect to analog ground

detailed description

transmit channel

The transmitter channel is powered by a high performance DAC. This is a 4.416 MHz, 14-bit DAC that provides 16X over-sampling to reduce the DAC noise. A band pass filter limits the output of the transmitter from 28.875 kHz to 138 kHz. A programmable attenuation with a range of 24 dB, in 1 dB step size, drives the output into the on-chip ADSL line driver (ac-coupling is needed). The 25.875-kHz digital high pass filter (HPF) can be bypassed by register programming.

The interface transfer rate is either 276 kHz or 552 kHz, controlled by register programming. The 138-kHz low pass filter edge is programmable and is controlled by bit D4 of FMR register. D4=0 selects 138-kHz (±3.5%) pole, while D4=1 selects a 125-kHz (±3.5%) pole. For details of register programming, see register programming section.

The output spectrum of the DAC complies with the nonoverlapped PSD mask specified in the ITU standard G.992.2 for G.lite application and G.992.1 for full rate application.

transmit channel(continued)

The line driver is also integrated in the TX channel. It helps optimize system components, board size, and cost. The driver is powered by a 12-V, supply and has a fixed gain of 15.7 dB. This provides a maximum drive of 18.2 Vp-p differential output when the input is 3 Vp-p (maximum input range). Thus, a transformer with 1:2 ratio is needed for ADSL modem application. The minimum load that the driver can drive is 33 Ω, thus, making the part coexist with up to 3 HPNA devices connected to the same line.

The line driver has separate input and output pins. This gives flexibility to add additional filters in the transmit path. The line driver can be powered down by register programming.

The TXOUTP and TXOUTM pins must be ac-coupled to the DRIVERINP and DRIVERINM through 0.1-μF capacitors, as the common mode voltage on the pin pairs are different (1.5 Vdc on TXOUTP/M and 6 Vdc on DRIVERINP/M). They must not be dc-coupled.

receive channel

The receiver channel consists of a coarse programmable gain amplifier (CPGA), analog high-pass and low-pass filters, two programmable gain amplifiers, ADC, and a digital filter. In addition, it adds an equalizer to obtain maximum system performance. The receive signal is processed in a fully differential way.

The ADC in the receiver channel is a 4.416-MHz, 14-bit converter. The interface transfer rate is either 1104 kHz or 2208 kHz, depending on the mode at operation. 1104 kHz is used for G.lite mode, and 2208 kHz is used for full rate mode. The mode can be selected either by pin 10 (MODESEL) or register programming. The related cutoff frequency of analog and digital filters is also changed with the mode selection.

The high-pass analog filter is used to reject the near end echo and maximize the dynamic range of the ADC. The high-pass filter edge is programmable and is controlled by bit D2 of FMR register. D2 = 0 selects a 180-kHz (±3.5%) pole, while D2 = 1 selects a 168-kHz (±3.5%) pole.

After the high-pass filtering stage, the receiver channel has two PGAs. A 552-kHz/1104-kHz low-pass filter with a 25-dB shape equalizer goes after them and antialiases the analog signal before it goes through the ADC. The RX low pass filter is also designed to reject the out-of-band HPNA signal. Next is a fine gain adjustment PGA of 0 to 9 dB, in 1-dB steps. All the RX PGAs and equalizer are controlled via the register programming.

External components are required to implement CPGA function. Suggested components and connection are shown in the Figure 1.

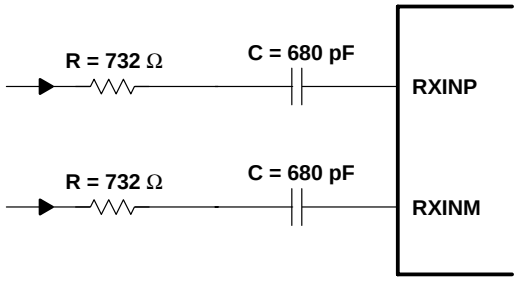


Figure 1. External Components for RXINP and RXINM

The configuration of Figure 1 gives the following setting for CPGA: –9dB to 9dB in 6 dB/steps and 9 dB to 30 dB in 3 dB/steps. The CPGA gain range is controlled by external resistors (732 Ω shown in Figure 1). The cut-off frequency of the HPF is controlled by external resistors (R) and capacitors (C). To keep the cutoff frequency of the first HPF unchanged, R × C need to be constant.

receive channel (continued)

For example: If R = 2063 Ω, the external capacitor (C) needs to be 240 pF. The gain setting for CPGA changes to the following range: –18 dB to 0 dB in 6 dB/steps and 0 dB to 21 dB in 3 dB/steps. The 9 dB shifting is calculated by using the following equation:

$$20 \times \log\left(\frac{2063}{732}\right) = 9 \text{ dB}$$

The linearity of the external capacitors and inductors is very important to the whole RX channel performance. Capacitors of NPO grade or better need to be used.

clock control-VCXO

A 12-bit, serial DAC is used to control the external 35.328-MHz VCXO (voltage control oscillator) that provides the system clock to the CODEC. Two 8-bit registers, (each 2s complement) VCRM and VCRL, are used to generate the 12-bit control code. This implies using two 8-bits to obtain a 12-bit code. The VCRM register occupies the most significant 8 bits in the 12-bit code and the lower 4 bits of the VCRL register (VCRL[3:0]) are used for the low 4 bits of the 12-bit code. The internal DAC register is updated only when VCRL is programmed.

Table 1 shows some representative analog outputs.

Table 1. VCXO DAC Digital-Analog Mapping

OPERATION	HEX RESULT	ANALOG OUTPUT	COMMENTS
VCRM[7:0] × 2^4 + VCRL[3:0]	0x800	0 V	Min scale
	0x801	ΔV	Just above min
	…	…	…
	0xFFF	2047ΔV	Just below mid
	0x000	2048ΔV	Mid scale
	0x001	2049ΔV	Just above mid
	…	…	…
	0x7FE	4094ΔV	Just below max
	0x7FF	4095ΔV	Max scale

Where step-size, Δ = (3/4095) V.

1. The analog output is computed as follows: ((VCRM[7:0] × 2^4 + VCRL[3:0]) + 2048(decimal)) × Δ.

2. Step-size Δ is computed as follows: 0 x 800 (–2048 decimal) is 0 V and 0x7FF (2047 decimal) is 3 V. Thus, Δ = (3 – 0) / (2047 – (–2048)) V = (3/4095) V

clock generation

The clock generation block provides the necessary clocks for the different functional blocks on the board with minimum skew and jitters. This is closely dependent on the performance of the external VCXO. The external VCXO specification is:

- 3.3-V supply
- 35.328 MHz ±50 PPM
- Minimum duty cycle is 60/40 (50/50 is the best)

The on-chip clocks are shown in Table 2. CLK1OUT and CLK2OUT can be used as general clock sources, or they can be disabled if they are not used.

clock generation (continued)

Table 2. Clock Description

CLOCK	FREQUENCY (MHz)		SYMMETRY
	CLKOUT_EN = 1		
	CLK1SEL = 0	CLK1SEL = 1	
SCLK	35.328	35.328	50/50
CLK1OUT	20.187	15.701	43/57 for 20.187 44/56 for 15.701
CLK2OUT	4.096	4.096	49/51

serial interface

The serial interface on the TLFD600PAP will connect gluelessly to the C5000 or C6000 families of DSPs from Texas Instruments. The serial interface operates at 35.328 MHz. The serial port is made up of five signals: SCLK, FSX, FSR, SDX, and SDR. A typical connection diagram is shown in Figure 2.

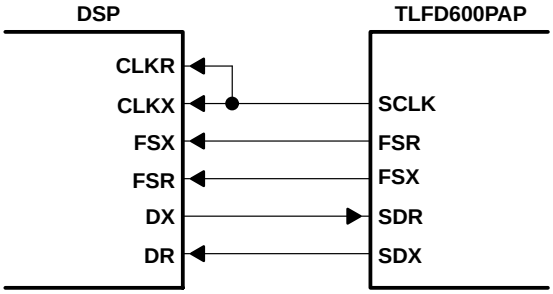


Figure 2. Typical Serial Port Connection

The serial port utilizes a primary/secondary scheme to transfer conversion data and control register data (command). A primary transfer is used to transfer conversion data. A secondary transfer is used to transfer control data when requested by the host processor. The host processor requests a secondary transfer by using the LSB of the SDR data of the primary transfer. A value of 1 indicates a secondary transfer request. Once the secondary request is made and the primary transfer has completed, a secondary FSR pulse is transmitted to the host processor to indicate the beginning of the secondary transfer. The secondary FSR signal arrives 48 SCLKs after the host processor request. Each bit is read/written at the rising edge of SCLK clock. Data bit mappings and example data transfers are shown in Table 3.

Table 3. SDR LSB Control Function

CONTROL BIT D0	CONTROL BIT FUNCTION
0	No secondary transfer requested
1	Secondary transfer requested

primary transfer data mapping

The data bit mapping of a primary transfer is shown in Figure 3. D15–D2 bits of the SDR data stream are DAC data. D1 is unused. D0 is the secondary transfer request bit. When a 1 is written to D0, the host is requesting a secondary data transfer.

In the SDX data stream, D15–D2 contain the ADC conversion data. D1 and D0 can be configured to reflect the values of GPIO0 and GPIO1, when they are configured as inputs. D1 and D0 will contain zeroes if they are not configured to reflect their corresponding GPIO pin value, or if the GPIO pin is configured as an output. To configure D1 and D0 to reflect the GPIO values, the proper bit in the control register needs to be set.

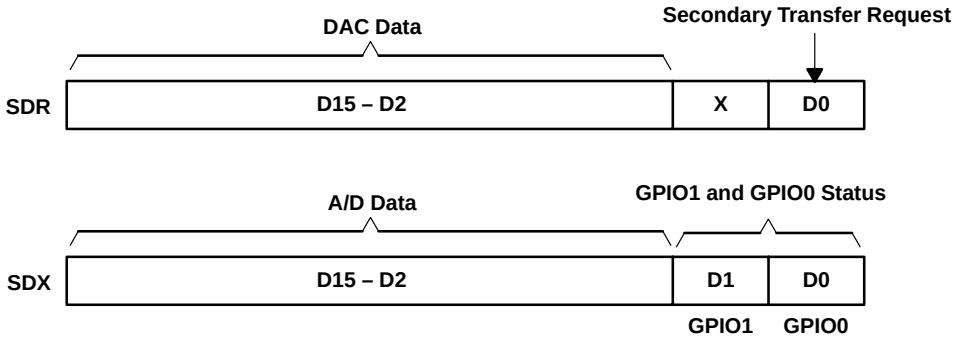


Figure 3. Primary Transfer Data Bit Mapping

secondary transfer data mapping

Secondary serial communication is used to configure the device. The data bit mapping for a secondary transfer is shown in Figure 4. The D14–D10 bits of the SDR data, from the host, are the address bits of the control register involved in the transfer. Bits D7–D0 contain the data to the register. D15 needs to be set to zero all the time.

A control register read-back function is not supported. As a result, there is no secondary FSX or SDX.

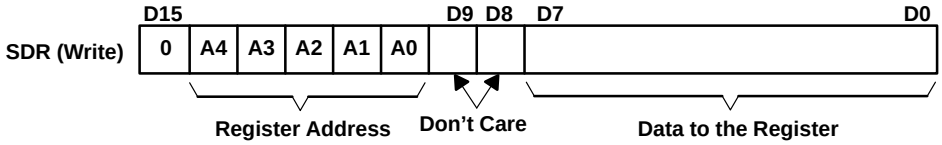


Figure 4. Secondary Transfer Data Bit Mapping

example data transfers

Figure 5 and 6 show the timing relationship for SCLK, FSX, SDX, FSR, and SDR in a primary or secondary communication. The update rate for TX and RX are controlled by pin configuration and register programming. The timing sequence for this operation is as follows:

1. FS is brought high and remains high for one SCLK period, then goes back low.
2. A 16-bit word is transmitted from the ADC (SDX) and a 16-bit word is received for DAC conversion (SDR).

Figure 5 through 14 show the timing relationship of the data transfers with and without secondary request.

example data transfers (continued)

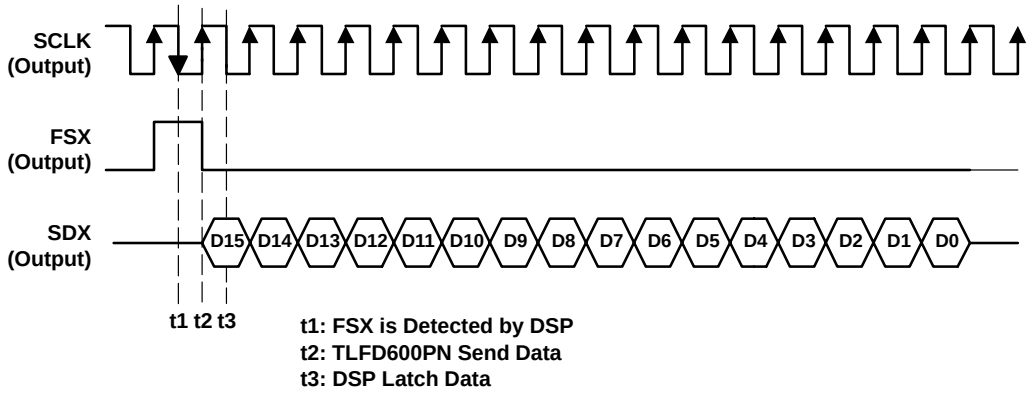


Figure 5. Example Data Transfers (TLFD600PAP to DSP)

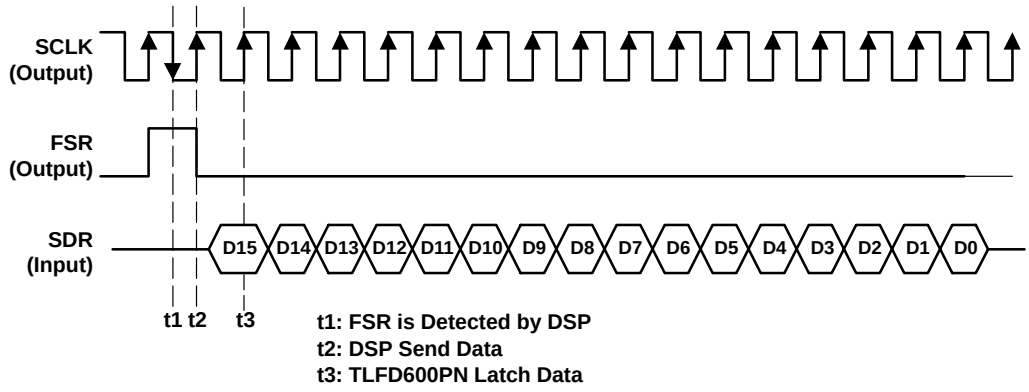


Figure 6. Example Data Transfers (DSP to TLFD600PAP)

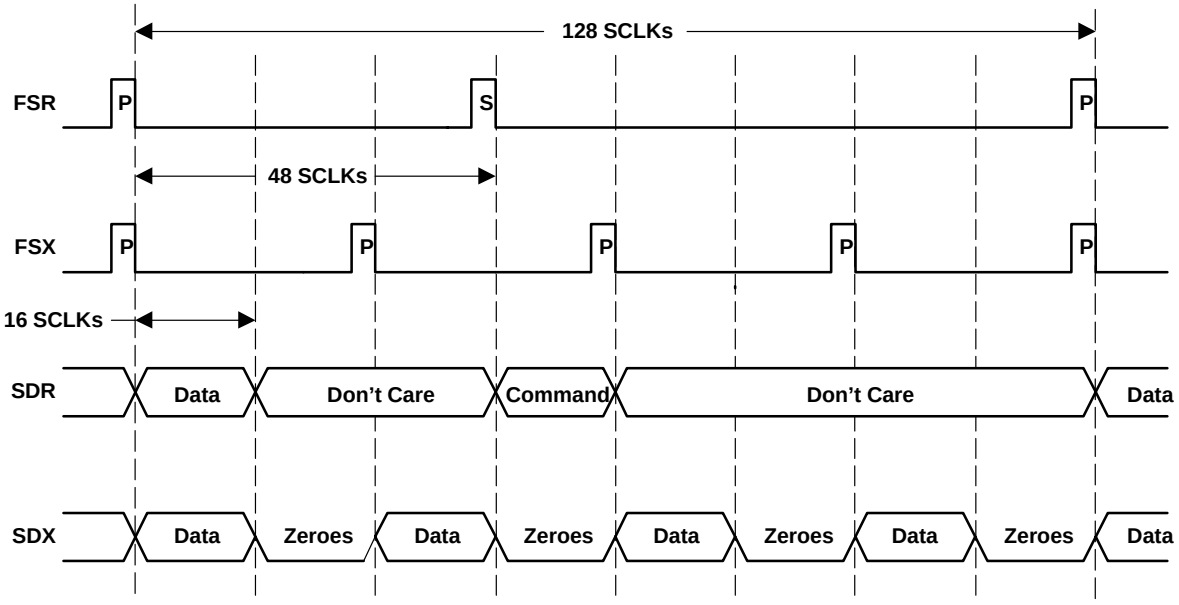


Figure 7. Example Data Transfers With Secondary Request in G.Lite and Normal TX Mode (276 Ksps for TX/FSR and 1104 Ksps for RX/FSX)

example data transfers (continued)

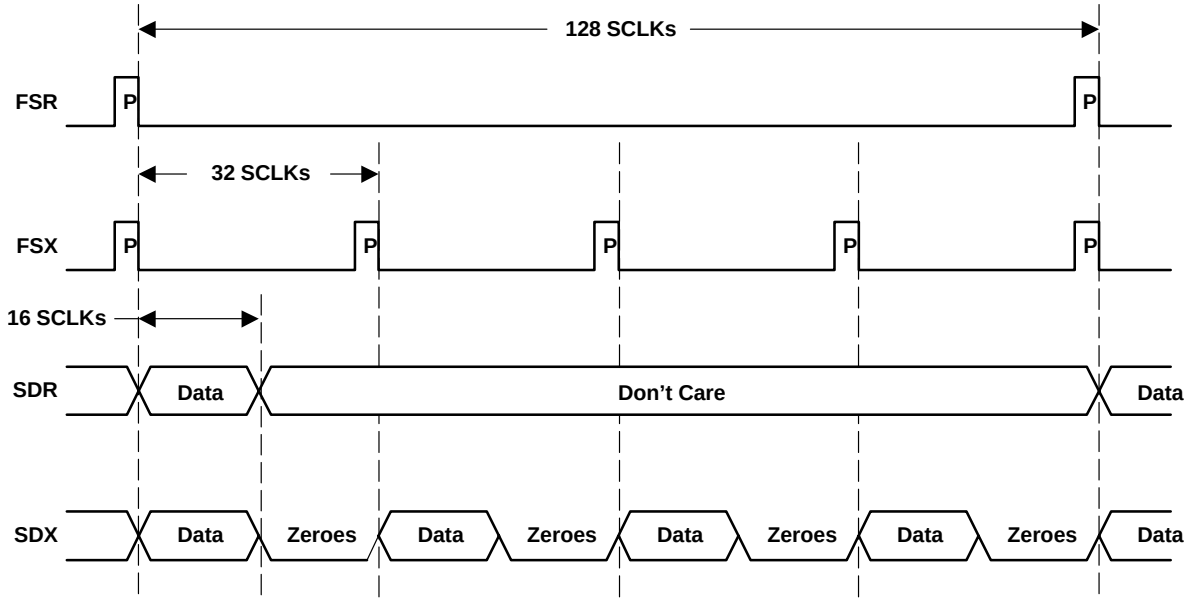


Figure 8. Example Data Transfers Without Secondary Request in G.Lite and Normal TX Mode (276 Ksps for TX/FSR and 1104 Ksps for RX/FSX)

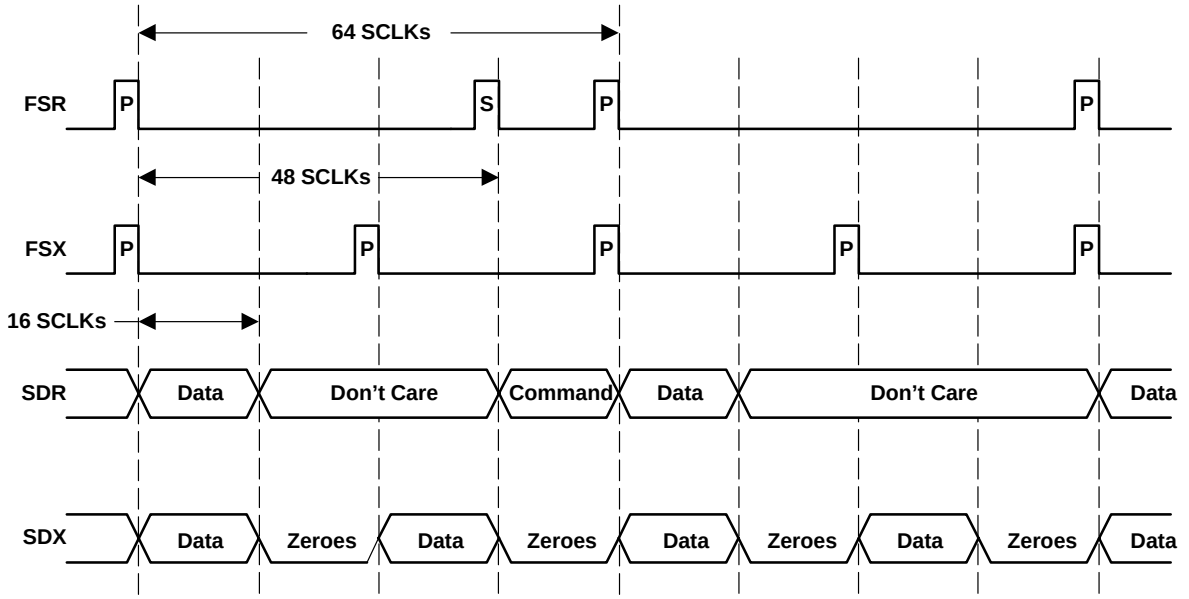


Figure 9. Example Data Transfers With Secondary Request in G.Lite and Double TX Mode (552 Ksps for TX/FSR and 1104 Ksps for RX/FSX)

example data transfers (continued)

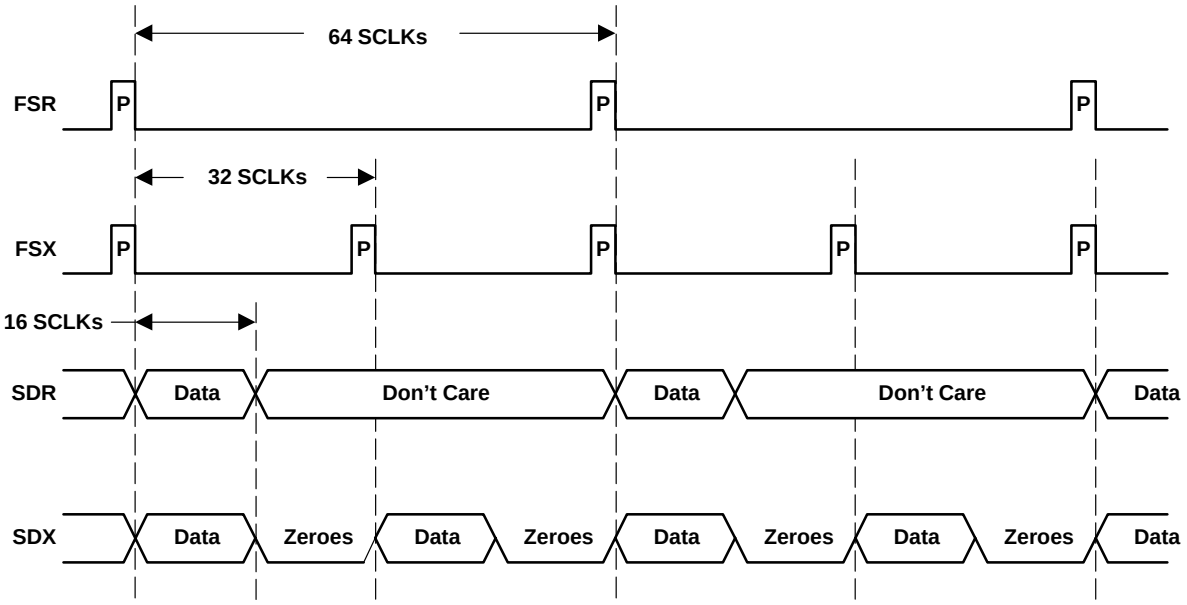


Figure 10. Example Data Transfers Without Secondary Request in G.Lite and Double TX Mode (552 Ksps for TX/FSR and 1104 Ksps for RX/FSX)

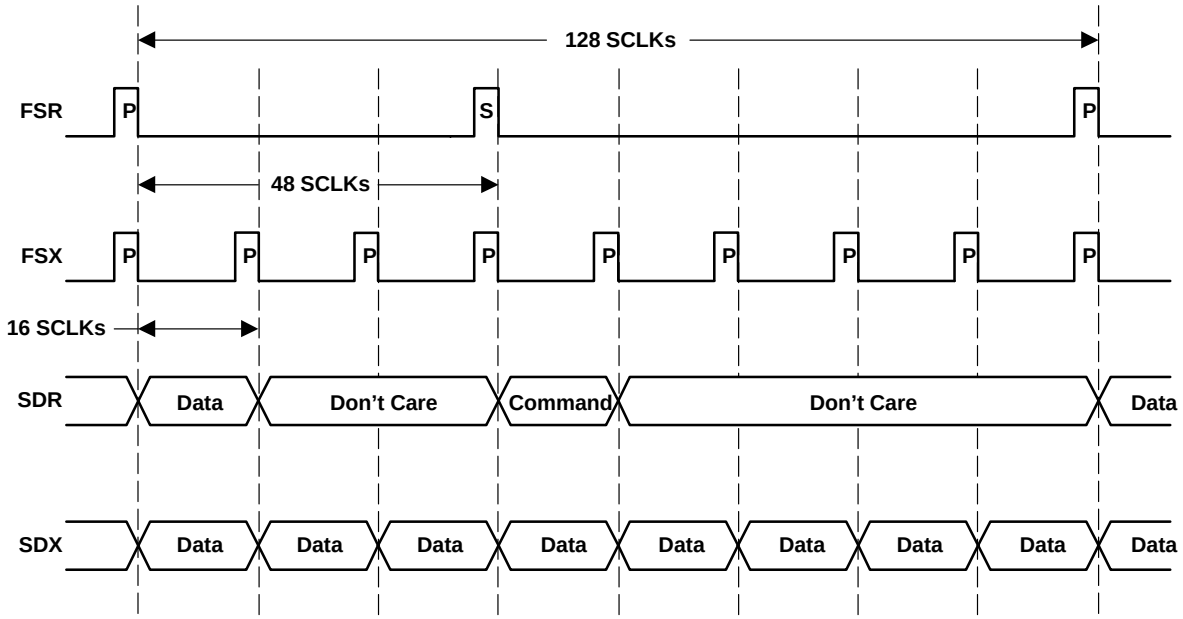


Figure 11. Example Data Transfers With Secondary Request in Full Rate and Normal TX Mode (276 Ksps for TX/FSR and 2208 Ksps for RX/FSX)

example data transfers (continued)

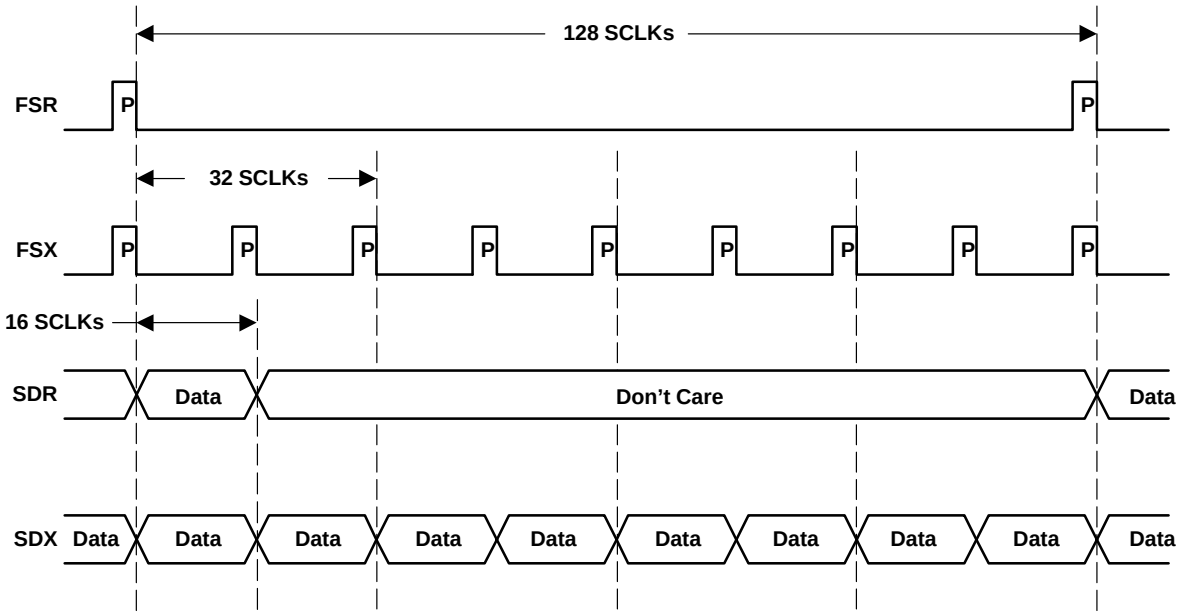


Figure 12. Example Data Transfers Without Secondary Request in Full Rate and Normal TX Mode (276 Ksps for TX/FSR and 2208 Ksps for RX/FSX)

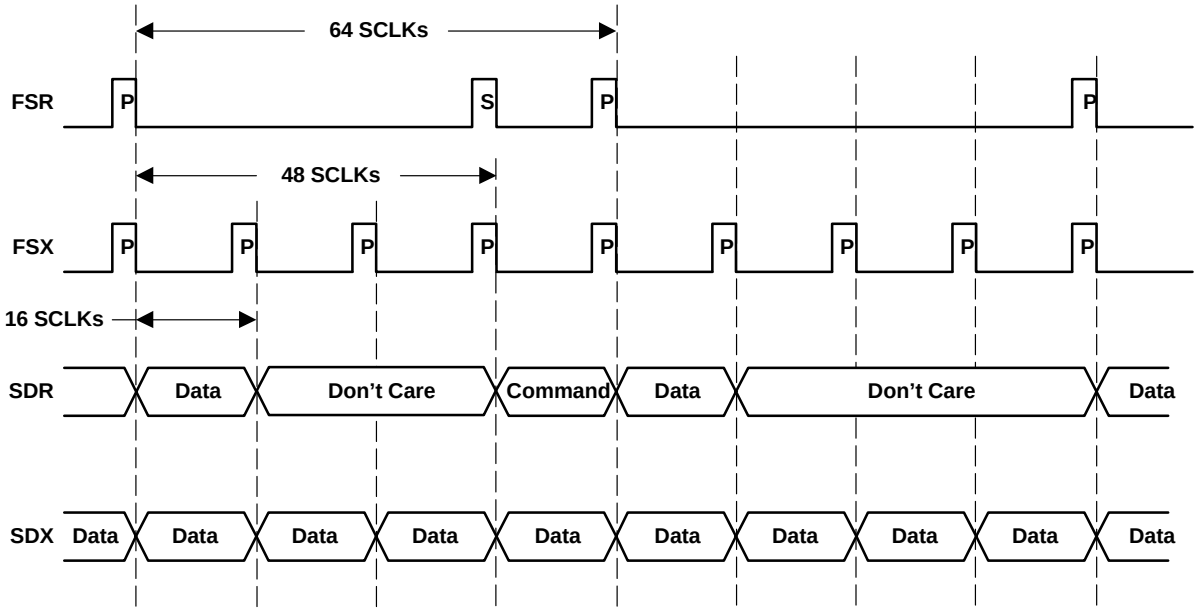


Figure 13. Example Data Transfers With Secondary Request in Full Rate and Double TX Mode (552 Ksps for TX/FSR and 2208 Ksps for RX/FSX)

example data transfers (continued)

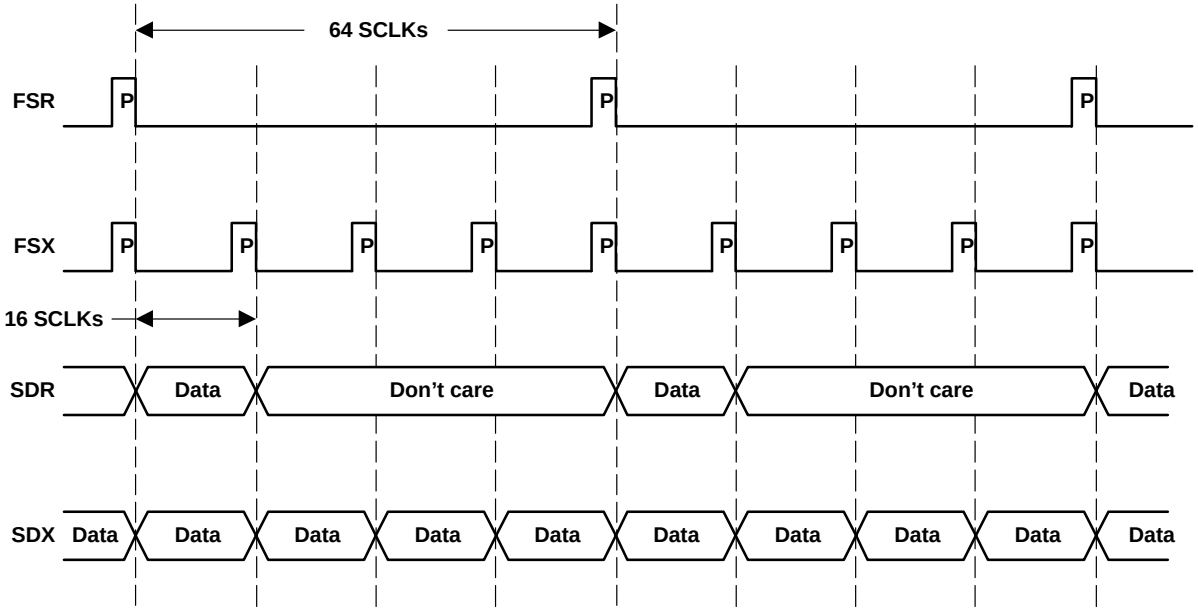


Figure 14. Example Data Transfers Without Secondary Request in Full Rate and Double TX Mode (552 Ksps for TX/FSR and 2208 Ksps for RX/FSX)

general-purpose I/O port (GPIO)

The general-purpose I/O port provides input/output pins for control of external circuitry or reading status of external devices. GPIO0 and GPIO1 can be configured through the control register as input/output. GPO2 to GPO5 are output only.

The configuration of GPIO0 and GPIO1 pins are controlled by the AUXGPRC register and are reflected in the GPR-D register. The status of GPIO0 and GPIO1 can also be mapped into the lower 2 bits of the SDX (that is, from codec to DSP) data stream during primary data transfers. To map the values of GPIO0 and GPIO1 into the lower 2 bits of the SDX ADC data stream, set the appropriate bit in the main control register (MCR).

Each I/O output is capable of driving 2 mA.

reference system

The integrated reference provides the needed voltage and current to the internal analog blocks. It is also brought out to external pins for noise decoupling.

auxiliary amplifiers

There are two high-performance auxiliary operational amplifiers on-chip for additional onboard filtering and amplification at the appropriate configuration. Each op-amp is differential input and differential output and can be disabled by register programming. The typical specifications are as follows:

DC gain:	126 dB
Bandwidth:	116 MHz
PSRR:	100 dB at dc, 70 dB at 1 MHz and 40 dB at 4 MHz
Input common mode:	1.65-V at 3.3-V power supply
Amplifier input referred noise:	2 nV/$\sqrt{\text{Hz}}$

power down

Both hardware and software power-down modes are provided. Some function blocks can be powered down individually according to the control register setting. A logic-zero on the $\overline{\text{PWRDWN}}$ pin will completely shut down the codec.

device initialization time

$\overline{\text{RESET}}$ must be held at least 20 μs after power up. To reset the reference circuit and registers requires 100 ms. When the chip is woken up from hardware power-down mode, it takes 100 ms to reset the reference circuit before the chip works in normal mode. When the chip is woken up from software power-down mode, only 20 μs is needed before valid data comes out (reference must be kept on). Register values will not change in either wake-up operation.

DPLL description

As an alternative to the VCXODAC and VCXO, an off-chip crystal oscillator (XO) followed by an on-chip digital PLL is also implemented. See Figure 15 for the internal functional block diagram. The input clock (35.328 MHz) goes to a programmable frequency-divider to generate the sampling clock for the ADC and DAC. By changing the divide ratio, the phase of sampling clock for ADC and DAC channels can be adjusted. therefore, setting the PLLSEL (pin 26) high to enable the DPLL mode.

The default value of register NCO_DEF is 64, and it can only be changed internally. With the 35.328-MHz input clock, the output frequency of PLL is 4 x 35.328 = 141.312 MHz. To obtain an ADC clock (ADCCLK) of 4.416 MHz, the divide ratio (controlled by register NCO_DEF and NCO_DELTA) needs to be 32. Increasing or decreasing this ratio (for example, 32.5 or 31.5) temporally can effect the phase of 4.416-MHz sampling clock. See the following example for details.

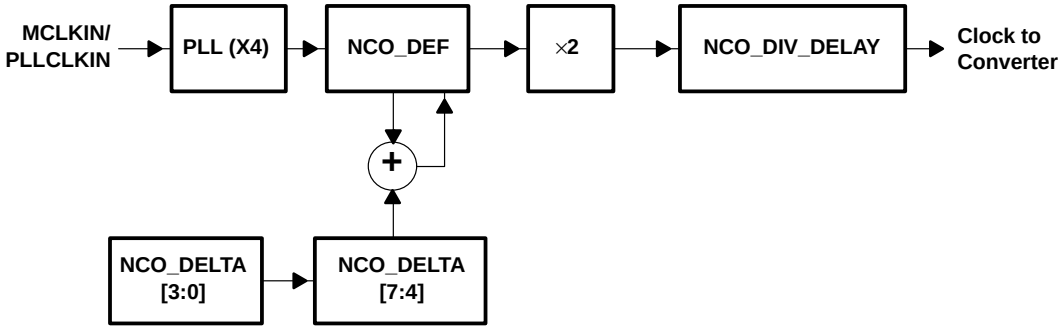


Figure 15. DPLL Internal Functional Block Diagram

Example: MCLKIN/PLLCLKIN = 35.328 MHz. With NCO_DEF defaults at 64, 4.416-MHz clock is provided to the ADC converter by the following equation:

$$4.416 = \left(35.328 \times \frac{4}{64}\right) \times 2$$

If NCO_DELTA [7:4] is set to –1, NCO_DELTA [3:0] is set to 3, and NCO_DIV_DLY is set to 2 (NCO_DIV_DLY should be the last register to be programmed), the internal divider will change to 63 three times. The change of the internal ADC clock will be reflected at the 55th, 71st, and 87th SCLK cycles after NCO_DIV_DLY is programmed. The serial clock normally has a high of 14 ns and a low of 14 ns. The duty cycle of the SCLK changes to 14 ns / 7 ns (14 ns / 21 ns if NCO_DELTA [7:4] = +1) during those jittering SCLK cycles. Reprogramming of the register NCO_DIV_DELAY is needed if further adjustment is required.

DPLL description (continued)

The position of the first jittering SCLK cycle is calculated by using the following equation:

$$(\text{NCO\_DIV\_DLY}\ [7:0] + 1) \times 16 + 7$$

The following jittering SCLKs will separate by 16 SCLK from the first one if NCO_DELTA[3:0] is more than one.

Figures 16 and 17 shows the timing of SCLK at the following setting:

NCO_DELTA [7:4] = –1
NCO_DELTA [3:0] = 2
NCO_DIV_DELAY = 2

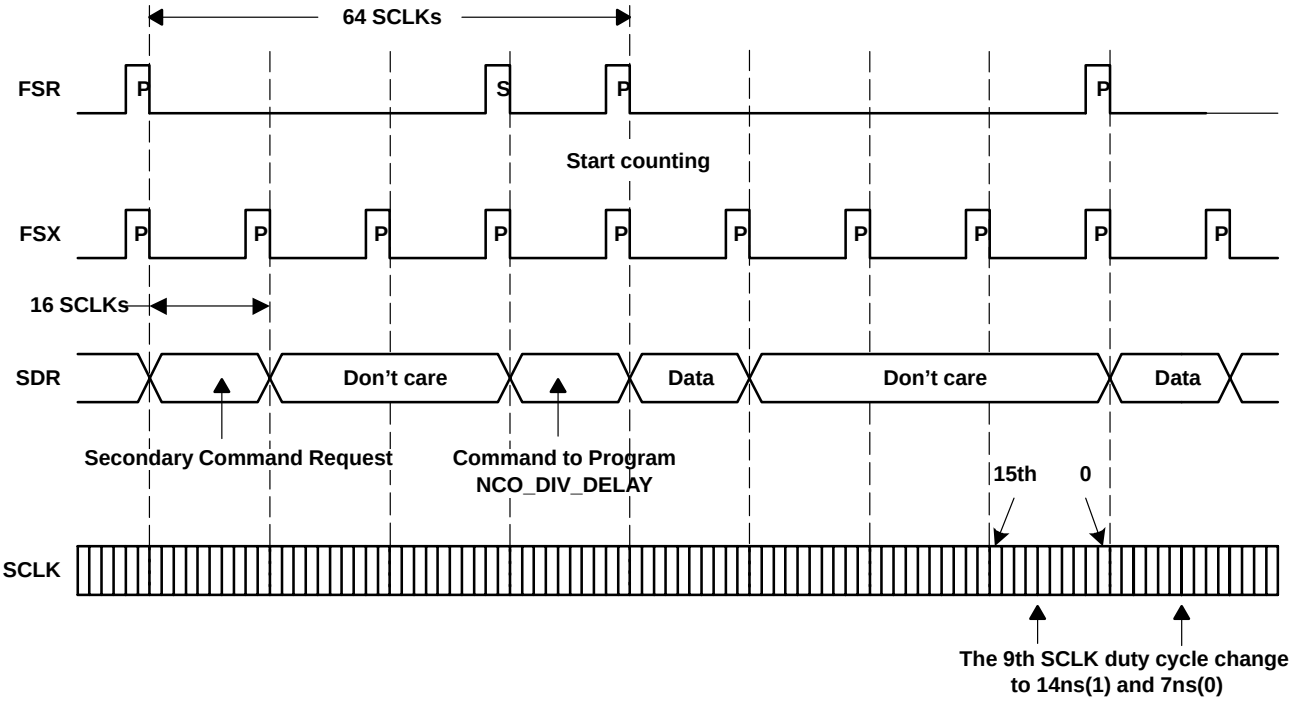


Figure 16. DPLL Operation Example (FSR = 552 kHz and FSX = 2208 kHz)

NOTE: The situation will be the same for FSR = 276 kHz

DPLL description (continued)

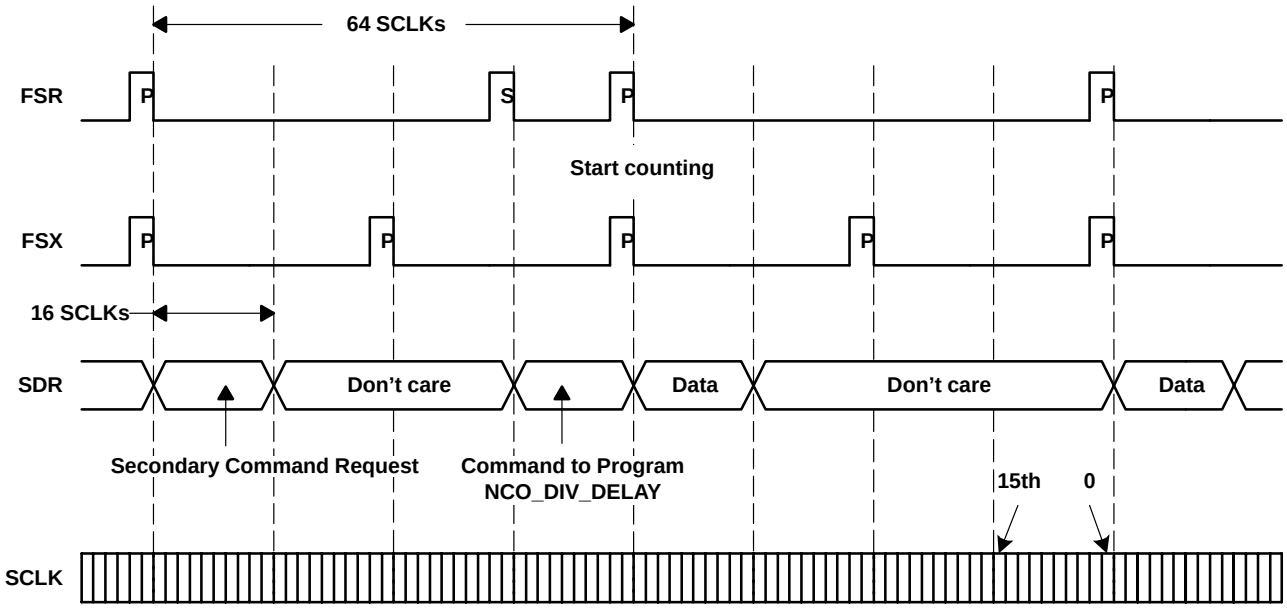


Figure 17. DPLL Operation Example (FSR = 552 kHz and FSX = 1104 kHz)

NOTE: The situation will be the same for FSR = 276 kHz.

register programming

The codec registers are listed below. All registers are 8-bits wide. Bits not defined in Table 4 are reserved for future use. These reserved bits need to be written as zero during register programming.

Table 4. Register Programming

REGISTER		DEFAULT VALUE	FUNCTION
NAME	ADDRESS A4–A0		
BCR	00001	00000000	D2: Bypass TX digital HP filter D3: Echo mode: Echo SDR data on SDX D5: Force all digital outputs high D6: Force all digital outputs low D7: Power-down TX line driver
PCR-RX1	00010	00000000	D[5:2] = RXPGA3[3:0]; Fine gain, 0 to 9 dB, 1 dB step
PCR-RX2	00011	00001011	D[7:4] = RXPGA2[3:0]; 0 to 30 dB, 3 dB step D[3:0] = RXCPGA[3:0]; –9 to 9 dB at 6 dB/step and 9 to 30 dB at 3 dB/step.
PCR-TX	00100	00000000	D[4:0] = TX PAA[4:0]; 0 to –24 dB, –1 dB/step
EQR	00101	00000000	D[2:0] = EQ[2:0]; 0 to 25 dB/MHz, 5 dB/MHz per step
VCR-M	00110	00000000	D[7:0] = VCXO DAC control Bit[11:4]
VCR-L	00111	00000000	D[3:0] = VCXO DAC control Bit[3:0]. D[7:4] must be zero
NOT USED	01000	00000000	Reserved
GPR-D	01001	00000000	D[7:0] = General-purpose I/O data register data
FMR	01010	00000000	D0: G.Lite/full rate mode selection. (0 = same as pin default, 1 = opposite of pin default. See MODESEL in pin description section) D1:TX update rate selection; 276 Ksps (D1 = 0) or 512 Ksps (D1=1) D2:Reserved D3:Reserved D4:Bandwidth selection for TX channel (0 = 138 kHz, 1 = 125 kHz)
AUXGPRC	01011	00001100	D0=1: Enable auxiliary amplifier 2 D1=1: Enable auxiliary amplifier 1 D[3:2] = GPIO0 and GPIO1 I/O control (0 = output, 1 = input)
NCO_DEF	01100	01000000	D[6:0] = Default NCO divide number
NCO_DIV_DLY	01101	00000000	D[7:0] Number of samples (or frames), from current secondary transfer, after which effect of delta will occur. This register should be the last register to be programmed in DPLL mode.
NCO_DELTA	01110	00000000	D[7:4] = Delta from default for first sample of data frame (–1 through 1) D[3:0] = Number of times the internal NCO divider remains changed after register NCO_DIV_DLY is programmed.
MCR	01111	00000000	D0: S/W power down main reference D1: S/W power down TX channel with reference still on D2: S/W power down RX channel with reference still on D3: S/W power down VCXO DAC with reference still on D4: S/W reset D5: Analog loop back D6: Digital loop back D7: Enable GPIO0 and 1 to show in SDX primary data.

NOTE: The gain range of CPGA is related to the external resistor. The gain setting shown above is under the condition of R = 732 Ω and C = 680 pF. Refer to the *receiver channel* section for details.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AVDD to AGND, DVDD to DGND . . . . . –0.3 V to 4.5 V
Supply voltage, AVDD_DRIVER to AGND . . . . . –0.3 V to 15 V
Analog input voltage range to AGND . . . . . See Note 1
Digital input voltage range . . . . . –0.3 V to 4.5 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 120°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The analog input pins (RXINP/RXINM) are virtual ac ground in the normal application mode.

recommended operating conditions

power supply

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	Driver analog supply (AV_{DD}_DRIVER)		12		V
	Analog supply (AVDD_RX, AVDD_REF, AVDD_TX)	3	3.3	3.6	V
	Digital supply (DVDD, DVDD_IO, DVDD_RX)	3	3.3	3.6	V

analog inputs

		MIN	TYP	MAX	UNIT
Full scale range (single ended) at point A and B (see Figure 20)	RX CPGA = –9 dB		4.2		$V_{p–p}$

digital inputs

	MIN	TYP	MAX	UNIT
High-level input voltage, V_{IH}	2.4			V
Low-level input voltage, V_{IL}			0.6	V
High-level input current, I_{IH}		10		μA
Low-level input current, I_{IL}		10		μA

digital outputs

	MIN	TYP	MAX	UNIT
High-level output voltage, V_{OH}	2.4			V
Low-level output voltage, V_{OL}			0.6	V

clock inputs

	MIN	TYP	MAX	UNIT
Input clock frequency		35.328		MHz
Input clock high time	13.5	14.15	15	ns

electrical characteristics, T_A = 25°C, analog power supplies = 3.3 V, digital power supplies = 3.3 V, AVDD_DRIVER = 12 V, f_{CLKIN} = 35.328 MHz (unless otherwise noted)

RX channel

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal bandwidth	High-pass filter	FMR [D2] = 1	162	168	174	kHz
		FMR [D2] = 0	174	180	186	
	Low-pass filter	G.lite mode		552		
		Full rate mode		1104		
Missing tone power ratio (MTPR)	G.lite mode	1. 4.3125 kHz spaced tones from 138 – 552 kHz 2. 422.625 kHz tone is missing		60		dB
	Full rate mode	1. 4.3125 kHz spaced tones from 138 – 1104 kHz 2. 422.625 kHz tone is missing		60		
Group delay distortion		G.lite or full rate mode			10	µs
Gain step error	CPGA	G.lite or full rate mode	–0.5		0.5	dB
	PGA2		–0.5		0.5	
	PGA3		–0.5		0.5	
PSRR	G.lite mode	See Note 2		–70		dB
	Full rate mode	See Note 2		–70		
Input reference noise floor	G.lite mode	CPGA = 21 dB, PGA2 = 30 dB, PGA3 = 9 dB, Equalizer = 0 dB		–150		dBm/Hz
	Full rate mode			–150		
CMRR		G.lite and Full Rate Mode		60		dB

NOTE 2: Inject single tone signal (267.375 kHz) at 200 mVp-p to analog power supplies and measure 267.375 kHz tones at RX output.

electrical characteristics, T_A = 25°C, analog power supplies = 3.3 V, digital power supplies = 3.3 V, AVDD_DRIVER = 12 V, f_{CLKIN} = 35.328 MHz (unless otherwise noted) (continued)

TX channel (TX line driver is not included)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Signal bandwidth	Low-pass filter	FMR [D4] = 0	133	138	143	kHz
		FMR [D4] = 1	121	125	129	
	High-pass filter			25.875		kHz
MTPR	1. 4.3125kHz spaced tones from 25.875 to 138 kHz 2. 81.9375 kHz tone is missing			70		dB
Group delay distortion					10	µs
PAA gain step error			–0.5		0.5	dB
PSRR	See Note 2			–70		dB
Out-of-band noise	See Note 3			–150		dBm/Hz

NOTES: 2. Inject single tone signal (267.375 kHz) at 200 mVp-p to analog power supplies and measure 267.375 kHz tones at RX output.
3. Send multitone signal (25.875 to 138 kHz at 4.3125 kHz/step) at full scale output level and measure signal level beyond 276 kHz at TXOUTP/M.

TX driver (AVDD_DRIVER = 12 V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage swing	Input signal is 138 kHz @ 3 V_{P-P} differential at DRIVERINP/M, R_L = 50 Ω			18.2	V_{P-P}
Output current				220	mA
Output short circuit protection current limit				300	
TSNR	Input 3 V_{P-P} differential @ 138 kHz at DRIVERINP/M		85		dB
DRIVERINP/M	Input impedance		600		Ω

VCXO DAC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		Bits
DNL	Differential nonlinearity			±1		LSB
INL	Integral nonlinearity			±4		LSB
	Monotonicity				12	Bits
	Offset error		–100		100	mV
	Output compliance voltage	Maximum code input with load = 50 kΩ		3		V
	Output load			50		kΩ

power dissipation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog (TX line driver is not included)	All AVDD = 3.3 V		620	695	mW
Digital	All DVDD = 3.3 V		150	165	mW
Fully operational without TX line driver			770	860	mW
TX Driver	Quiescent, AVDD_DRIVER = 12 V		510	570	mW
TX Driver	–47 dBm/Hz DMT signal (PAR = 17 dB) on 50-Ω load, (AVDD_DRIVER = 12 V)		610	690	mW
Fully operational with driver			1380	1530	mW
H/W power down			160	250	mW

electrical characteristics, T_A = 25°C, analog power supplies = 3.3 V, digital power supplies = 3.3 V, AVDD_DRIVER = 12 V, f_{CLKIN} = 35.328 MHz (unless otherwise noted) (continued)

reference voltage

PARAMETER	MIN	TYP	MAX	UNIT
REFP	2.4	2.5	2.6	V
TXBANDGAP, RXBANDGAP	1.4	1.5	1.6	V
REFM	0.4	0.5	0.6	V
VMID_ADC		1.47		V

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

serial port (see Figures 18 and 19)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(1)}$	Delay time, FSX goes high after SCLK↑			4	ns
$t_{d(2)}$	Delay time, FSX goes low after SCLK↑			4	ns
$t_{d(3)}$	Delay time, SDX valid after SCLK↑			4	ns
$t_{d(4)}$	Delay time, FSR goes high after SCLK↑			4	ns
$t_{d(5)}$	Delay time, FSR goes low after SCLK↑			4	ns
t_{su}	Set up time, SDR ready before SCLK↑	6			ns
t_h	Hold time, SDR keep active after SCLK↑	2			ns

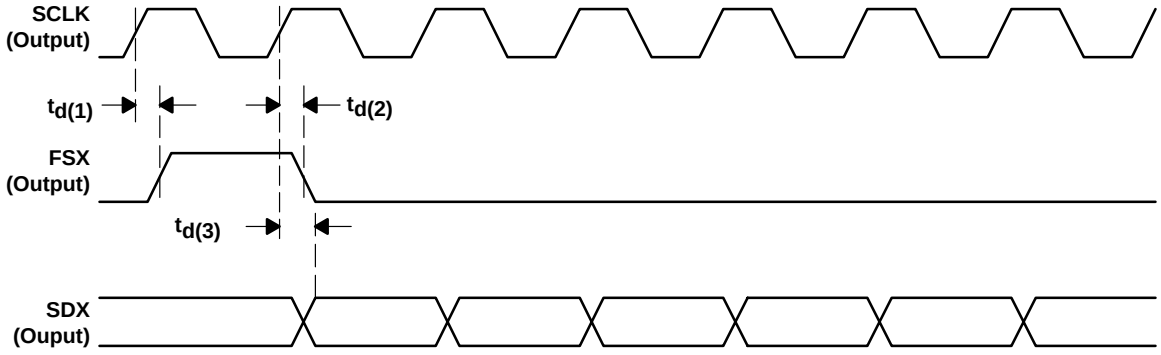


Figure 18. Serial Interface Timing (TX Channel)

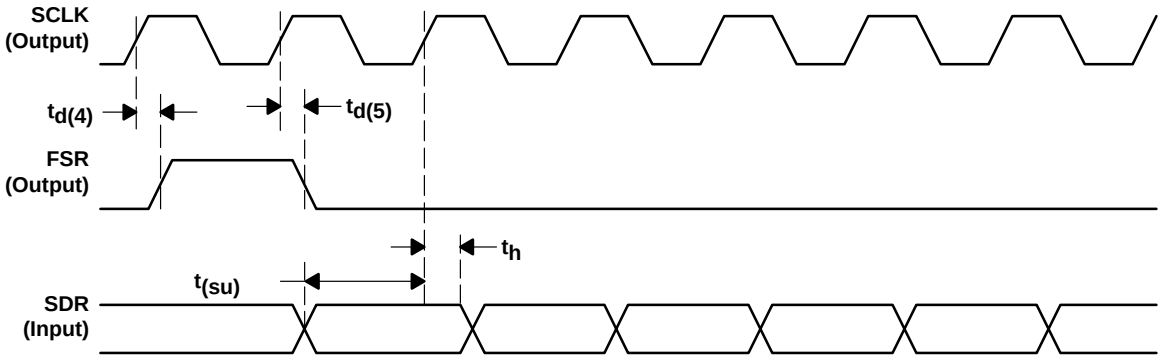


Figure 19. Serial Interface Timing (RX Channel)

APPLICATION INFORMATION

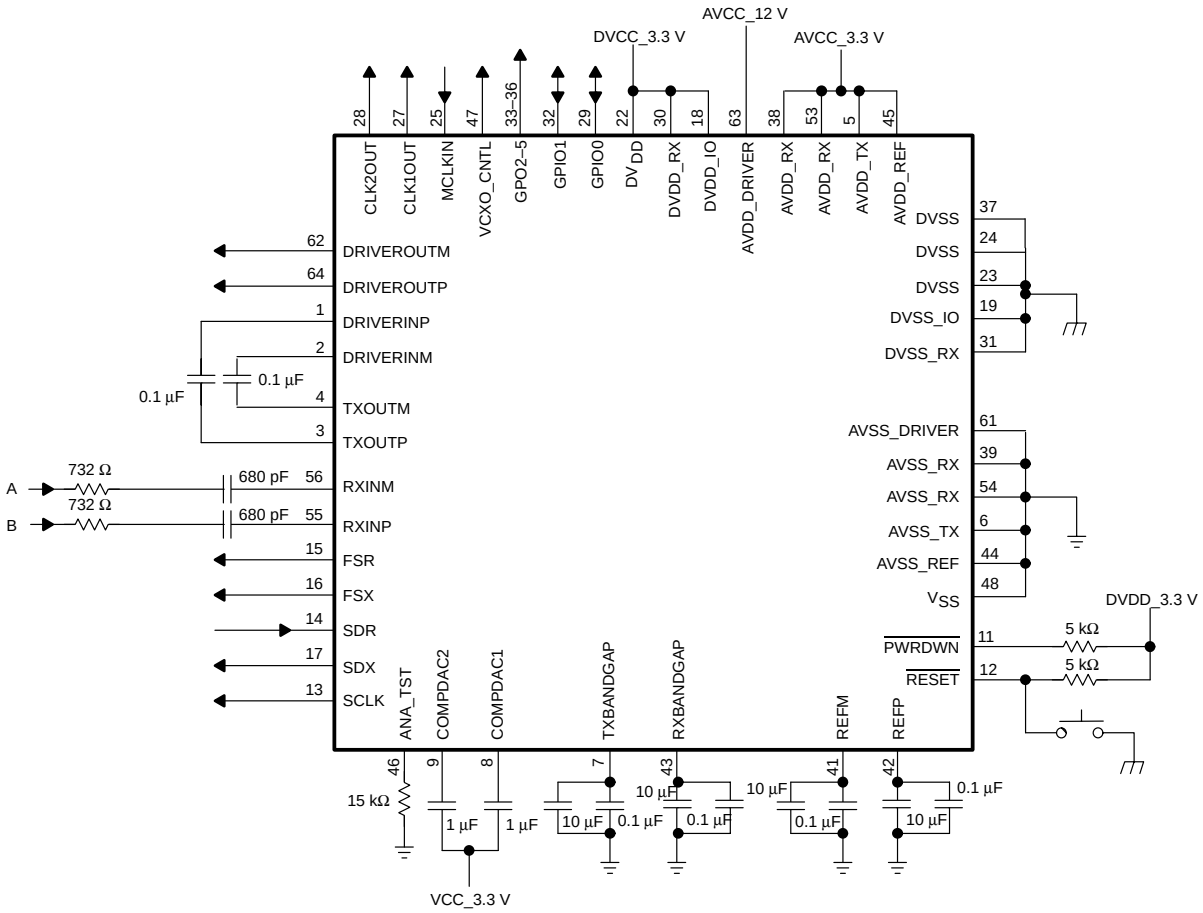


Figure 20. Typical Chip Configuration

PROGRAMMING INFORMATION

BCR – bypass control register

Address: 00001b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
PDTXDR	DIG_LOW	DIG_HIGH	Reserved	ECHO	BPTXHP	Reserved	Reserved

Table 5. BCR Control Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
PDTXDR	1								Power down TX line driver
DIG_LOW		1							Force all digital outputs low
DIG_HIGH			1						Force all digital outputs high
Reserved				0					Reserved bit. See Note 4
ECHO					1				Echo SDR data on SDX. See Note 5
BPTXHP						1			Bypass TX HP Filter (25.875 kHz)
Reserved							0		Reserved
Reserved								0	Reserved

NOTES: 4. All reserved bits should be programmed as 0 during normal application.
5. ECHO mode allows for a quick verification of whether the TLFD600 serial interface is working. It sends back the data from the input data buffer to the output data buffer and does not go through the RX or TX channel.

PCR-RX1 – programmable gain control register 1 for RX channel

Address: 00010b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	RXPGA3[3]	RXPGA3[2]	RXPGA3[1]	RXPGA3[0]	Reserved	Reserved

Table 6. PCR-RX1 Gain Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Reserved	0								Reserved
Reserved		0							Reserved
RXPGA3[3] RXPGA3[2] RXPGA3[1] RXPGA3[0]			0	0	0	0			RX PGA3 = 0 dB
			0	0	0	1			RX PGA3 = 1 dB
			0	0	1	0			RX PGA3 = 2 dB
			0	0	1	1			RX PGA3 = 3 dB
			0	1	0	0			RX PGA3 = 4 dB
			0	1	0	1			RX PGA3 = 5 dB
			0	1	1	0			RX PGA3 = 6 dB
			0	1	1	1			RX PGA3 = 7 dB
			1	0	0	0			RX PGA3 = 8 dB
			1	0	0	1			RX PGA3 = 9 dB
			–	–	–	–			See Note 6 for all other combinations
Reserved							0		Reserved
Reserved								0	Reserved

NOTE 6: Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used.

PROGRAMMING INFORMATION

PCR-RX2 – programmable gain control register 2 for RX channel

Address: 00011b Contents at reset: 00001011b

D7	D6	D5	D4	D3	D2	D1	D0
RXPGA2[3]	RXPGA2[2]	RXPGA2[1]	RXPGA2[0]	RXCPGA1[3]	RXCPGA1[2]	RXCPGA1[1]	RXCPGA1[0]

Table 7. PCR-RX2 Gain Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
RXPGA2[3] RXPGA2[2] RXPGA2[1] RXPGA2[0]	0	0	0	0					RX PGA2 = 0 dB
	0	0	0	1					RX PGA2 = 3 dB
	0	0	1	0					RX PGA2 = 6 dB
	0	0	1	1					RX PGA2 = 9 dB
	0	1	0	0					RX PGA2 = 12 dB
	0	1	0	1					RX PGA2 = 15 dB
	0	1	1	0					RX PGA2 = 18 dB
	0	1	1	1					RX PGA2 = 21 dB
	1	0	0	0					RX PGA2 = 24 dB
	1	0	0	1					RX PGA2 = 27 dB
	1	0	1	0					RX PGA2 = 30 dB
	–	–	–	–					See Note 6
RXCPGA1[3] RXCPGA1[2] RXCPGA1[1] RXCPGA1[0]					0	0	0	0	RXCPGA = 9 dB
					0	0	0	1	RXCPGA = 12 dB
					0	0	1	0	RXCPGA = 15 dB
					0	0	1	1	RXCPGA = 18 dB
					0	1	0	0	RXCPGA = 21 dB
					0	1	0	1	RXCPGA = 24 dB
					0	1	1	0	RXCPGA = 27 dB
					0	1	1	1	RXCPGA = 30 dB
					1	0	0	0	Invalid
					1	0	0	1	RXCPGA = 3 dB
					1	0	1	0	RXCPGA = –3 dB
					1	0	1	1	RXCPGA = –9 dB
					–	–	–	–	See Note 6

NOTE 6. Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used.

PROGRAMMING INFORMATION

PCR-RTX – programmable attenuation control register for TX channel

Address: 00100b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	TXPAA[4]	TXPAA[3]	TXPAA[2]	TXPAA[1]	TXPAA[0]

Table 8. PCR-TX Attenuation Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Reserved	0								Reserved
Reserved		0							Reserved
Reserved			0						Reserved
TXPAA[4] TXPAA[3] TXPAA[2] TXPAA[1] TXPAA[0]				0	0	0	0	0	TX PAA = 0 dB
				0	0	0	0	1	TX PAA = –1 dB
				0	0	0	1	0	TX PAA = –2 dB
				0	0	0	1	1	TX PAA = –3 dB
				0	0	1	0	0	TX PAA = –4 dB
				0	0	1	0	1	TX PAA = –5 dB
				0	0	1	1	0	TX PAA = –6 dB
				0	0	1	1	1	TX PAA = –7 dB
				0	1	0	0	0	TX PAA = –8 dB
				0	1	0	0	1	TX PAA = –9 dB
				0	1	0	1	0	TX PAA = –10 dB
				0	1	0	1	1	TX PAA = –11 dB
				0	1	1	0	0	TX PAA = –12 dB
				0	1	1	0	1	TX PAA = –13 dB
				0	1	1	1	0	TX PAA = –14 dB
				0	1	1	1	1	TX PAA = –15 dB
				1	0	0	0	0	TX PAA = –16 dB
				1	0	0	0	1	TX PAA = –17 dB
				1	0	0	1	0	TX PAA = –18 dB
				1	0	0	1	1	TX PAA = –19 dB
				1	0	1	0	0	TX PAA = –20 dB
				1	0	1	0	1	TX PAA = –21 dB
				1	0	1	1	0	TX PAA = –22 dB
				1	0	1	1	1	TX PAA = –23 dB
				1	1	0	0	0	TX PAA = –24 dB
				–	–	–	–	–	See Note 6

NOTE 6. Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used.

PROGRAMMING INFORMATION

equalizer shape control register

Address: 00101b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	EQS[2]	EQS[1]	EQS[0]

Table 9. EQR Shape Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Reserved	0								Reserved
Reserved		0							Reserved
Reserved			0						Reserved
Reserved				0					Reserved
Reserved					0				Reserved
EQS[2] EQS[1] EQS[0]						0	0	0	RX EQ = 0 dB/MHz
						0	0	1	RX EQ = 5 dB/MHz
						0	1	0	RX EQ = 10 dB/MHz
						0	1	1	RX EQ = 15 dB/MHz
						1	0	0	RX EQ = 20 dB/MHz
						1	0	1	RX EQ = 25 dB/MHz
						–	–	–	See Note 6 for all other combinations

NOTE 6. Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used.

VCR-M – VCXO DAC control register MSB

Address: 00110b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
VCRMM[7]	VCRM[6]	VCRM[5]	VCRM[4]	VCRM[3]	VCRM[2]	VCRM[1]	VCRM[0]

VCR-L – VCXO DAC control register LSB

Address: 00111b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	VCRL[3]	VCRL[2]	VCRL[1]	VCRL[0]

PROGRAMMING INFORMATION

GPR-D – GPIO data register

Address: 01001b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	GPOD[5]	GPOD[4]	GPOD[3]	GPOD[2]	GPOD[1]	GPOD[0]

Table 10. GPIO Control Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	Description
Reserved	0								Reserved
Reserved		0							Reserved
GPOD[5]			0/1						GPO5 = 0/1
GPOD[4]				0/1					GPO4 = 0/1
GPOD[3]					0/1				GPO3 = 0/1
GPOD[2]						0/1			GPO2 = 0/1
GPIOD[1]							0/1		GPIO1 = 0/1 when GPIO1 is configured as output. See Note 7.
GPIOD[0]								0/1	GPIO0 = 0/1 when GPIO1 is configured as output. See Note 7.

NOTE 7: It is recommended to write zeroes to GPIO1 and GPIO0 if they are configured as inputs.

FMR – frequency mode register

Address: 01010b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	SLTXBW	Reserved	SLRXBW	DBLTXS	TOGMOD

Table 11. FMR Control Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Reserved	0								Reserved
Reserved		0							Reserved
Reserved			0						Reserved
SLTXBW				1					TX LPF bandwidth 125 kHz
SLTXBW				0					TX LPF bandwidth 138 kHz
Reserved					0				Reserved
SLRXBW						0			Reserved
DBLTXS							1		TX FSR sampling at 552 Ksps
DBLTXS							0		TX FSR sampling at 276 Ksps
TOGMOD								1	Work mode (G.lite/full rate) opposite of that selected by MODESEL pin
TOGMOD								0	Work mode (G.lite/full rate) as selected by MODESEL pin

NOTE 8: Table 12 shows the effect of MODESEL pin (pin 10) and TOGMOD bit (FMR[0]).

PROGRAMMING INFORMATION

Table 12. Mode Selection Table

INPUTS		OUTPUT	COMMENTS
MODESEL PIN (PIN 10)	TOGMOD BIT (FMR[0])	RESULTANT MODE	
0	0	Full rate	RX analog and digital LPF at 1104 kHz
0	1	G.lite	RX analog and digital LPF at 552 kHz
1	0	G.lite	RX analog and digital LPF at 552 kHz
1	1	Full rate	RX analog and digital LPF at 1104 kHz

AUXGPRC – auxiliary amplifier and GPR direction control register

Address: 01011b Contents at reset: 00001100b

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	GPIOC[1]	GPIOC[0]	AMP1EN	AMP2EN

Table 13. AUXGPRC Control Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Reserved	1								Reserved bit
Reserved		1							Reserved bit
Reserved			1						Reserved bit
Reserved				1					Reserved bit
GPIOC[1]					0				Configure pin GPIO1 as output
GPIOC[1]					1				Configure pin GPIO1 as input
GPIOC[0]						0			Configure pin GPIO0 as output
GPIOC[0]						1			Configure pin GPIO0 as input
AMP1EN							0		Enable on-chip auxiliary amplifier 1
AMP2EN								0	Enable on-chip auxiliary amplifier 2

NCO_DEF – numerically controlled oscillator default value register

Address: 01100b Contents at reset: 01000000b (64 decimal)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	NCODEF[6]	NCODEF[5]	NCODEF[4]	NCODEF[3]	NCODEF[2]	NCODEF[1]	NCODEF[0]

NOTE 9: NCO_DEF register should never be written to. It always holds the default value of 64.

PROGRAMMING INFORMATION

NCO_DIV_DELAY – numerically controlled oscillator delay control register

Address: 01101b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
NCDLY[7]	NCDLY[6]	NCDLY[5]	NCDLY[4]	NCDLY[3]	NCDLY[2]	NCDLY[1]	NCDLY[0]

Table 14. NCO Value Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
NCDLY[7:0]	0	0	0	0	0	0	0	0	Invalid
	0	0	0	0	0	0	0	1	ADCLK jittered 1 sample clocks (of ADCLK) after write into the NCO_DIV_DELAY register
	–	–	–	–	–	–	–	–	ADCLK jittered 2 to 255 sample clocks (of ADCLK) after write into the NCO_DIV_DELAY register

NOTE 10: This register is also the only means of communicating to the codec that the ADCLK must be jittered. Thus, not writing a value implies that jitter will not take place even if other registers have non-default values. This register does not remember its value. All other registers store their values unless reset.

NCO_DELTA – numerically controlled oscillator delta value register

Address: 01110b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
NCDEL[3]	NCDEL[2]	NCDEL[1]	NCDEL[0]	NCRPT[3]	NCRPT[2]	NCRPT[1]	NCRPT[0]

Table 15. NCO_DELTA Delta and Repeat Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
NCDEL[3:0]	0	0	0	0					DELTA = 0
	0	0	0	1					DELTA = 1
	1	1	1	1					DELTA = –1
NCRPT[3:0]					0	0	0	0	REPEAT = 0
					0	0	0	1	REPEAT = 1
					–	–	–	–	
					1	1	1	1	REPEAT = 15

NOTE 11: N = NCODEF[6:0] + DELTA, and ADCCLK = (35.328 × 4)/(N/2).

Example:

1. If NCDEL[3:0] = 0000 (DELTA = 0), then N = 64. And ADCCLK = (35.328 × 4)/(N/2).
2. If NCDEL[3:0] = 0001 (DELTA = 1), then N = 65. And ADCCLK = (35.328 × 4)/(N/2).

PROGRAMMING INFORMATION

MCR – master control register

Address: 01111b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0
GP12EN	DLBEN	ALBEN	SWRST	VCDACPD	RXPD	TXPD	SWREFPD

Table 16. MCR Control Table

BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
GP12EN	1								Show GPIO 1, 2 in SDX primary
DLBEN		1							Enable digital loop back
ALBEN			1						Enable analog loop back
SWRST				1					Software reset
VCDACPD					1				Power down VCXO DAC
RXPD						1			Power down RX channel
TXPD							1		Power down TX channel
SWREFPD								1	Power down main reference

NOTES: 12. Analog loop back means looping back of the analog TX output to the RX input (the RX high-pass filters are bypassed). This way the codec can be tested without needing external analog sources. Refer to block diagram for signal path.

13. Digital loop back means looping back the digital RX output to the TX input. Refer to block diagram for signal path.

PRINCIPLES OF OPERATION

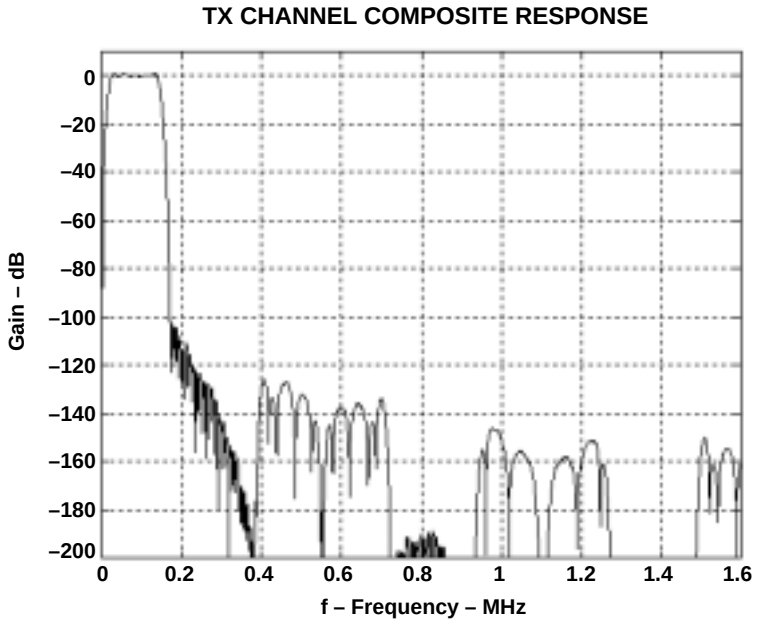


Figure 21. TX Channel Filter Response (DHPF Is Enabled)

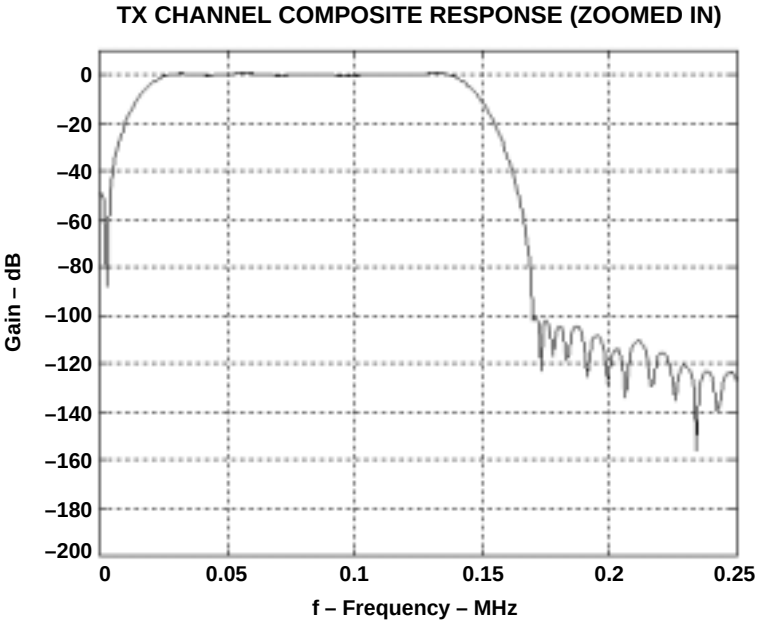


Figure 22. TX Channel Filter Response (Zoom In)

PRINCIPLES OF OPERATION

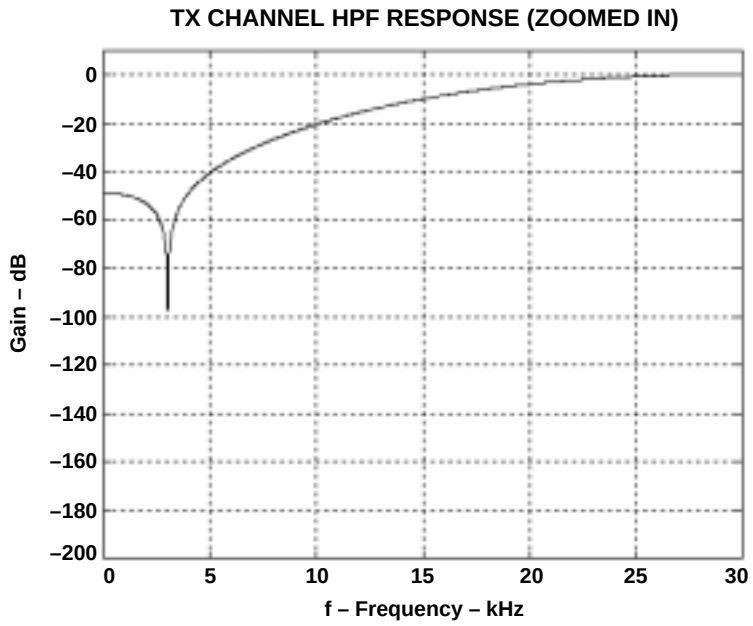


Figure 23. TX Channel HPF Response (Zoom In)

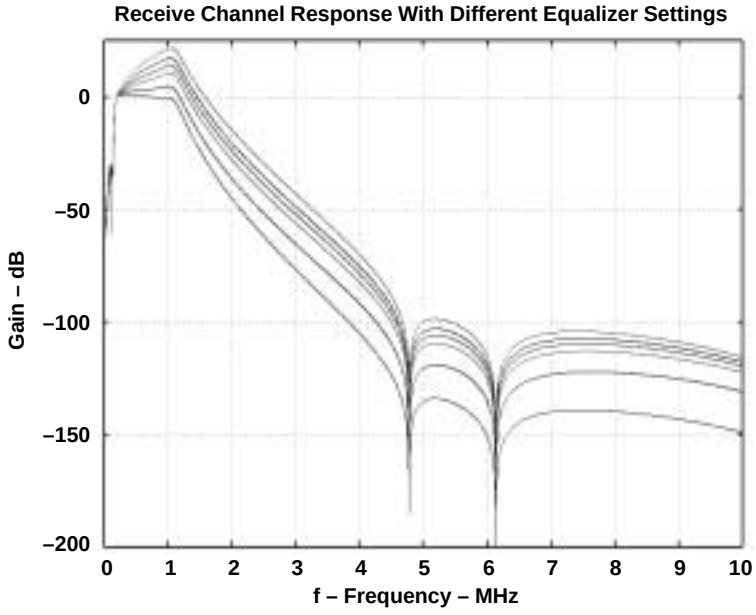


Figure 24. Receive Channel Frequency Responses With Different Equalizer Slope Settings (Full Rate)

PRINCIPLES OF OPERATION

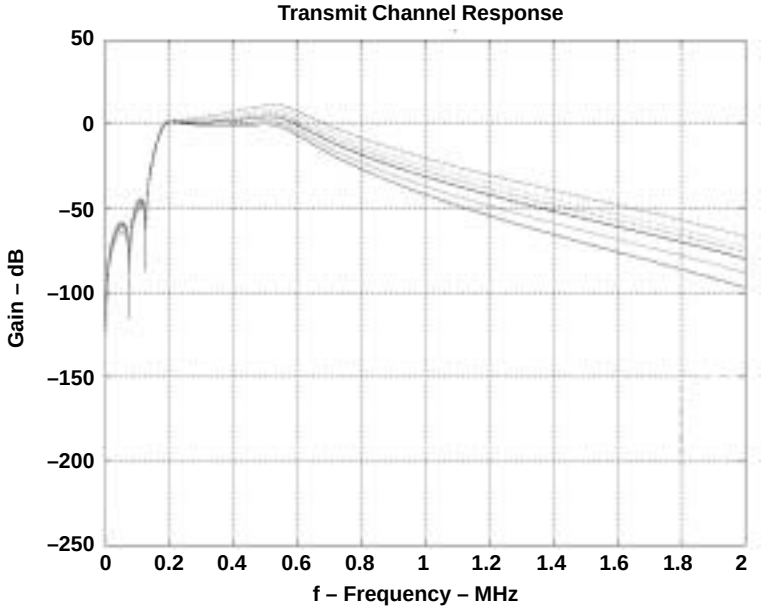


Figure 25. RX Channel Response With Different Equalizer Settings (G.lite Mode)

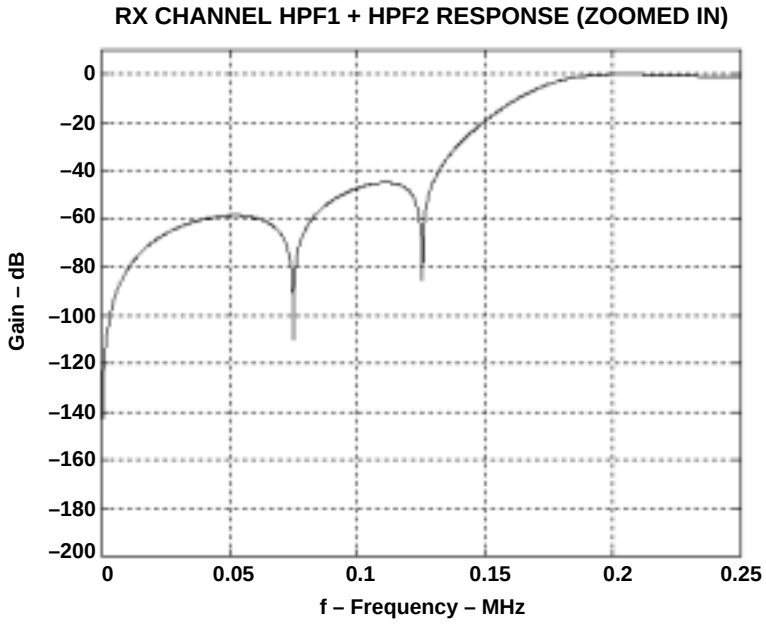
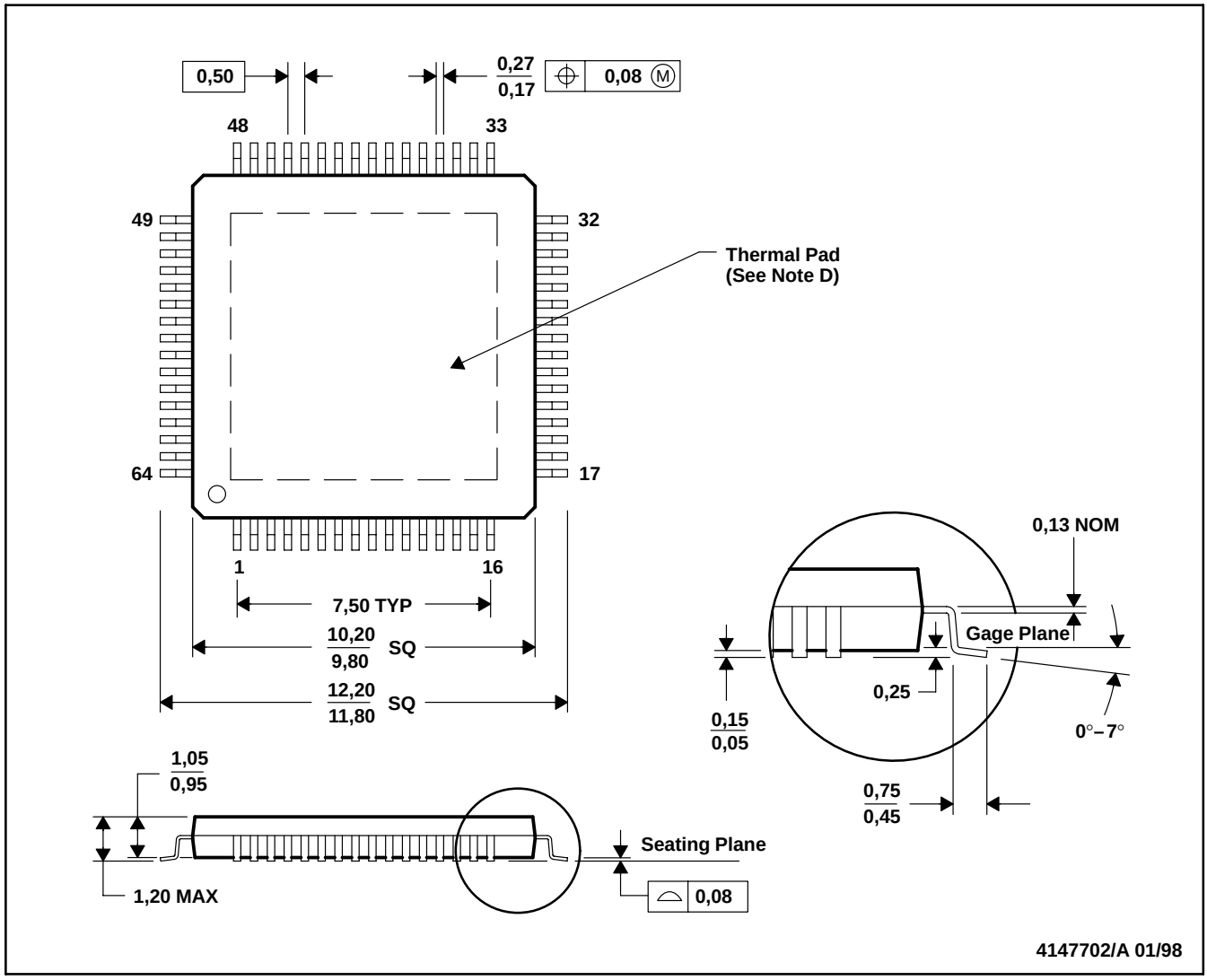


Figure 26. RX Channel HPF Response (Zoom In)

MECHANICAL DATA

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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