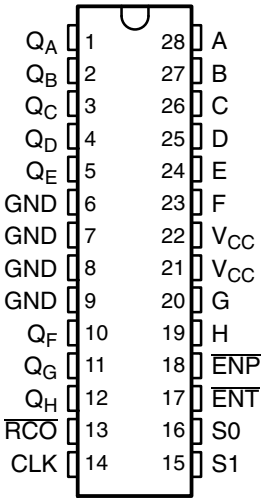
- **Inputs Are TTL-Voltage Compatible**
- **Asynchronous Clear**
- **Fully Independent Clock Circuit Simplifies Use**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11867 is a synchronous presettable binary counter featuring an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

The counters are fully programmable; that is, the outputs can each be preset to either logic level. The load-mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock rising edge.

The carry look-ahead circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. This is done with two count-enable inputs and a carry output. Both count-enable ($\overline{ENP}$ and $\overline{ENT}$) inputs must be low to count. The direction of the count is determined by the levels of the select (S0 and S1) inputs (see the function table). Input $\overline{ENT}$ is fed forward to enable the ripple-carry ($\overline{RCO}$) output. $\overline{RCO}$ then produces a low-level pulse while the count is zero (all outputs low) when counting down or 255 during counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ and $\overline{ENT}$ are allowed regardless of the level of the clock input.

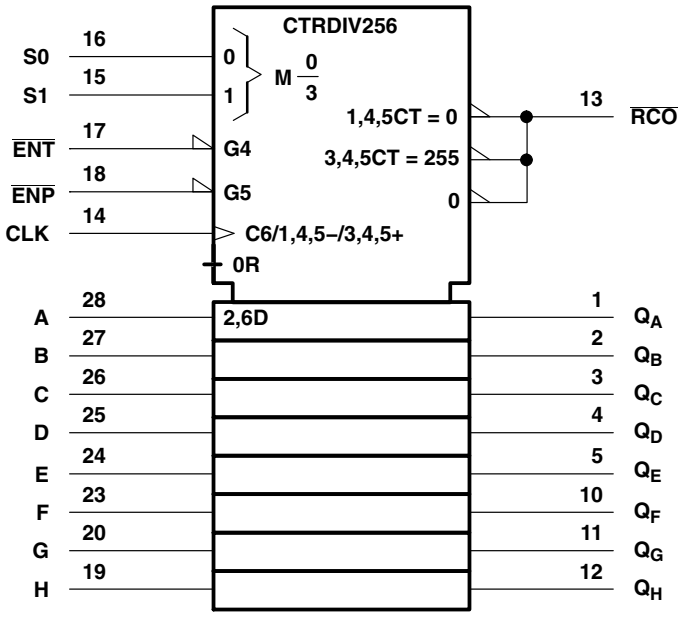
These counters feature a fully independent clock circuit. Whenever $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ either goes high or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The 74ACT11867 is characterized for operation from –40°C to 85°C.

MODE FUNCTION TABLE

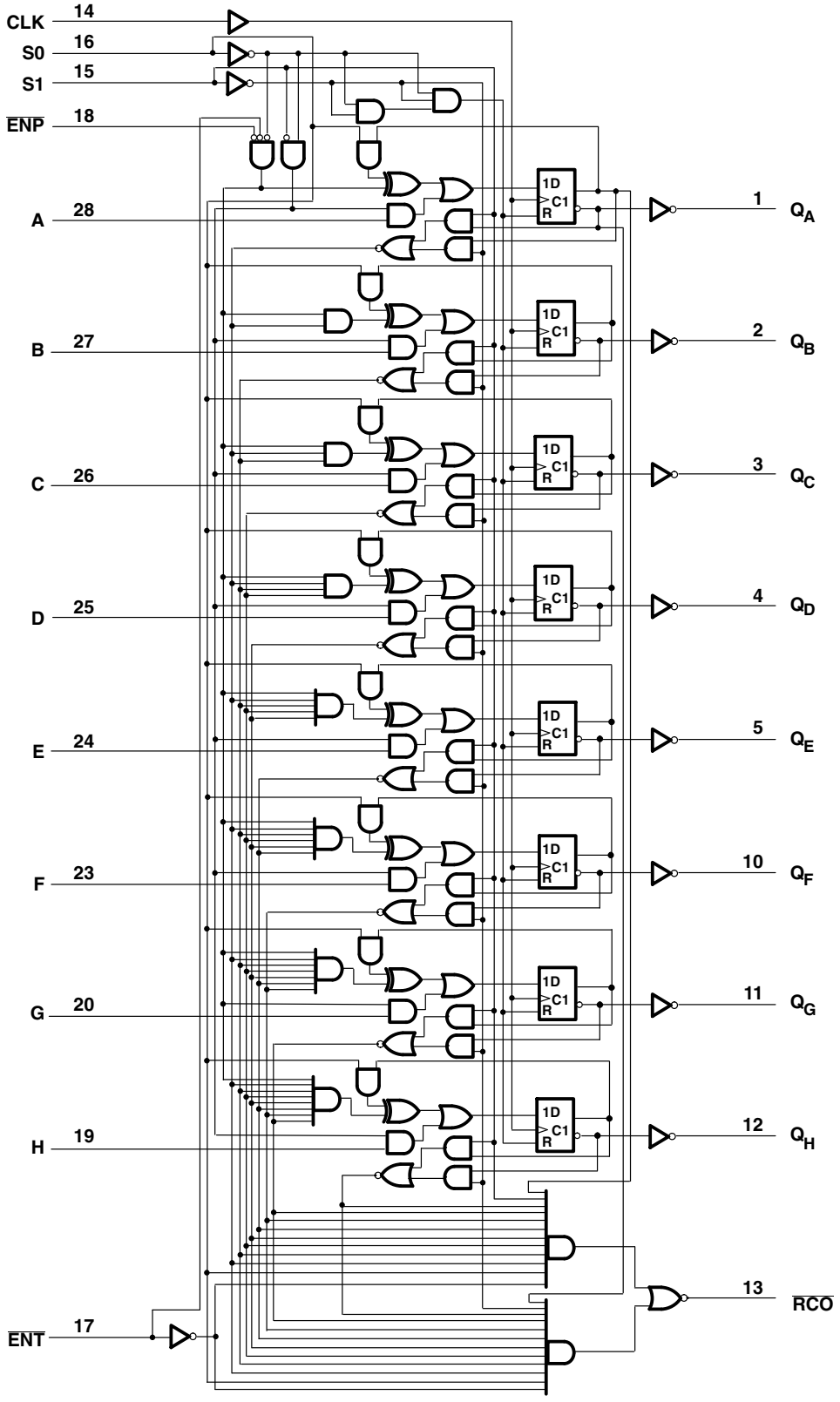
S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

logic symbol†

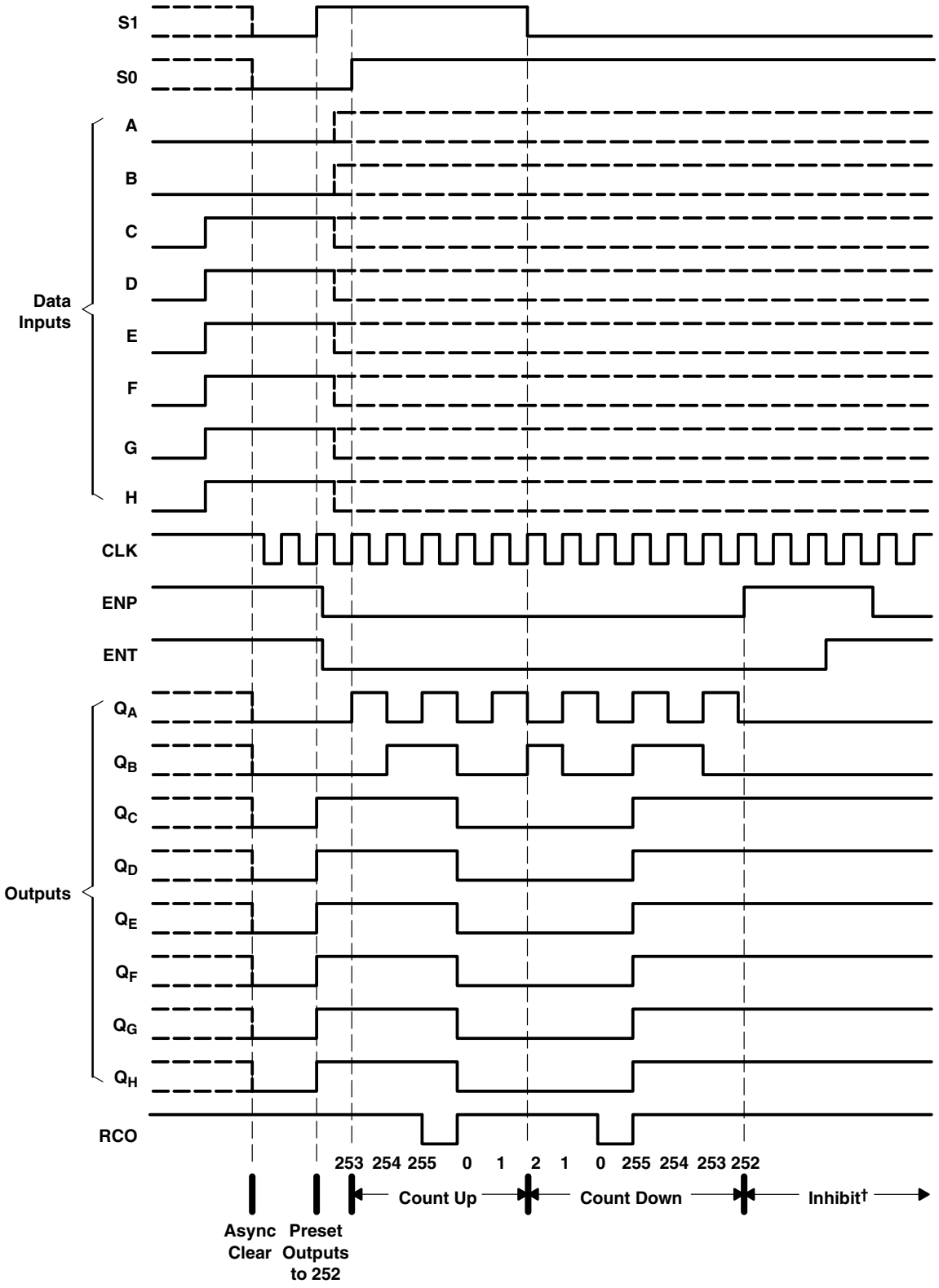


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



output sequence



† $\overline{\text{ENT}}$ and $\overline{\text{ENP}}$ must both be low for counting to occur.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±225 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = –24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	70	0	70	MHz
t_w	Pulse duration	S0 and S1 low	12		12		ns
		CLK	6.5		6.5		
t_{su}§	Setup time before CLK↑	Data	8		8		ns
		$\overline{ENP}$, $\overline{ENT}$	4		4		
		S0, S1 (load)	11		11		
		S0, S1 (count down)	11		11		
		S0, S1 (count up)	11		11		
t_h	Hold time after CLK↑	Data	1		1		ns
t_{skew}	Skew time between S0 and S1 to avoid inadvertent clear¶	S0 and S1 low		0		0	ns

§ This setup time is required to ensure stable data.
¶ This is the maximum time for which S0 and S1 can be low simultaneously when the device transitions between the load (S1 = H, S0 = L) and count-down (S1 = L, S0 = H) modes.

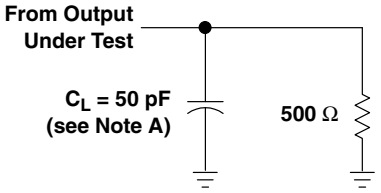
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CLK	$\overline{RCO}$	6	9.9	12.7	6	14.6	ns
t_{PHL}			6.4	10.9	14.2	6.4	16.3	
t_{PLH}	CLK	Q	5	8.9	11.9	5	13.6	ns
t_{PHL}			4.9	9	12.2	4.9	14	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3.9	6.8	9.1	3.9	10.5	ns
t_{PHL}			3.1	7	10.2	3.1	11.5	
t_{PHL}	Clear (S0, S1 low)	Q	6.3	11.9	16.6	6.3	19.1	ns
t_{PLH}	S0, S1 (count up/down)	$\overline{RCO}$	5.5	10.4	15.6	5.5	17.8	ns
t_{PHL}	S0, S1 (count up/down)	$\overline{RCO}$	5.6	10.1	14.8	5.6	17.2	ns
t_{PHL}	Clear (S0, S1 low)	$\overline{RCO}$	6.2	11.3	15.6	6.2	17.8	ns

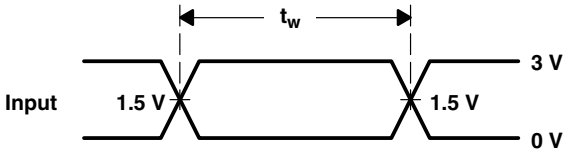
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	62	pF

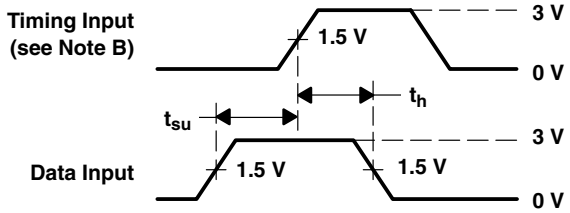
PARAMETER MEASUREMENT INFORMATION



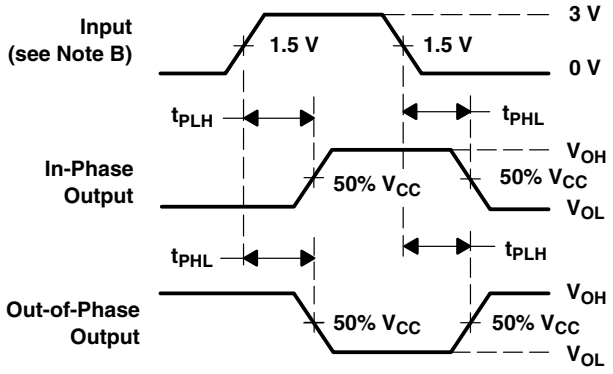
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ACT11867DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	-40 to 85		
74ACT11867DWR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	-40 to 85		
74ACT11867NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI	-40 to 85		

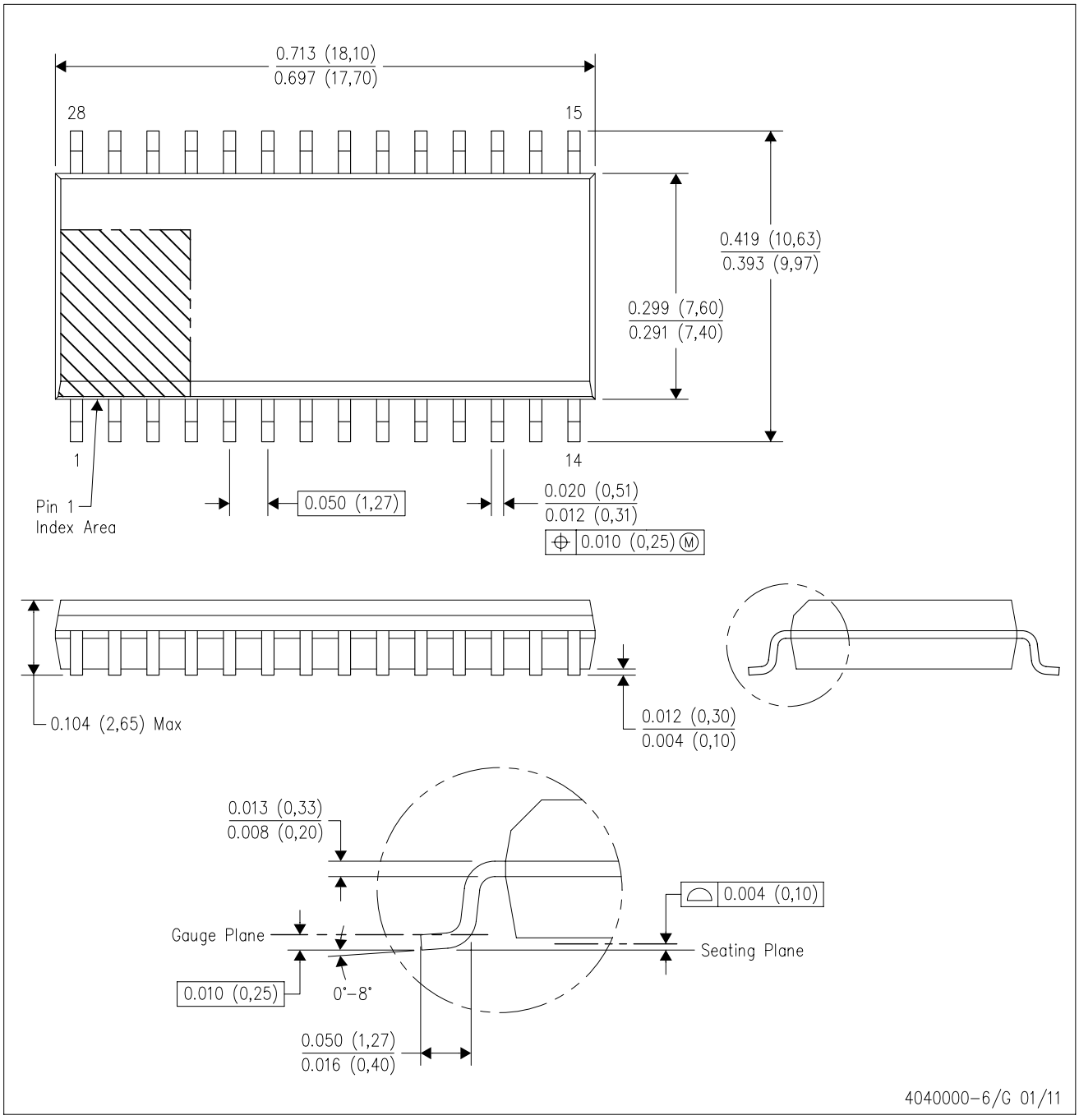
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265