SY58021U

4GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination Precision Edge®

General Description

The SY58021U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 LVPECL fanout buffer. Optimized to provide four identical output copies with less than 15ps output skew and only 70 fs_{RMS} phase jitter, the SY58021U can process clock signals as fast as 4GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture interfaces to differential LVPECL, CML, and LVDS signals (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the VT pin. The outputs are 100k LVPECL compatible, with extremely fast rise/fall times guaranteed to 70fs.

The SY58021U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require faster rise/fall times, or greater bandwidth, consider the SY58022U 1:4 fanout buffer with 400mV LVPECL output swing, or the SY58020U 1:4 CML fanout buffer. The SY58021U is part of Micrel's high-speed, Precision Edge® product line.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Precision Edge®

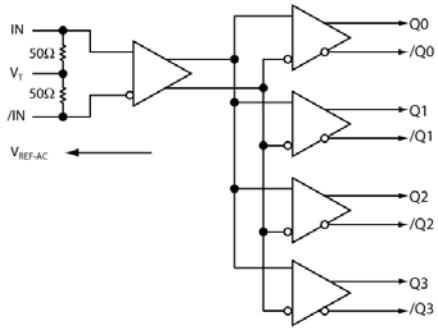
Features

- Precision 1:4 LVPECL fanout buffer
- Low jitter performance:
  - 70fs_{RMS} phase jitter (typical)
- Accepts an input signal as low as 100mV
- Unique input termination and VT pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML
- 100k LVPECL-compatible 800mV swing output
- Power supply 2.5V ±5% and 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 16-pin (3mm × 3mm) QFN package

Applications

- All SONET and GigE clock distribution
- Fibre Channel clock and data distribution
- Backplane distribution
- High-end, low-skew, multiprocessor, synchronous clock distribution

Block Diagram



Precision Edge is a registered trademark of Micrel, Inc.

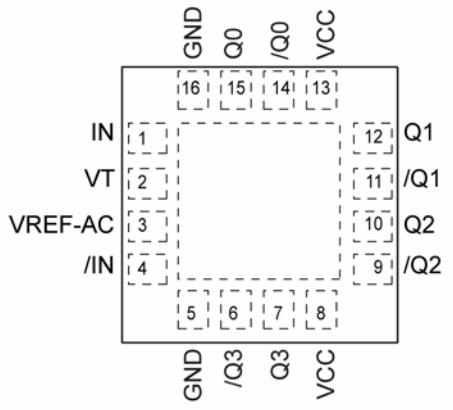
\Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58021UMI	QFN-16	Industrial	021U	Sn-Pb
SY58021UMITR[2]	QFN-16	Industrial	021U	Sn-Pb
SY58021UMG[3]	QFN-16	Industrial	021U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58021UMGTR[2, 3]	QFN-16	Industrial	021U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electrical only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

Pin Configuration



16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The V_T pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See “Input Interface Applications” section.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} –1.2V. It is used when AC-coupling to differential inputs. Connect V_{REF-AC} directly to the VT pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. See “Input Interface Applications” section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
5, 16	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15, 11, 12, 9, 10, 6, 7	/Q0, Q0, /Q1, Q1, /Q2, Q2, /Q3, Q3	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 800mV Proper termination is 50Ω to V_{CC}–2V at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See “LVPECL Output Termination” section.

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Source or Sink Current on VT Pin
  V_T Current ..... ±100mA
Source or Sink Current on IN, /IN
  Input Current ..... ±50mA
Source or Sink Current on V_{REF-AC}[4]
  V_{REF} Current ..... ±1.5mA
Soldering (20s) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) ..... +2.375V to +3.60V
Operating Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance
  QFN (θ_{JA})
    Still-Air ..... +60°C/W
    500 lpfm ..... +54°C/W
  QFN (ψ_{JB})
    Junction-to-Board Resistance[3] ..... +33°C/W

Input DC Electrical Characteristics[5]

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V	2.375	2.5	2.625	V
		V_{CC} = 3.3V	3.0	3.3	3.60	
I_{CC}	Power Supply Current	No load, V_{CC} = maximum		125	160	mA
V_{IH}	Input HIGH Voltage	IN, /IN (Note 6)	V_{CC} – 1.6		V_{CC}	V
V_{IL}	Input LOW Voltage	IN, /IN	0		V_{IH} – 0.1	V
V_{IN}	Input Voltage Swing	IN, /IN (see Figure 1a)	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing	IN, /IN (see Figure 1b)	0.2			V
R_{IN}	IN-to-V_T Resistance		40	50	60	Ω
V_{T_IN}	IN-to-V_T Voltage				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC} – 1.30	V_{CC} – 1.2	V_{CC} – 1.1	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (minimum) not lower than 1.2V.

LVPECL Output DC Electrical Characteristics[5]

V_{CC} = 3.3V ±10% or 2.5 ±5%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} – 1.145		V_{CC} – 0.895	V
V_{OL}	Output LOW Voltage		V_{CC} – 1.945		V_{CC} – 1.695	V
V_{OUT}	Output Voltage Differential Swing	(see Figure 1a)	550	780	1050	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	(see Figure 1b)	1100	1560	2100	mV

AC Electrical Characteristics

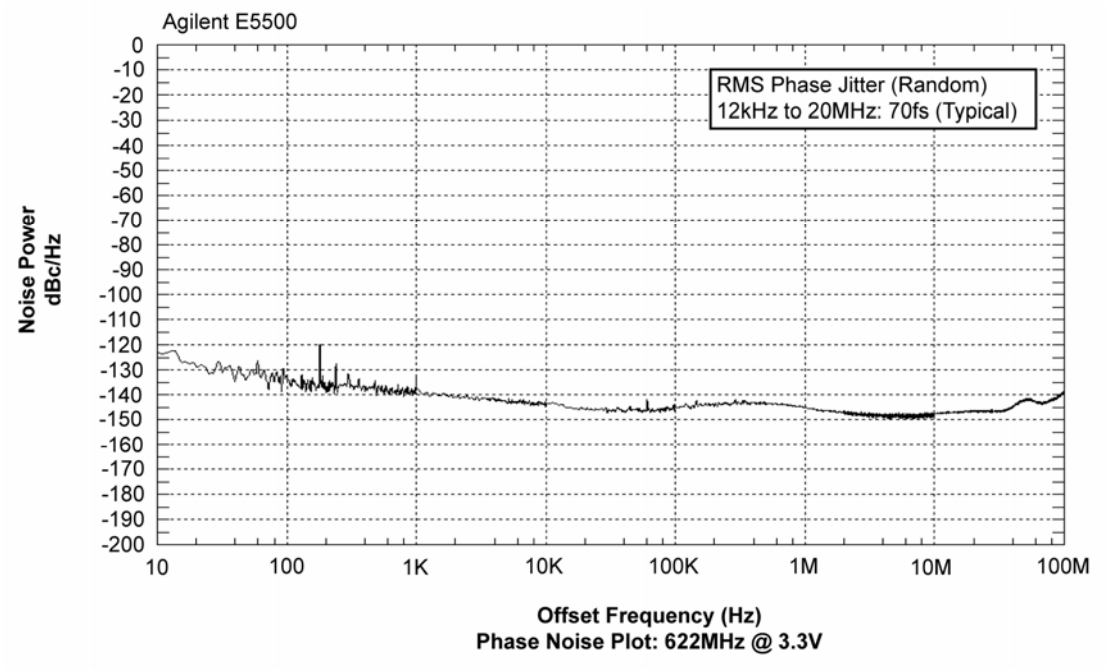
V_{CC} = 2.5V ±5% or 3.3 ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Operating Frequency	$V_{OUT} \geq$ 400mV Clock	4			GHz
		NRZ Data		5		Gbps
t_{PD}	Propagation Delay		150	220	300	ps
t_{CHAN}	Channel-to-Channel Skew	Note 7		4	15	ps
t_{SKEW}	Part-to-Part Skew	Note 8			50	ps
t_{JITTER}	RMS Phase Jitter	Output: 622MHz Integration Range: 12kHz – 20MHz		70		fs
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full swing	35	75	110	ps

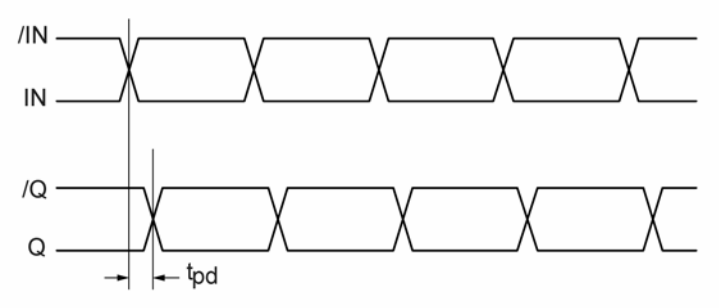
Notes:

7. Skew is measured between outputs of the same bank under identical transitions.
8. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

Phase Noise Graph



Timing Diagram



Single-Ended and Differential Swings

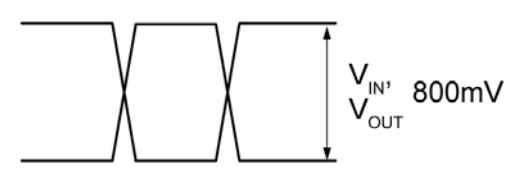


Figure 1a. Single-Ended Voltage Swing

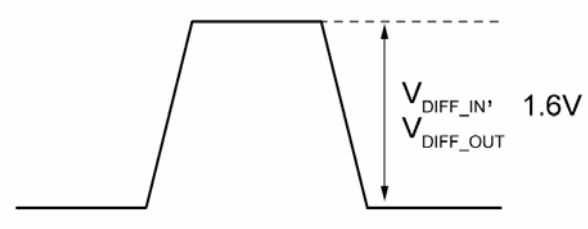
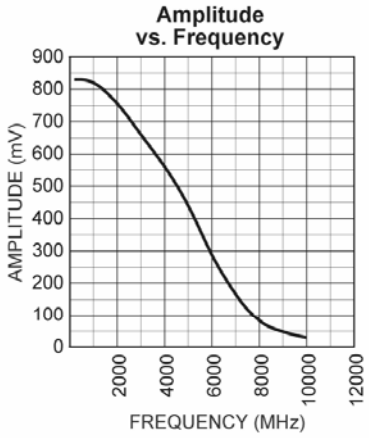
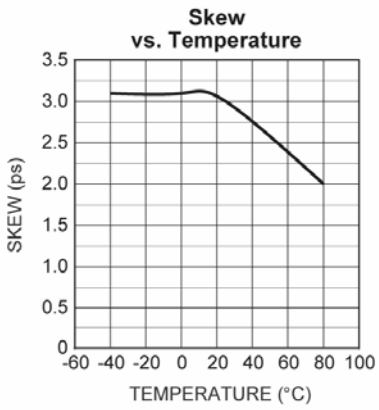


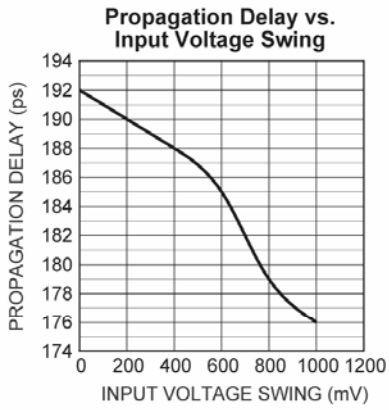
Figure 1b. Differential Voltage Swing

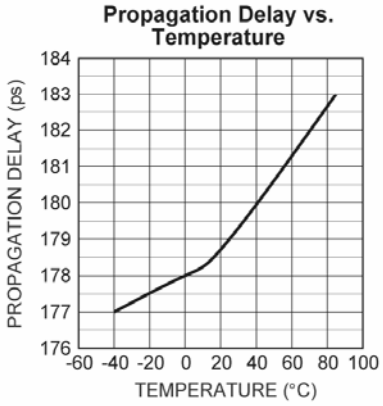
Typical Characteristics

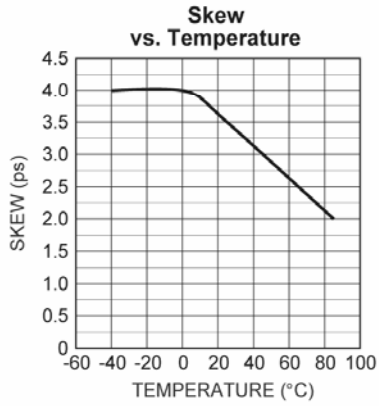
V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.





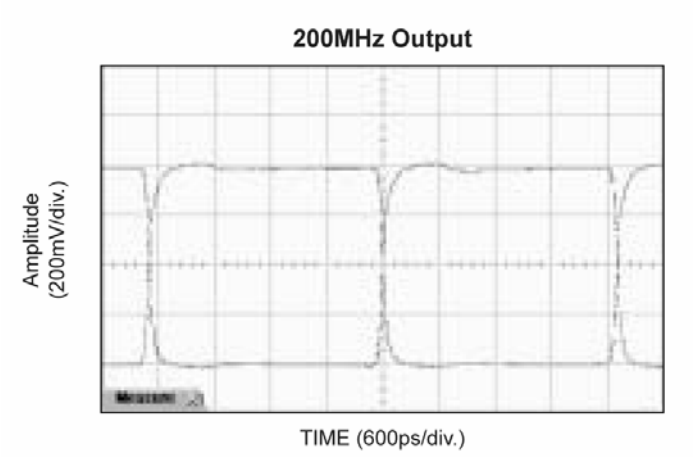


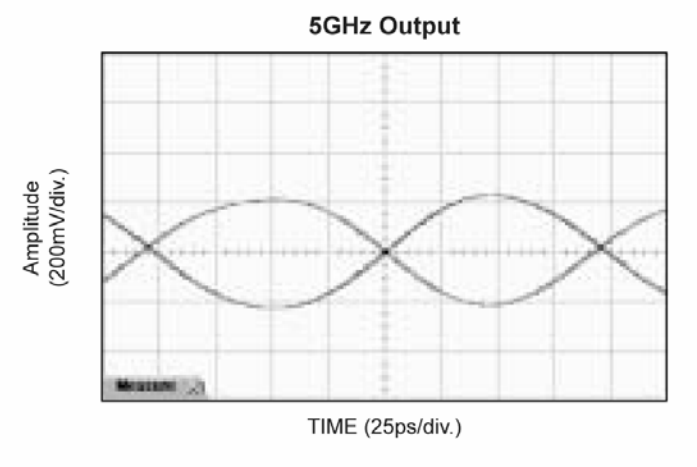


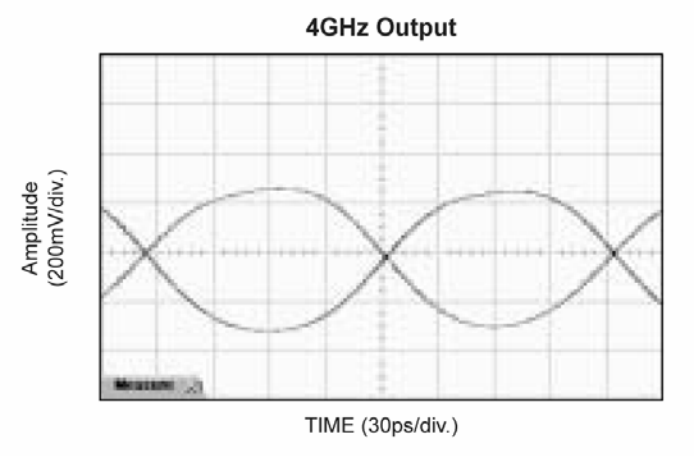


Functional Characteristics

V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.







Input Stage

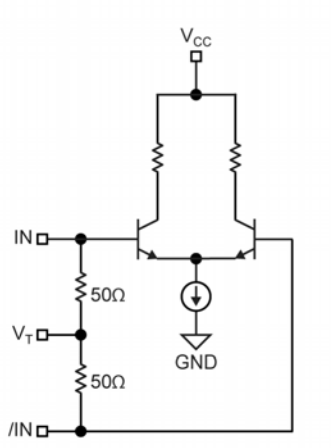


Figure 2. Simplified Differential Input Buffer

Input Interface Applications

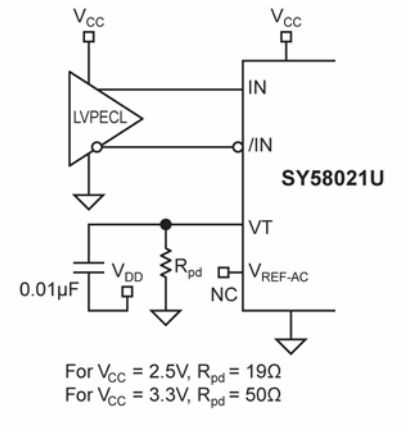


Figure 3a. LVPECL Input Interface

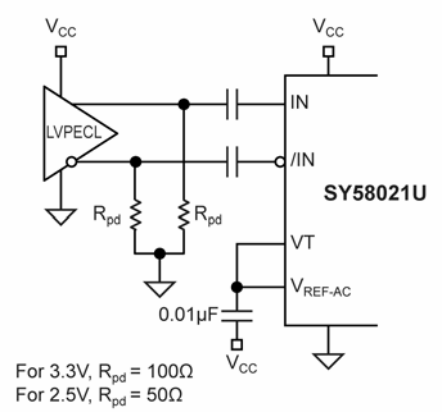


Figure 3b. AC-Coupled LVPECL Input Interface

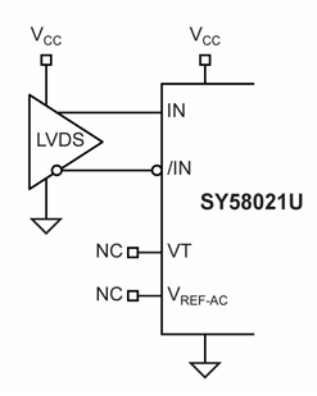


Figure 3c. LVDS Input Interface

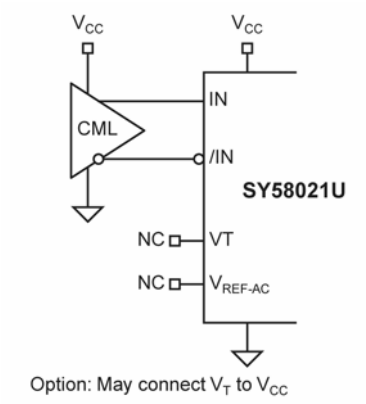


Figure 3d. DC-Coupled CML Input Interface

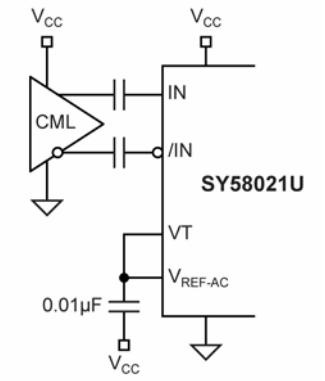
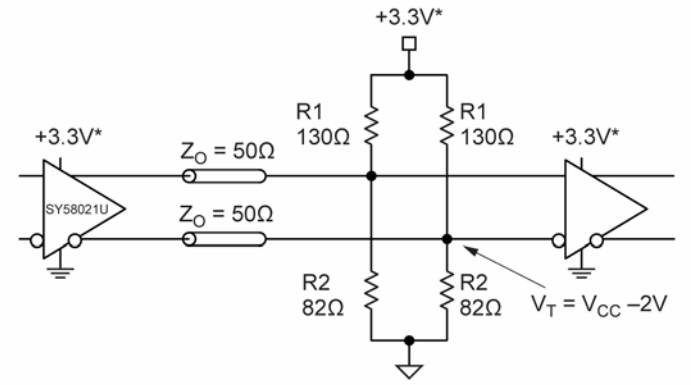


Figure 3e. AC-Coupled CML Input Interface

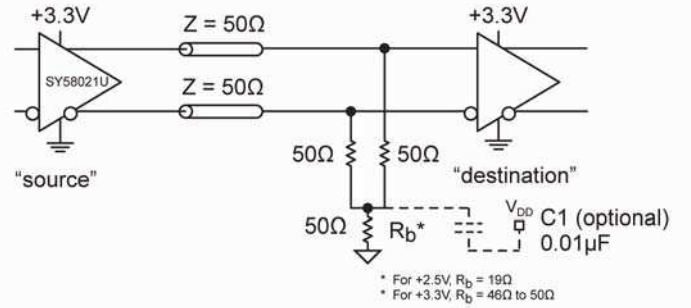
LVPECL Output

LVPECL outputs have very-low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques in terminating the LVPECL output (Figures 4 through 6).



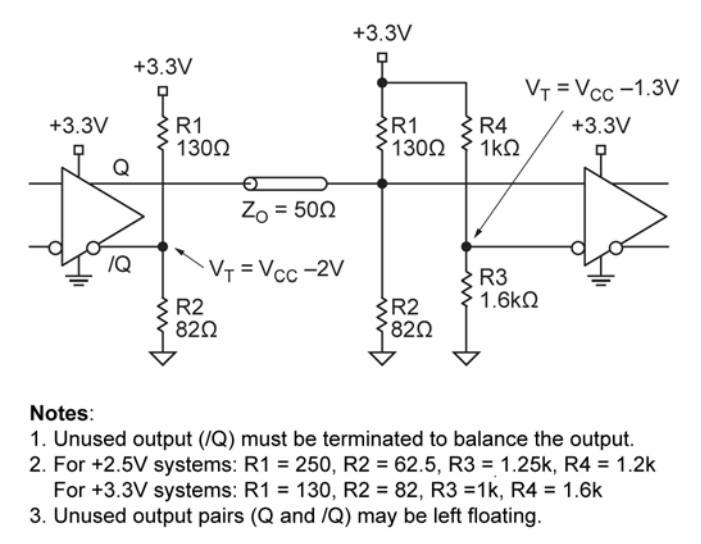
Note:
1. For +2.5V systems, R1 = 250Ω, R2 = 62.5Ω.

Figure 4. Parallel Termination-Thevenin Equivalent



Notes:
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. Rb resistor sets the DC bias voltage, equal to VT.

Figure 5. Parallel Termination (3-Resistor)



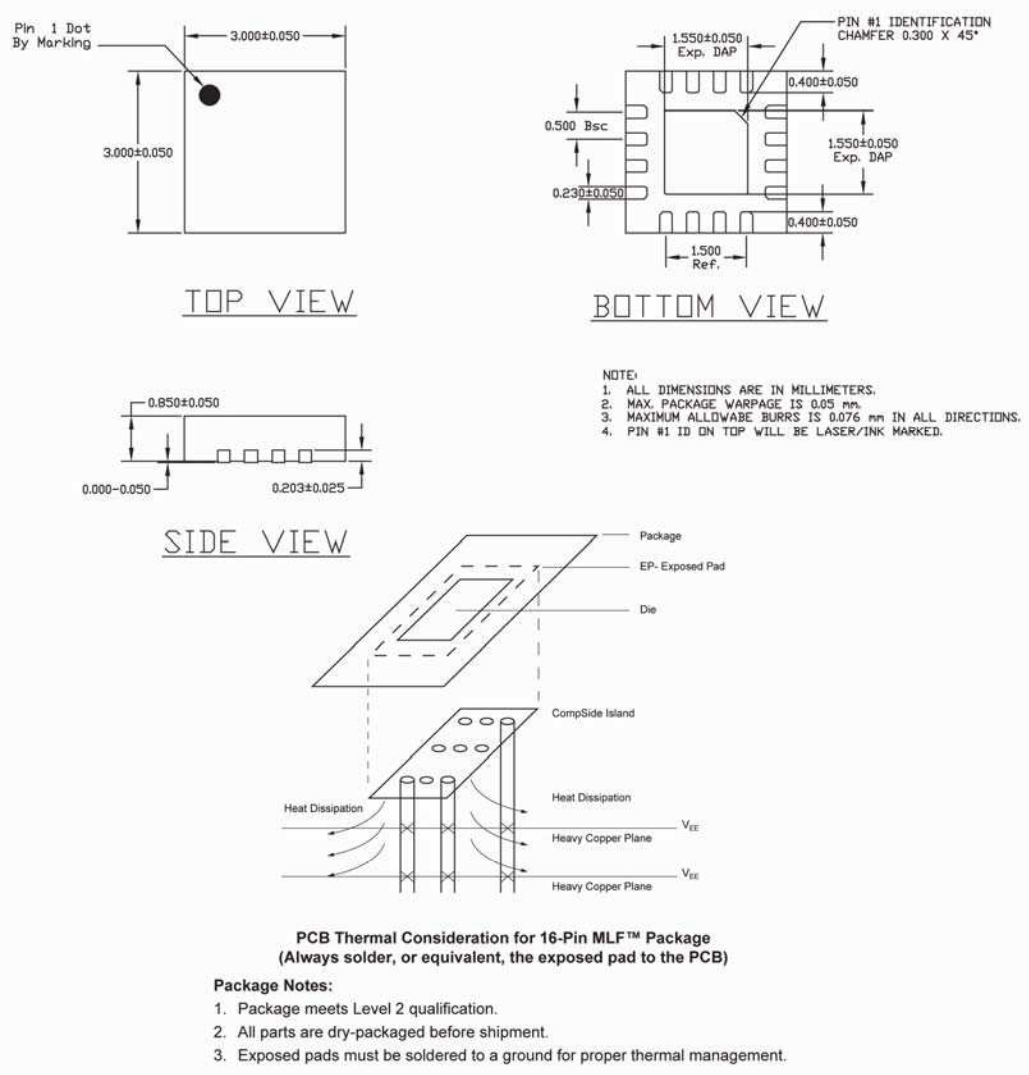
Notes:
1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250, R2 = 62.5, R3 = 1.25k, R4 = 1.2k
   For +3.3V systems: R1 = 130, R2 = 82, R3 =1k, R4 = 1.6k
3. Unused output pairs (Q and /Q) may be left floating.

Figure 6. Terminating Unused I/O

Related Micrel Products and Support Documentation

Part Number	Function	Data Sheet Link
SY58020U	6GHz, 1:4 CML Fanout Buffer/Translator with Internal I/O Terminations	www.micrel.com/product-info/products/sy58020u.shtml
SY58021U	4GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	www.micrel.com/product-info/products/sy58021u.shmtl
SY58022U	5.5GHz, 1:4 Fanout Buffer/Translator with 400mV LVPECL Outputs and Internal Terminations	www.micrel.com/product-info/products/sy58022u.shtml
M-0317	HBW Solutions	www.micrel.com/product-info/as/solutions.shtml

Package Information



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

16-Pin QFN

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