Datasheet

5.5V to 28V Input, 2ch Synchronous Buck DC/DC Controller

BD9528AMUV

General Description

BD9528AMUV is a dual buck regulator controller with adjustable output voltage from1.0V to 5.5V and an input voltage range of 5.5 to 28V. High efficiency is achieved with an external synchronous Nch-MOSFET. H^3Reg^{TM}, Rohm's advanced proprietary control method that uses constant on-time control to provide ultra high transient responses to load changes is used. SLLM(Simple Light Load Mode) technology is added to improve efficiency with light loads giving high efficiency over a wide load range. In addition to the dual buck regulator controllers, here are 2 LDO regulators included that are fixed output voltage of 3.3V and 5.0V. Other functions included are soft start, variable frequency, short circuit protection with timer latch, over voltage, and power good outputs. This buck regulator is optimal for high-current applications.

Features

- Adjustable Simple Light Load Mode (SLLM), Quiet light Load Mode (QLLM), Forced continuous Mode.
- Multifunctional Protection Circuit
  - -Settable Over Current Protection (OCP)
  - -Thermal Shut down (TSD)
  - -Under Voltage Lock Out (UVLO)
  - -Over Voltage Protection (OVP)
  - -Short Circuit Protection with Timer-Latch (SCP)
- 150kHz to 500kHz Switching frequency.
- Adjustable Soft Start.
- Power Good.
- Dual Linear Regulator (5V/3.3V (total 100mA)).
- Output Discharge.
- Reference voltage Circuit (0.7V).
- Boot diode

Applications

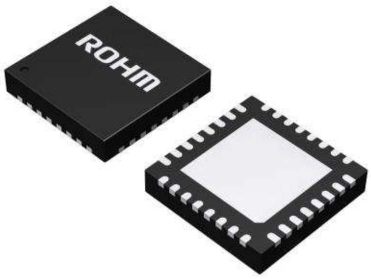
- Industrial Equipment ,FPGA, POL Power Supply, Mobile PC, Desktop PC, LCD-TV, Digital Components, etc.

Key Specifications

- Input Voltage Range: 5.5V to 28V
- Output Voltage Range: 1.0V to 5.5V
- Switching Frequency: 200k to 500kHz(Typ)
- Operating Temperature Range: -20°C to +100°C

Package

Package	W(Typ) x D(Typ) x H(Max)
VQFN032V5050	5.00mm x 5.00mm x 1.00mm



VQFN032V5050

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuit

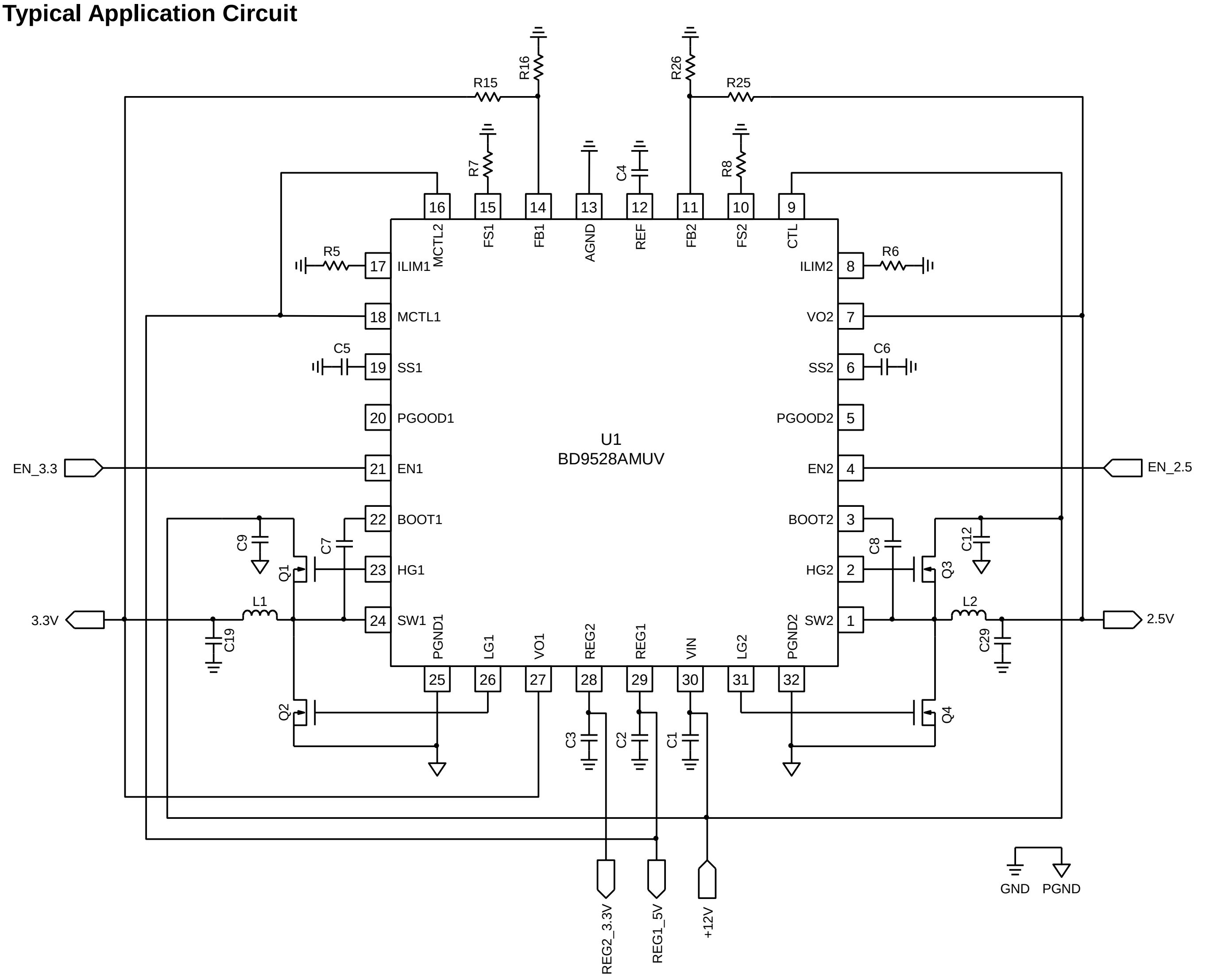


Figure 1. Application Circuit

Pin Configuration

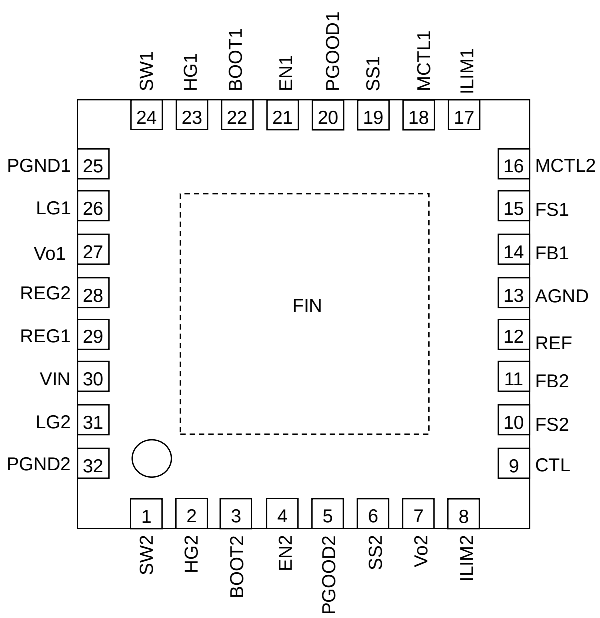


Figure 2. Pin Configuration

Pin Descriptions

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th></tr>
<tr><td>1
24</td><td>SW2
SW1</td><td>Ground pin for High-side FET. The maximum voltage range of this pin is 30V.</td></tr>
<tr><td>2
23</td><td>HG2
HG1</td><td>High-side FET gate drive pin.</td></tr>
<tr><td>3
22</td><td>BOOT2
BOOT1</td><td>This is the power supply pin for High-side FET driver. The maximum voltage range to ground is to 35V, to SW pin is to 7V. In switching operations, the voltage swings from (VIN+REG1) to REG1 by BOOT pin operation.</td></tr>
<tr><td>4
21</td><td>EN2
EN1</td><td>When EN pin voltage is at least 2.3V, the status of the switching regulator becomes active.
Conversely, the status switches off when EN pin voltage goes lower than 0.8V.
This pin is pulled down to AGND with 1MΩ resistor.</td></tr>
<tr><td>5
20</td><td>PGOOD2
PGOOD1</td><td>If FB pin voltage is 15% or less of reference voltage, it will output low level.
The output format is open drain, so please connect pull-up resistance.</td></tr>
<tr><td>6
19</td><td>SS2
SS1</td><td>This is the setting pin for soft start. The rising time is determined by the capacitor connected between SS and ground, and the fixed current inside IC after it is the status of low in standby mode. It controls the output voltage till SS voltage catch up the REF pin to become the SS terminal voltage.</td></tr>
<tr><td>7
27</td><td>VO2
VO1</td><td>This is the output discharge pin, and output voltage feedback pin for frequency setting.</td></tr>
<tr><td>8
17</td><td>ILIM2
ILIM1</td><td>This is the coil current limit setting pin. Set the resistor which is connected in between ground.</td></tr>
<tr><td>9</td><td>CTL</td><td>When CTL pin voltage is at least 2.3V, the status of the linear regulator REG1 and REG2 output becomes active. Conversely, the status switches off when CTL pin voltage goes lower than 0.8V. The switching regulator doesn’t become active when the status of CTL pin is low, if the status of EN pin is high.
This pin is pulled up to VIN with 1MΩ resistor.</td></tr>
<tr><td>10
15</td><td>FS2
FS1</td><td>Frequency input. A resistor to ground will set the switching frequency.
Frequencies from 150kHz to 500kHz are possible.</td></tr>
<tr><td>11
14</td><td>FB2
FB1</td><td>This is the output voltage feedback pin.
The IC controls reference voltage and FB terminal voltage are almost same.</td></tr>
<tr><td>12</td><td>REF</td><td>This is the output voltage setting pin.
The IC controls reference voltage and FB terminal voltage are almost same.</td></tr>
<tr><td>13</td><td>AGND</td><td>Ground input for control circuit.</td></tr>
<tr><td>16
18</td><td>MCTL2
MCTL1</td><td>This is the operation mode setting pin. If terminal voltage reaches less than 0.8V, it will be Low Level.
If terminal voltage reaches more than 2.3V, it will be High Level. This pin is pulled down to AGND with 300kΩ resistor.
<table><tr><td colspan="2">Input</td><td rowspan="2">Control Mode</td></tr><tr><td>MCTL1</td><td>MCTL2</td></tr><tr><td>Low</td><td>Low</td><td>SLLM</td></tr><tr><td>Low</td><td>High</td><td>QLLM</td></tr><tr><td>High</td><td>Low</td><td>Continuous PWM Mode</td></tr><tr><td>High</td><td>High</td><td>Continuous PWM Mode</td></tr></table></td></tr>
<tr><td>25
32</td><td>PGND1
PGND2</td><td>This is the ground pin for Low-side FET drive.</td></tr>
<tr><td>26
31</td><td>LG1
LG2</td><td>This is the Low-side FET gate drive pin. It is operated in switching between REG1 to PGND.
ON resistance of output stage when High, it is 2Ω and when Low, it is 0.5Ω drive Low-side FET gate with the high pace.</td></tr>
<tr><td>28</td><td>REG2</td><td>This is the output pin for 3.3V/50mA linear regulator (5V/3.3V (total 100mA)).
Please connect 10μF capacitor which characteristic is more than X5R near the pin.</td></tr>
<tr><td>29</td><td>REG1</td><td>This is the output pin for 5V/50mA linear regulator (5V/3.3V (total 100mA)).
Please connect 10μF capacitor which characteristic is more than X5R near the pin.</td></tr>
<tr><td>30</td><td>VIN</td><td>Supply pin of H^3Reg^{TM} control circuit and linear regulator. Monitor input voltage and determine necessary on-time. As a result, this terminal voltage changes, and then the IC operation become unstable. Please connect 10μF capacitor which characteristic is more than X5R near the pin.</td></tr>
<tr><td>FIN</td><td>FIN</td><td>This is the thermal PAD. Please connect to the ground.</td></tr>
</table>

Output condition table

Input			Output			
CTL	EN1	EN2	REG1(5V)	REG2(3.3V)	DC/DC1	DC/DC2
Low	Low	Low	OFF	OFF	OFF	OFF
Low	Low	High	OFF	OFF	OFF	OFF
Low	High	Low	OFF	OFF	OFF	OFF
Low	High	High	OFF	OFF	OFF	OFF
High	Low	Low	ON	ON	OFF	OFF
High	Low	High	ON	ON	OFF	ON
High	High	Low	ON	ON	ON	OFF
High	High	High	ON	ON	ON	ON

∗CTL pin is connected to VIN pin with 1MΩ resistor(pull up) internal IC.
∗EN pin is connected to AGND pin with 1MΩ resistor(pull down) internal IC.

Block Diagram

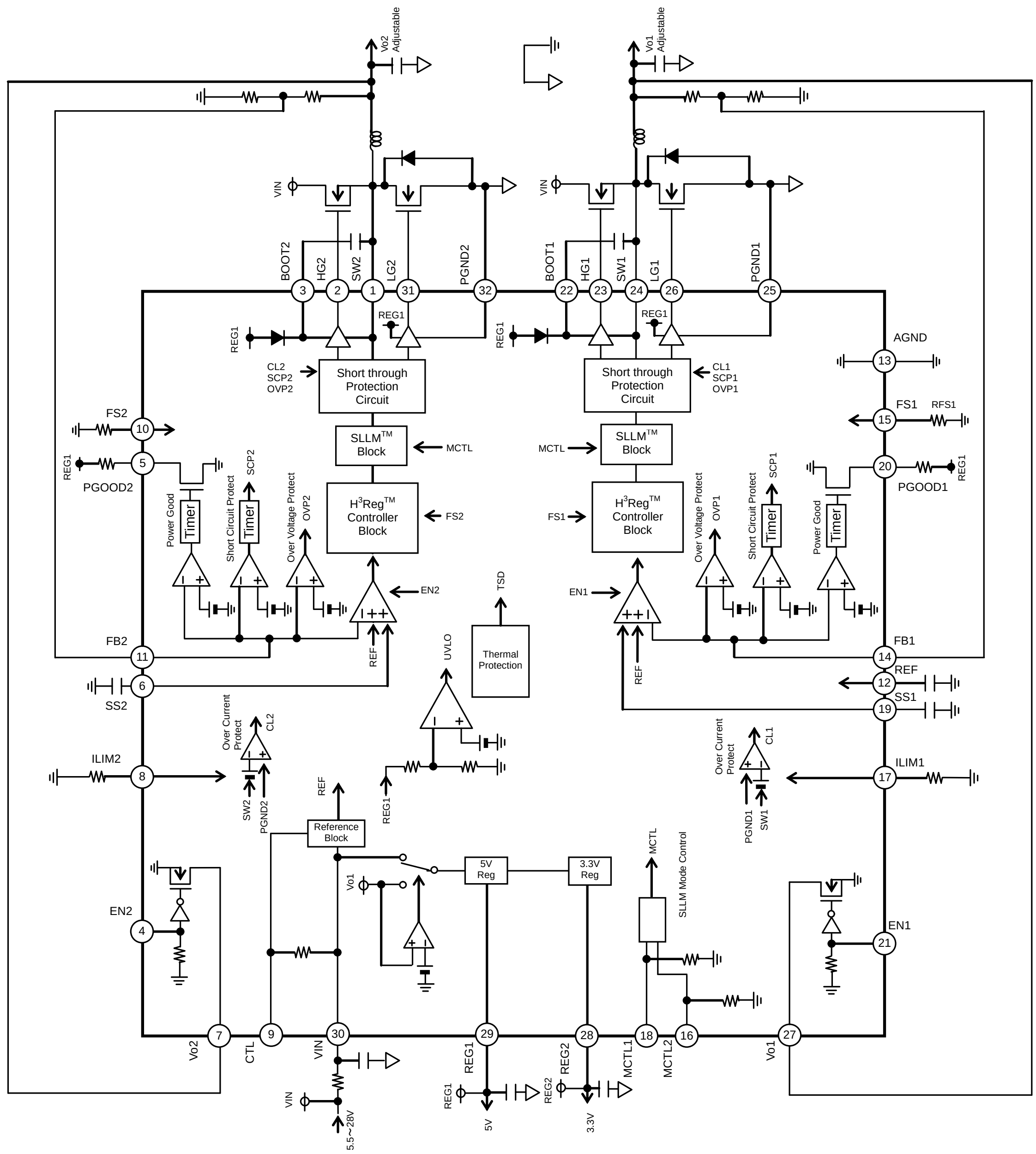


Figure 3. Block Diagram

Absolute Maximum Ratings(Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Terminal Voltage	VIN, CTL, SW1, SW2	30	V	Note 1
	EN1, EN2, PGOOD1, PGOOD2 Vo1, Vo2, MCTL1, MCTL2	6	V	Note 1, Note 2
	FS1, FS2, FB1, FB2, ILIM1, ILIM2, SS1, SS2, LG1, LG2, REF,REG2	REG1+0.3	V	Note 1
	BOOT1, BOOT2	35	V	Note 1, Note 2
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	7	V	Note 1, Note 2
	HG1	BOOT1+0.3	V	Note 1, Note 2
	HG2	BOOT2+0.3	V	Note 1, Note 2
	PGND1, PGND2	AGND±0.3	V	Note 1, Note 2
Power Dissipation1	Pd1	0.38	W	Note 3
Power Dissipation2	Pd2	0.88	W	Note 4
Power Dissipation3	Pd3	3.26	W	Note 5
Power Dissipation4	Pd4	4.56	W	Note 6
Operating Temperature Range	Topr	-20 to +100	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature	Tjmax	+150	°C	

(Note 1) Not to exceed Pd.
(Note 2) Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
(Note 3) Derating in done 3.0 mW/°C for operating above Ta ≥ 25°C (when don't mounted on a heat radiation board).
(Note 4) Derating in done 7.0 mW/°C for operating above Ta ≥ 25°C (Mount on 1-layer 74.2mm x 74.2mm x 1.6mm board).
Surface heat dissipation copper foil:20.2mm^2.
(Note 5) Derating in done 26.1 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 74.2mm x 74.2mm x 1.6mm board
Two sides heat dissipation copperfoil:20.2mm^2. 2 or 3-layer : heat dissipation copper foil : 5505mm^2).
(Note 6) Derating in done 36.5 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 74.2mm x 74.2mm x 1.6mm board)
All layers heat dissipation copper foil:5505mm^2.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Terminal Voltage	VIN	5.5	-	28	V	
	CTL	-0.3	-	28	V	
	EN1, EN2, MCTL1, MCTL2	-0.3	-	5.5	V	
	BOOT1, BOOT2	4.5	-	33	V	
	SW1, SW2	-0.3	-	28	V	
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	-0.3	-	5.5	V	
	Vo1, Vo2, PGOOD1, PGOOD2	-0.3	-	5.5	V	
Minimum ON Time	TONMIN	-	-	150	nsec	
Soft Start time	Tss_max	-	-	100	ms	

This product should not be used in a radioactive environment.

Electrical Characteristics (Unless otherwise noted, Ta=25°CVIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VIN Standby Current	I_{STB}	70	150	250	μA	EN1= EN2= 0V, CTL= 5V
VIN Bias Current	I_{IN}	60	130	230	μA	Vo1= 5V
VIN Shut Down Mode Current	I_{SHD}	6	12	18	μA	CTL= 0V
CTL Low Voltage	V_{CTLL}	-0.3	-	0.8	V	
CTL High Voltage	V_{CTLH}	2.3	-	28	V	
CTL Bias Current	I_{CTL}	-18	-12	-6	μA	CTL= 0V
EN Low Voltage	V_{ENL}	-0.3	-	0.8	V	
EN High Voltage	V_{ENH}	2.3	-	5.5	V	
EN Bias Current	I_{EN}	-	3	6	μA	EN= 3V
5V Linear Regulator -VIN						
REG1 Output Voltage	V_{REG1}	4.90	5.00	5.10	V	IREG1=1mA
Maximum Current	I_{REG1}	100	-	-	mA	IREG2= 0mA, (Note 7)
Line Regulation	$R_{EG.I1}$	-	90	180	mV	VIN= 5.5 to 28V
Load Regulation	$R_{EG.L1}$	-	30	50	mV	IREG1= 0 to 30mA
3.3V Linear Regulator						
REG2 Output Voltage	V_{REG2}	3.27	3.30	3.33	V	IREG2= 1mA
Maximum Current	I_{REG2}	100	-	-	mA	IREG1= 0mA, (Note 7)
Line Regulation	$R_{EG.I2}$	-	-	20	mV	VIN= 5.5 to 28V
Load Regulation	$R_{EG.L2}$	-	-	30	mV	IREG2= 0 to 30mA
5V Linear Regulator -Vo1						
Input Threshold Voltage	R_{EG1th}	4.1	4.4	4.7	V	Vo1: Sweep up
Input Delay Time	T_{REG1}	1.5	3.0	6.0	ms	
Switch Resistance	R_{REG1}	-	1.0	3.0	Ω	
Under Voltage Lock Out Block						
REG1 Threshold Voltage	R_{EG1_UVLO}	3.9	4.2	4.5	V	REG1: Sweep up
Hysteresis Voltage	$dV_{\_UVLO}$	50	100	200	mV	REG1: Sweep down
Output Voltage Sense Block						
Feedback Voltage1	V_{FB1}	0.693	0.700	0.707	V	
FB1 Bias Current	I_{FB1}	-	0	1	μA	FB1= REF
Output Discharge Resistance1	$R_{DISOUT1}$	50	100	200	Ω	
Feedback Voltage2	V_{FB2}	0.693	0.700	0.707	V	
FB2 Bias Current	I_{FB2}	-	0	1	μA	FB2= REF
Output Discharge Resistance2	$R_{DISOUT2}$	50	100	200	Ω	
H^3REG^{TM} Control Block						
On Time1	$t_{ON}1$	0.760	0.910	1.060	μs	Vo1= 5V,FS1= 51kΩ
On Time2	$t_{ON}2$	0.470	0.620	0.770	μs	Vo2= 3.3V ,FS2= 51kΩ
Maximum On Time 1	$t_{ONMAX}1$	2.5	5	10	μs	Vo1= 5V
Maximum On Time 2	$t_{ONMAX}2$	1.65	3.3	6.6	μs	Vo2= 3.3V
Minimum Off Time	t_{OFFMIN}	-	0.2	0.4	μs	
FET Driver Block						
HG High Side ON Resistance	HG_{HON}	-	3.0	6.0	Ω	
HG Low Side ON Resistance	HG_{LON}	-	2.0	4.0	Ω	
LG High Side ON Resistance	LG_{HON}	-	2.0	4.0	Ω	
LG Low Side ON Resistance	LG_{LON}	-	0.5	1.0	Ω	

(Note 7) $I_{REG1}+I_{REG2} \leq$ 100mA.

Electrical Characteristics (Unless otherwise noted, Ta=25°CVIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

Over Voltage Protection Block						
OVP Threshold Voltage	V_{OVP}	0.77 (+10%)	0.84 (+20%)	0.91 (+30%)	V	
OVP Hysteresis	dV_{OVP}	50	150	300	mV	
Output Short Protection Block						
SCP Threshold Voltage	V_{SCP}	0.42 (-40%)	0.49 (-30%)	0.56 (-20%)	V	
Delay Time	T_{SCP}	0.4	0.75	1.5	ms	
Over Current Protection Block						
Offset Voltage	dV_{SMAX}	80	100	120	mV	ILIM= 100kΩ
Power Good Block						
Power Good Low Threshold	V_{PGTHL}	0.525 (-25%)	0.595 (-15%)	0.665 (-5%)	V	
Power Good Low Voltage	V_{PGL}	-	0.1	0.2	V	IPGOOD= 1mA
Delay Time	T_{PGOOD}	0.4	0.75	1.5	ms	
Power Good Leakage Current	I_{LEAKPG}	-2	0	2	μA	VPGOOD= 5V
Soft Start Block						
Charge Current	I_{SS}	1.5	2.3	3.1	μA	
Standby Voltage	V_{SS_STB}	-	-	50	mV	
Mode Control Block						
MCTL Low Voltage	V_{MCTL_L}	-0.3	-	0.3	V	
MCTL High Voltage	V_{MCTL_H}	2.3	-	REG1 +0.3	V	
MCTL Bias Current	I_{MCTL}	8	16	24	μA	MCTL= 5V

Typical Performance Curves (Reference data)

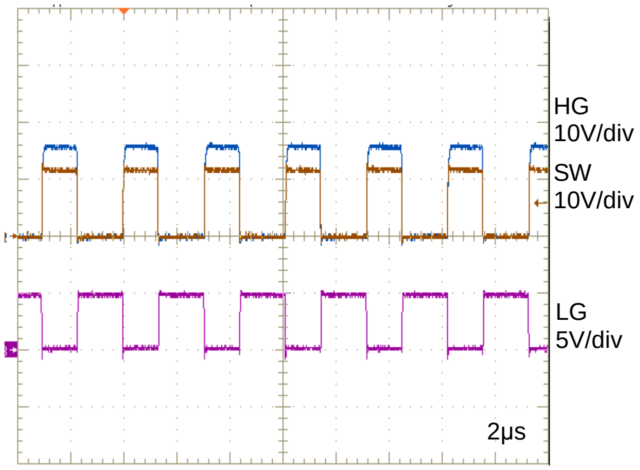


Figure 1. Switching Waveform
(Vo= 5V, Io= 0A, PWM)

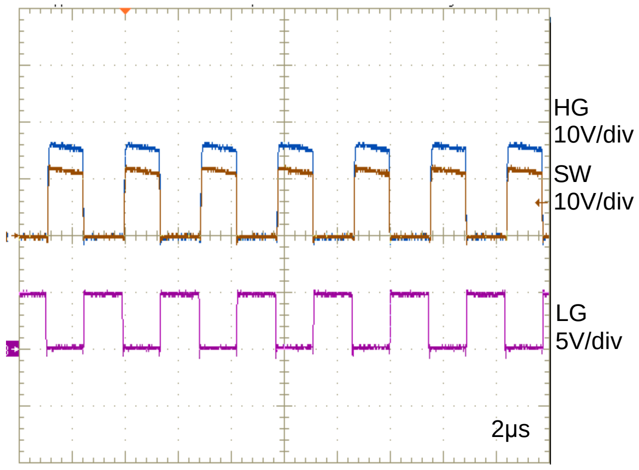


Figure 2. Switching Waveform
(Vo= 5V, Io= 8A, PWM)

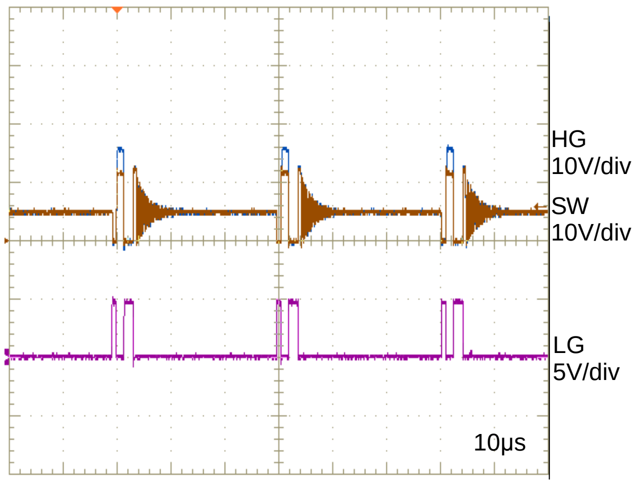


Figure 3. Switching Waveform
(Vo= 5V, Io= 0A, QLLM)

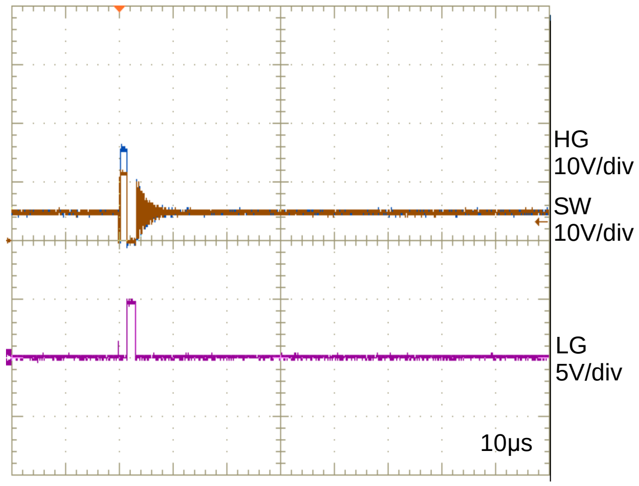


Figure 4. Switching Waveform
(Vo= 5V, Io= 0A, SLLM)

Typical Performance Curves - continued

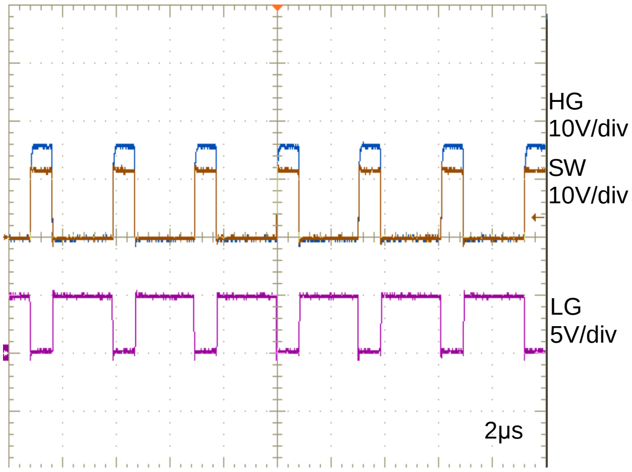


Figure 5. Switching Waveform
(Vo= 3.3V, Io= 0A, PWM)

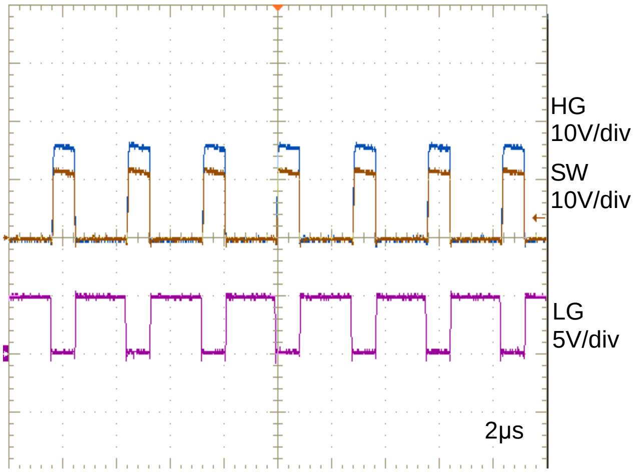


Figure 6. Switching Waveform
(Vo= 3.3V, Io= 8A, PWM)

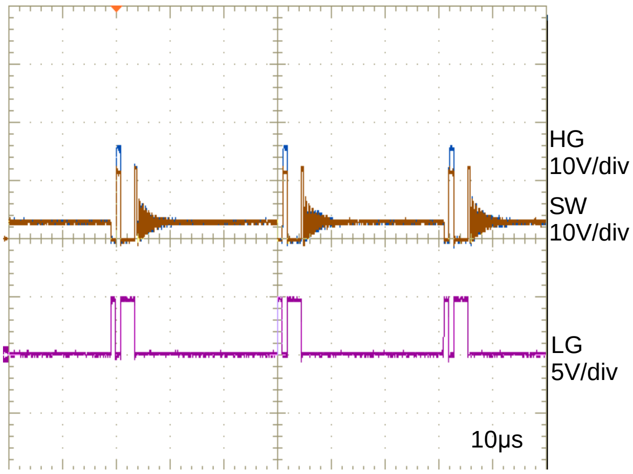


Figure 7. Switching Waveform
(Vo= 3.3V, Io= 0A, QLLM)

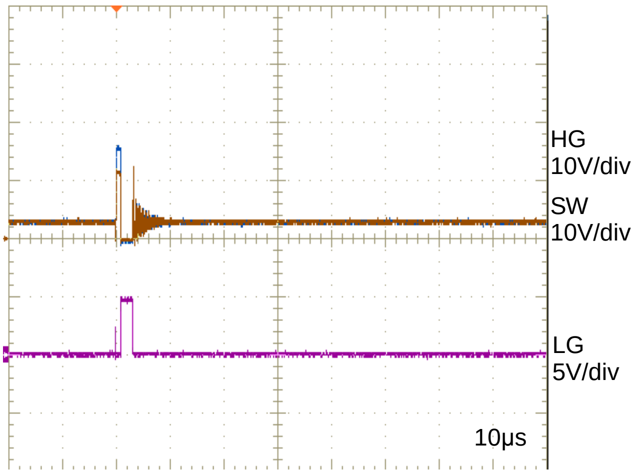


Figure 8. Switching Waveform
(Vo= 3.3V, Io= 0A, SLLM)

Typical Performance Curves - continued

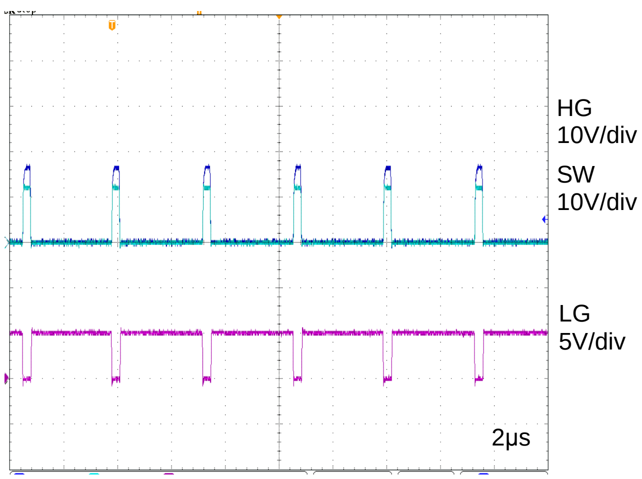


Figure 9. Switching Waveform
(Vo= 1V, Io= 0A, PWM)

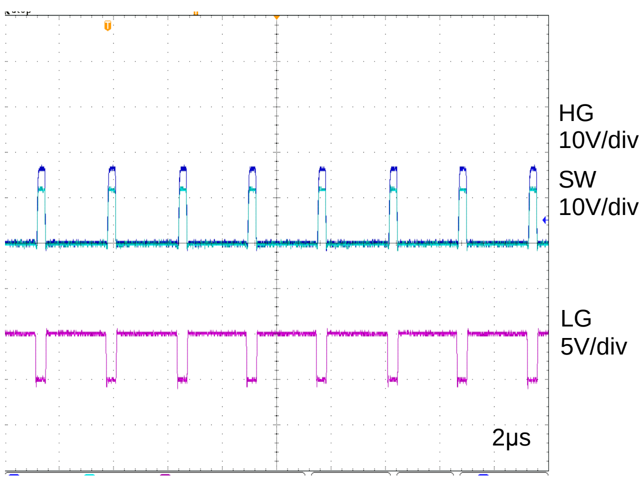


Figure 10. Switching Waveform
(Vo= 1V, Io= 8A, PWM)

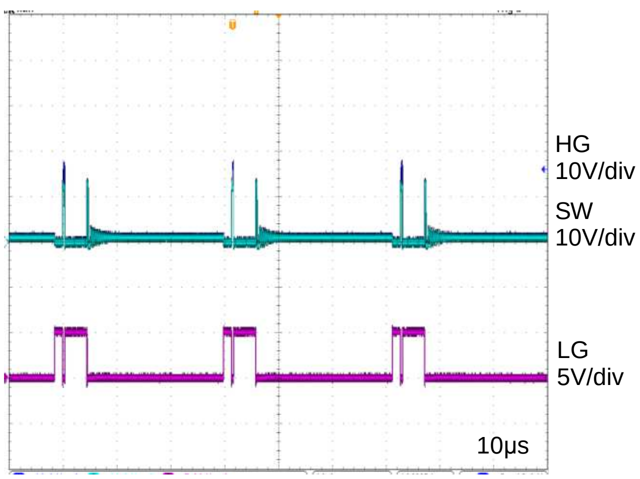


Figure 11. Switching Waveform
(Vo= 1V, Io= 0A, QLLM)

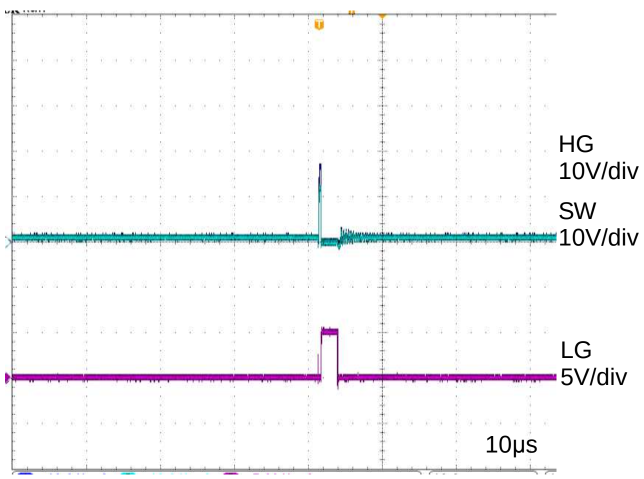


Figure 12. Switching Waveform
(Vo= 1V, Io= 0A, SLLM)

Typical Performance Curves - continued

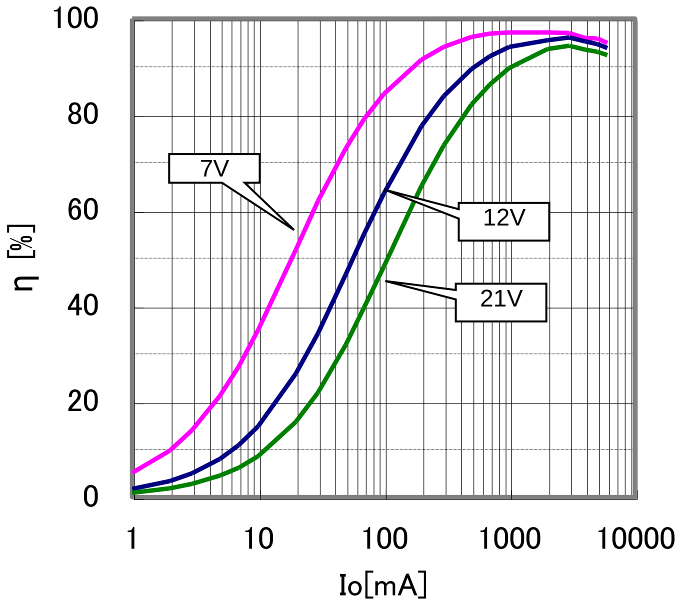


Figure 13. Efficiency
(Vo= 5V, PWM)

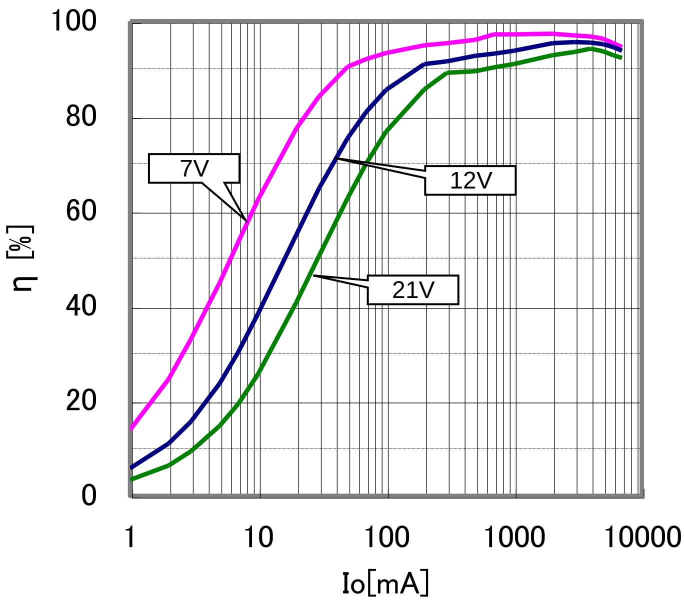


Figure 14. Efficiency
(Vo= 5V, QLLM)

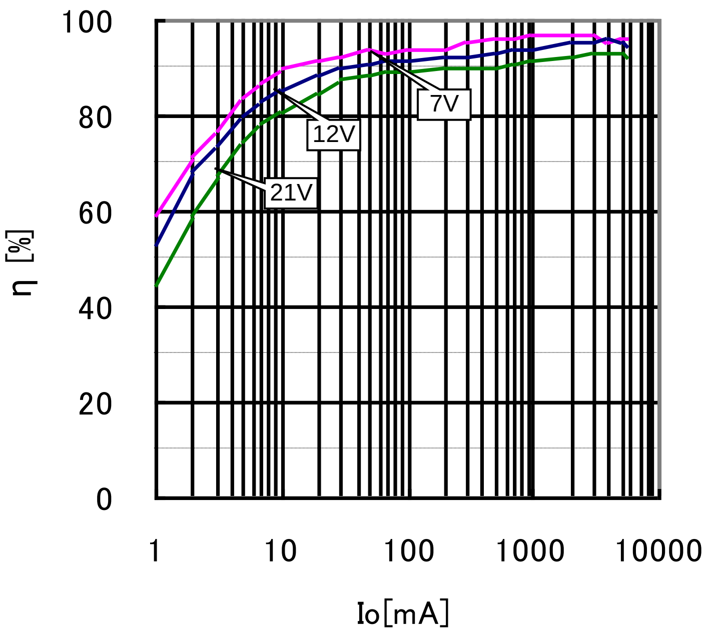


Figure 15. Efficiency
(Vo= 5V, SLLM)

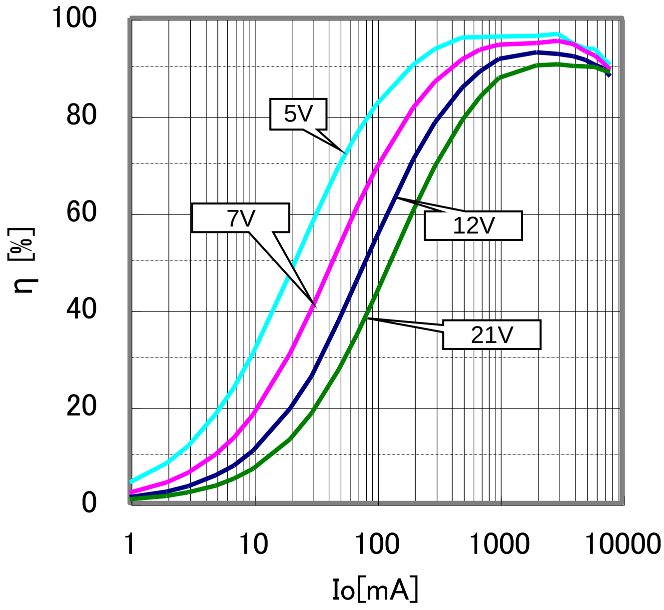


Figure 16. Efficiency
(Vo= 3.3V, PWM)

Typical Performance Curves - continued

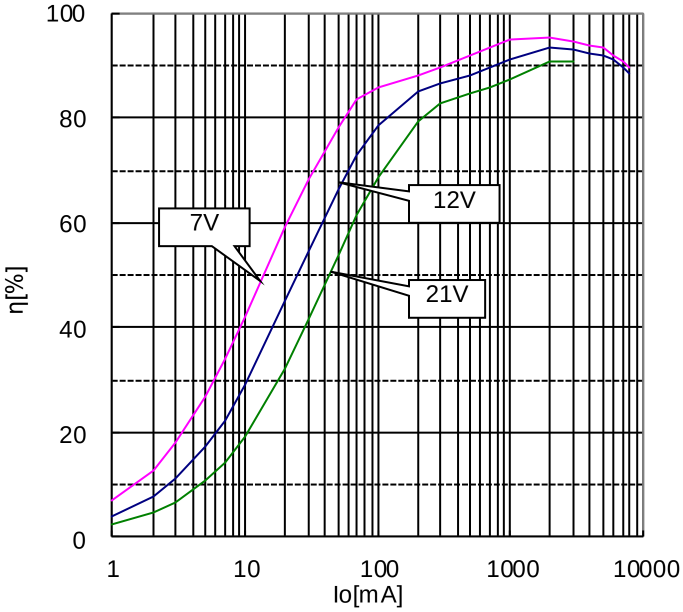


Figure 17. Efficiency
(Vo= 3.3V, QLLM)

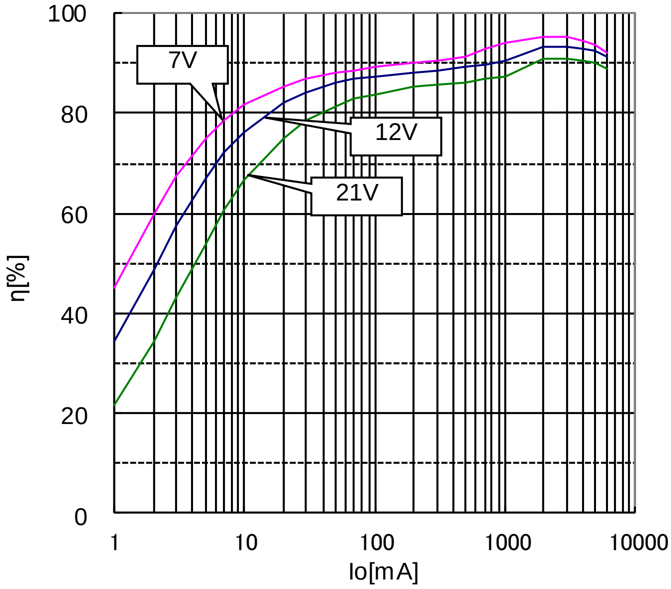


Figure 18. Efficiency
(Vo= 3.3V, SLLM)

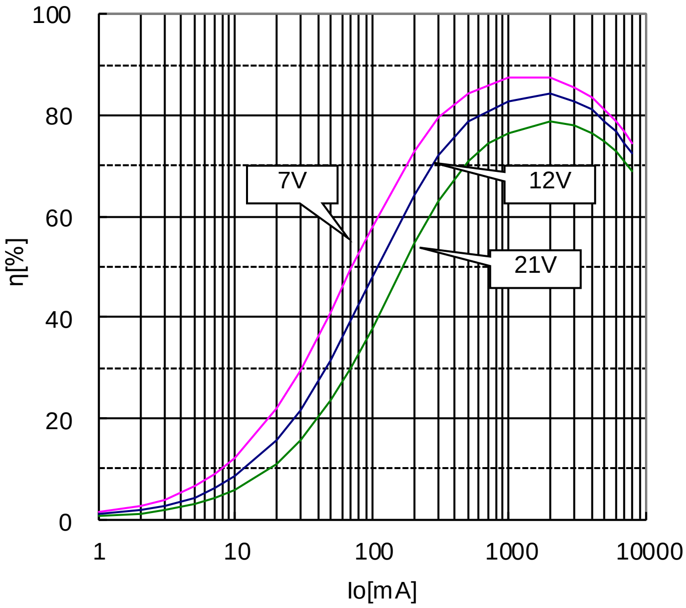


Figure 19. Efficiency
(Vo= 1V, PWM)

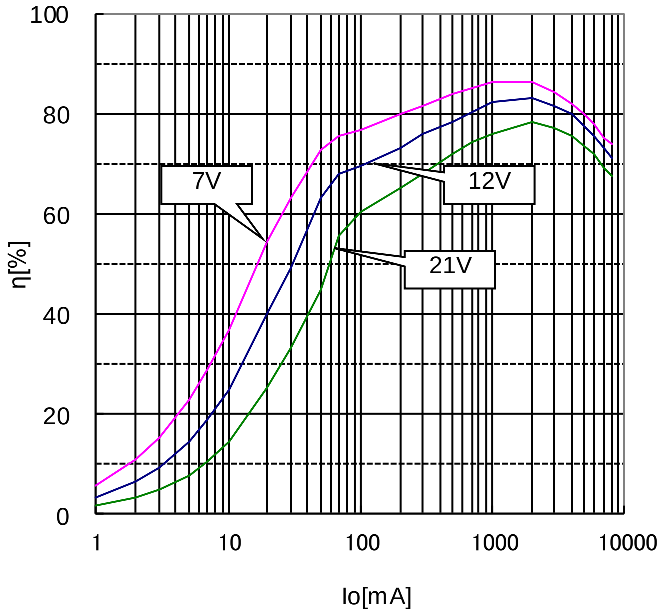


Figure 20. Efficiency
(Vo= 1V, QLLM)

Typical Performance Curves - continued

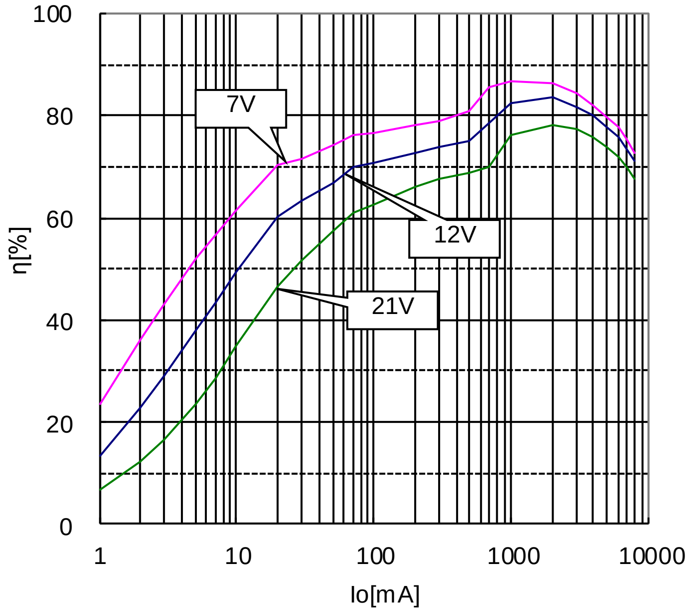


Figure 21. Efficiency
(Vo= 1V, SLLM)

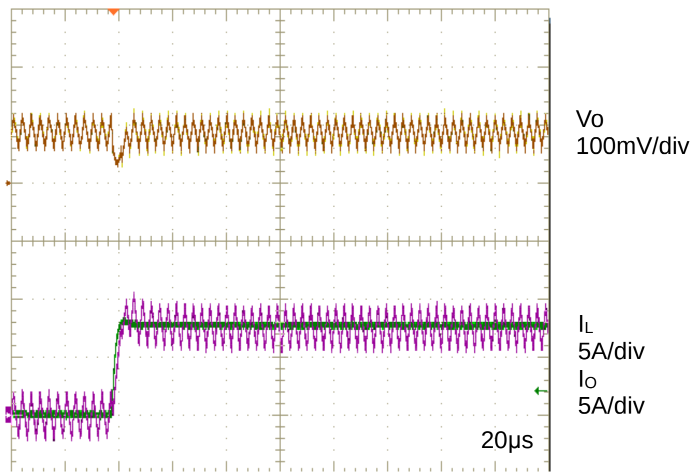


Figure 22. Transient Response
(Vo= 5V, PWM, Io= 0A→8A)

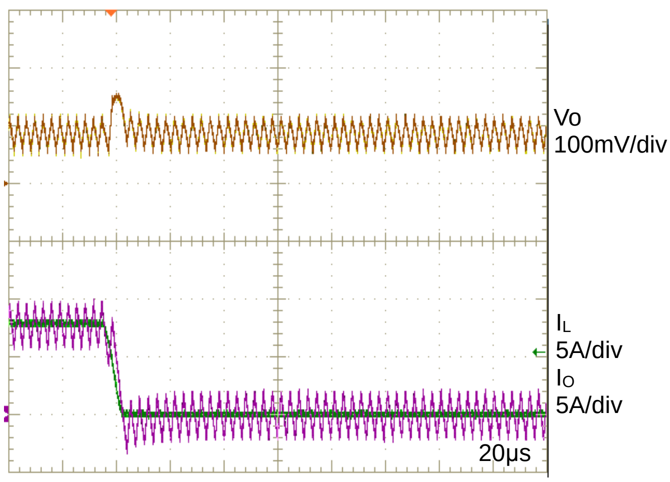


Figure 23. Transient Response
(Vo= 5V, PWM, Io= 8A→0A)

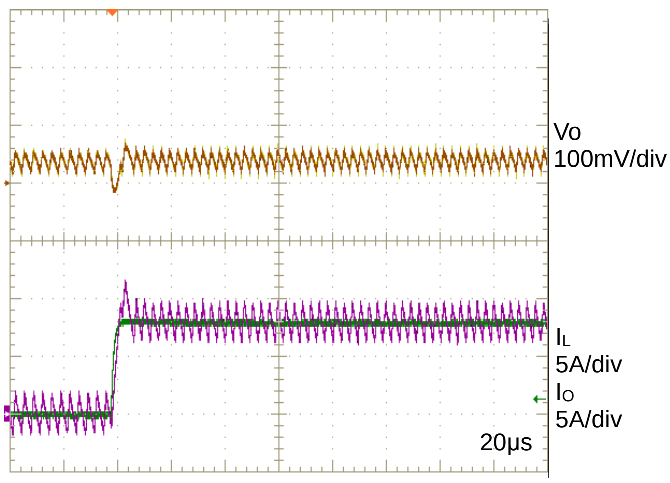


Figure 24. Transient Response
(Vo= 3.3V, PWM, Io= 0A→8A)

Typical Performance Curves - continued

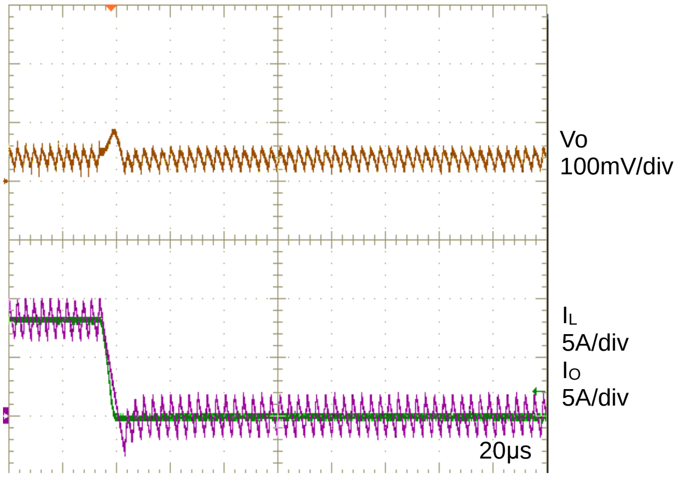


Figure 25. Transient Response
(Vo= 3.3V, PWM, Io= 8A→0A)

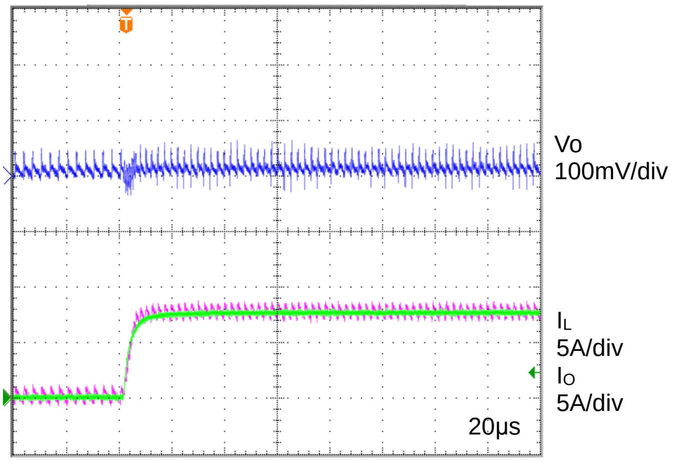


Figure 26. Transient Response
(Vo= 1V, PWM, Io= 0A→8A)

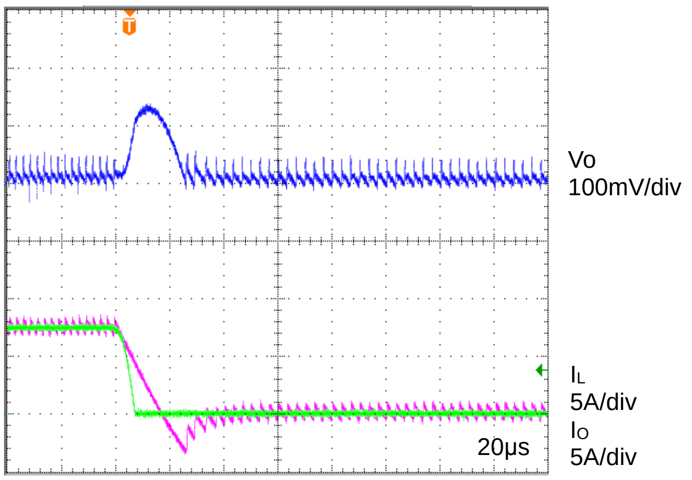


Figure 27. Transient Response
(Vo= 1V, PWM, Io= 8A→0A)

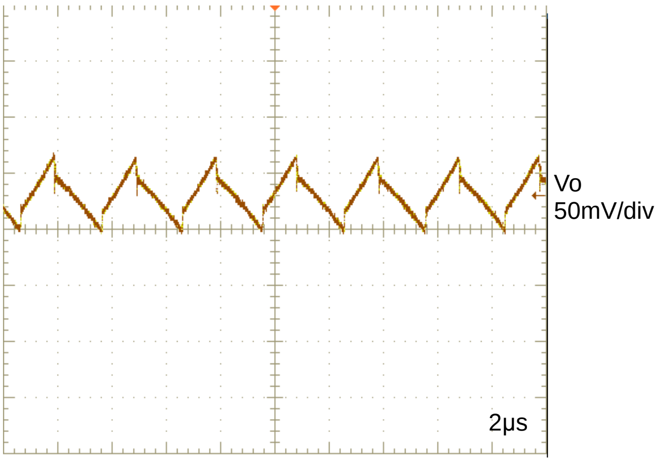


Figure 28. Output Voltage
(Vo= 5V, PWM, Io= 0A)

Typical Performance Curves - continued

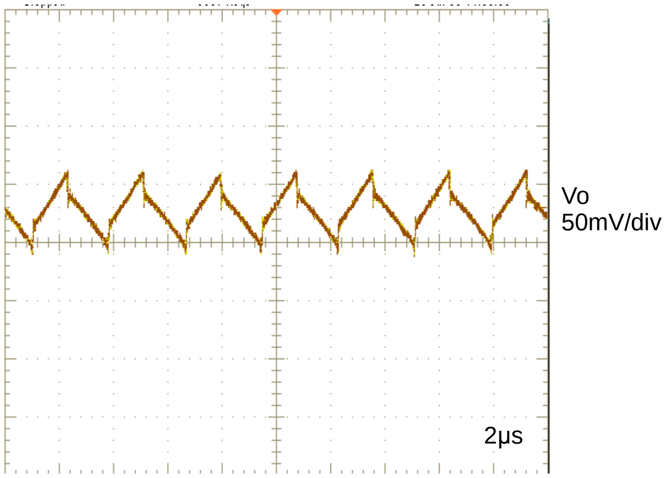


Figure 29. Output Voltage
(Vo= 5V, PWM, Io= 8A)

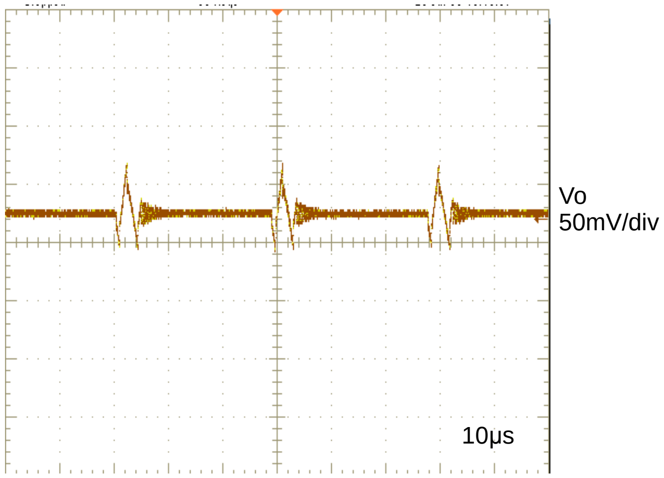


Figure 30. Output Voltage
(Vo= 5V, QLLM, Io= 0A)

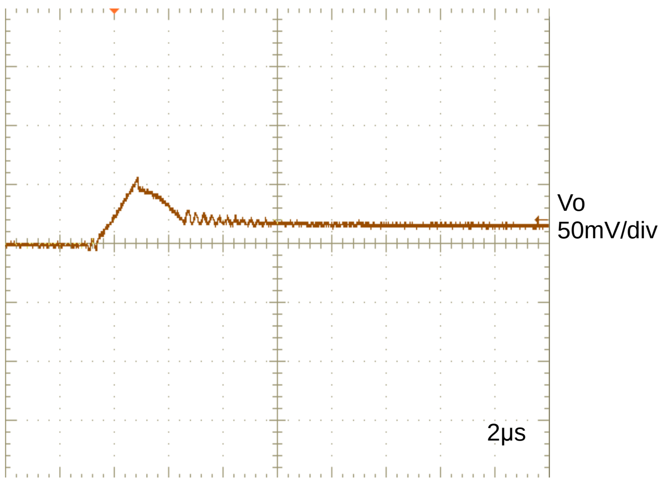


Figure 31. Output Voltage
(Vo= 5V, SLLM, Io= 0A)

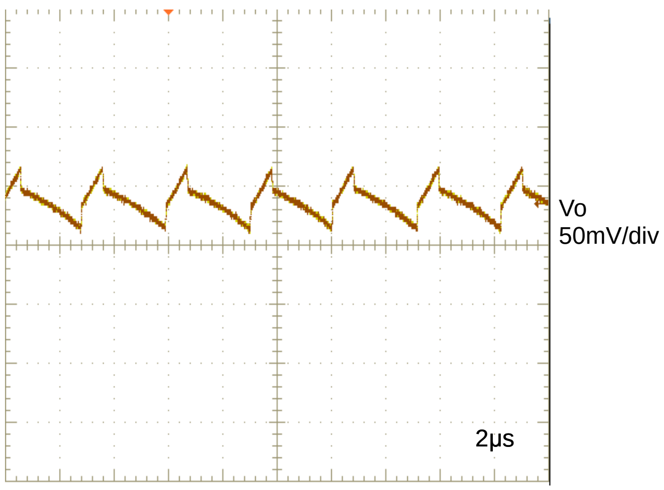


Figure 32. Output Voltage
(Vo= 3.3V, PWM, Io= 0A)

Typical Performance Curves - continued

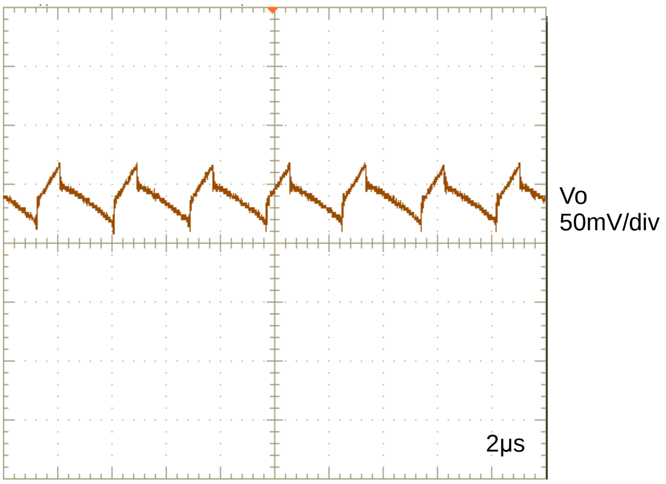


Figure 33. Output Voltage
(Vo= 3.3V, PWM, Io= 8A)

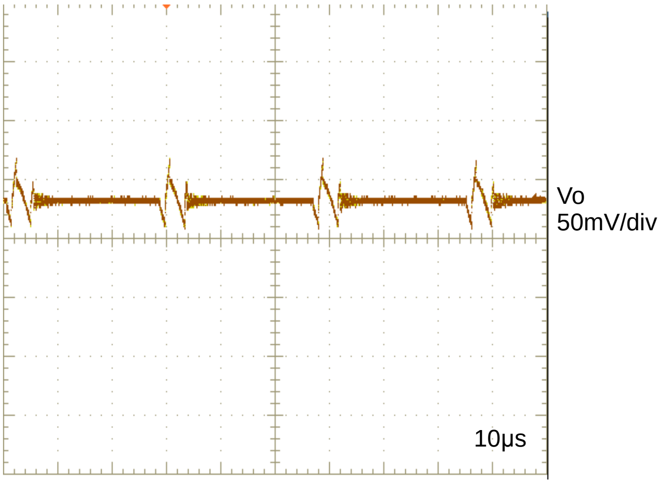


Figure 34. Output Voltage
(Vo= 3.3V, QLLM, Io= 0A)

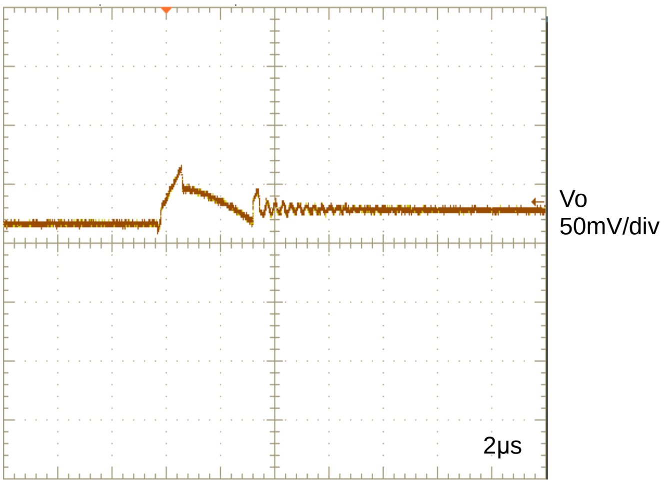


Figure 35. Output Voltage
(Vo= 3.3V, SLLM, Io= 0A)

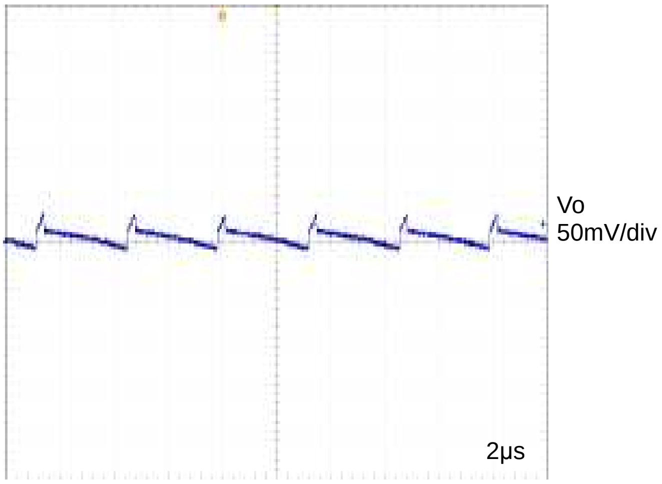
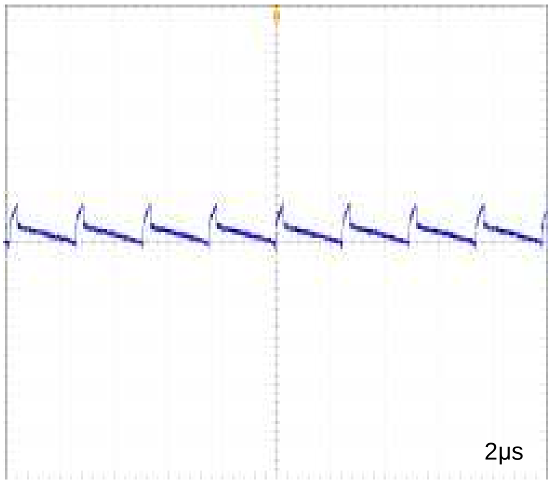


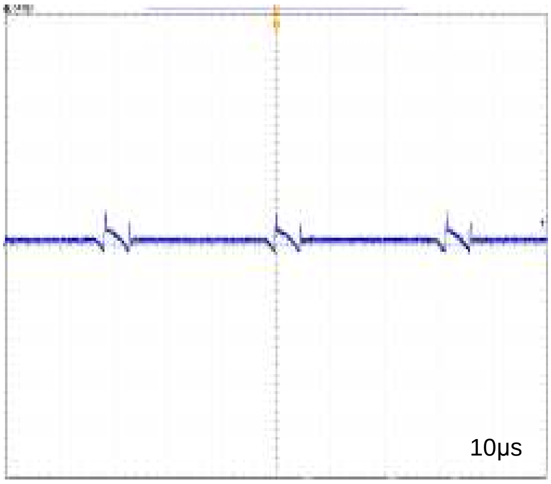
Figure 36. Output Voltage
(Vo= 1V, PWM, Io= 0A)

Typical Performance Curves - continued



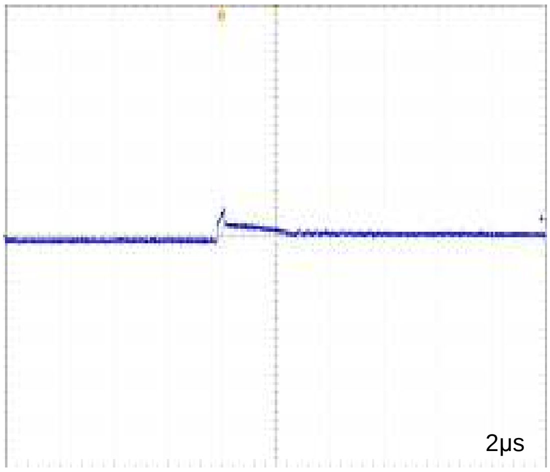
Vo
50mV/div

Figure 37. Output Voltage
(Vo= 1V, PWM, Io= 8A)



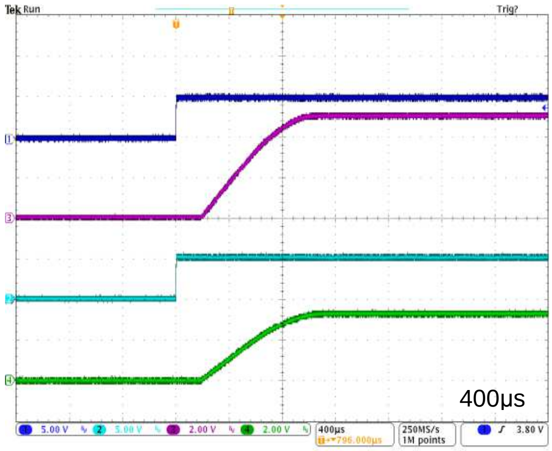
Vo
50mV/div

Figure 38. Output Voltage
(Vo= 1V, QLLM, Io= 0A)



Vo
50mV/div

Figure 39. Output Voltage
(Vo= 1V, SLLM, Io= 0A)



EN1
5V/div
Vo1
2V/div
EN2
5V/div
Vo2
2V/div

Figure 40. Start-up
(EN1= EN2)

Typical Performance Curves - continued

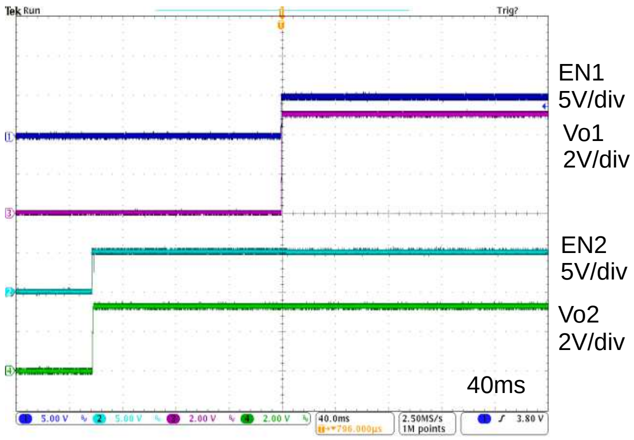


Figure 41. Start-up
(EN2→EN1)

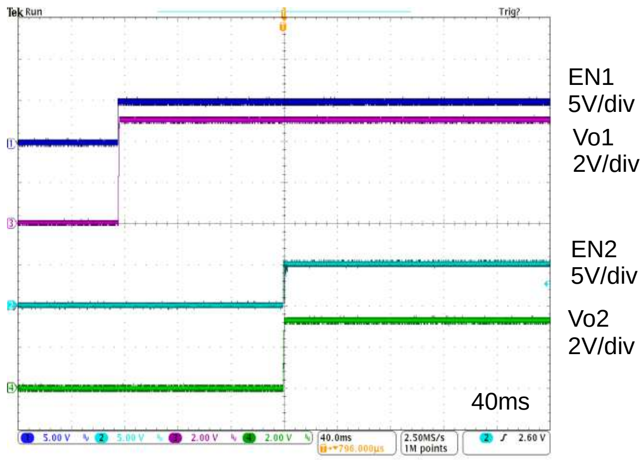


Figure 42. Start-up
(EN1→EN2)

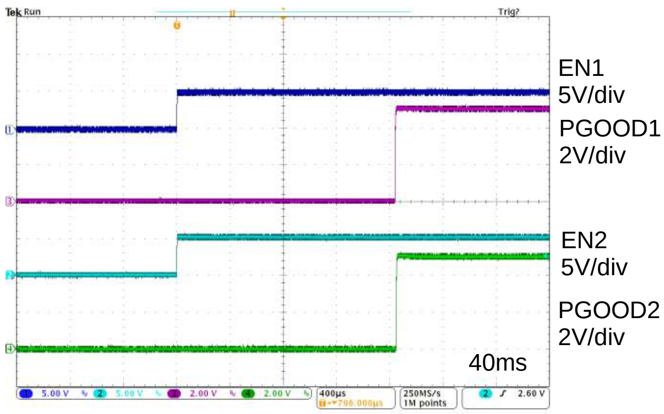


Figure 43. Start-up
(EN1/2→PGOOD1/2)

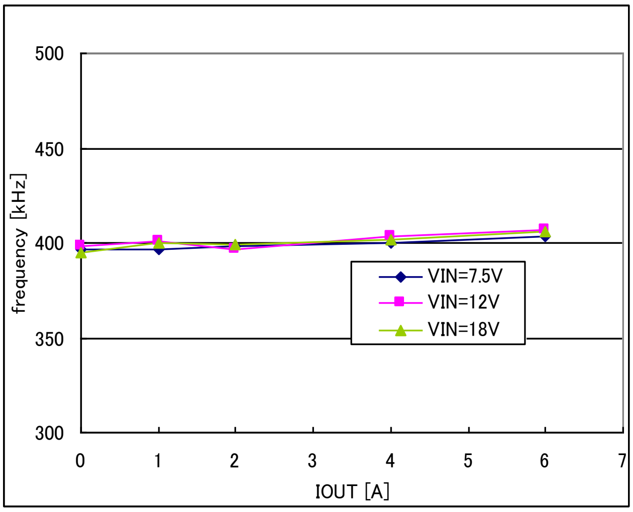


Figure 44. Io-frequency
(Vo= 5V, PWM, RFS= 68kΩ)

Typical Performance Curves - continued

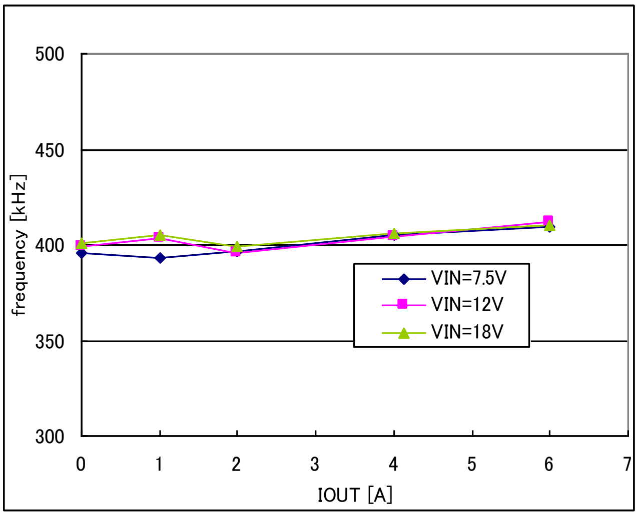


Figure 45. Io-frequency
(Vo= 3.3V, PWM, RFS= 68kΩ)

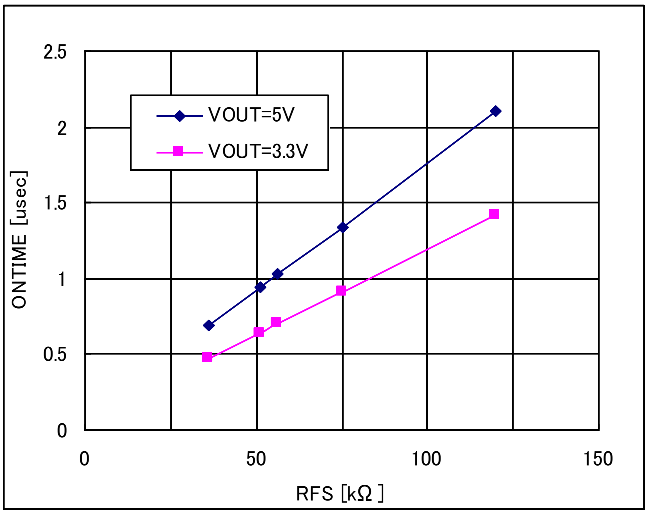


Figure 46. On time-RFS

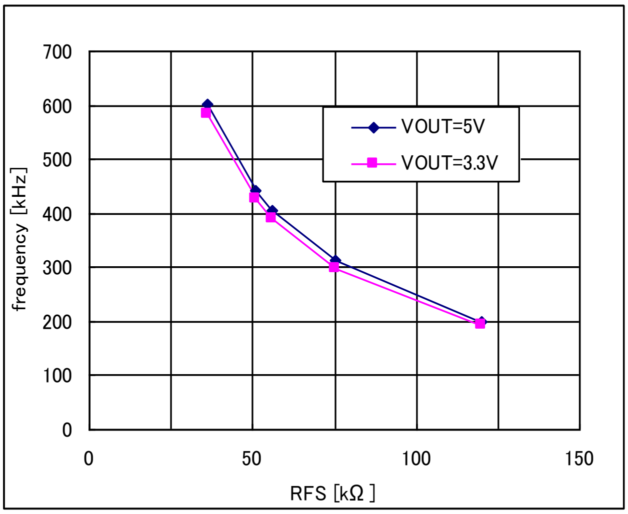


Figure 47. SW Frequency-RFS

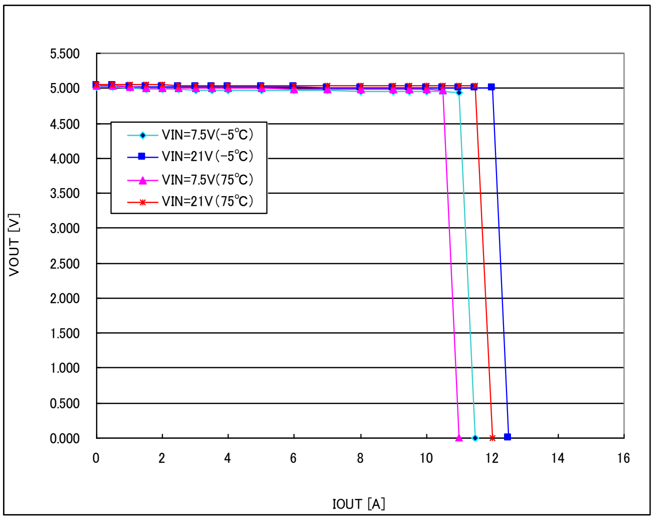


Figure 48. Current Limit
(Vo= 5V)

Typical Performance Curves - continued

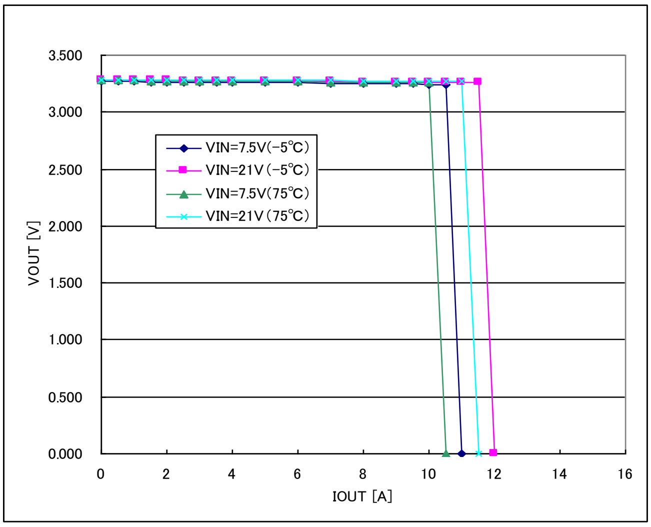


Figure 49. Current Limit
(Vo= 3.3V)

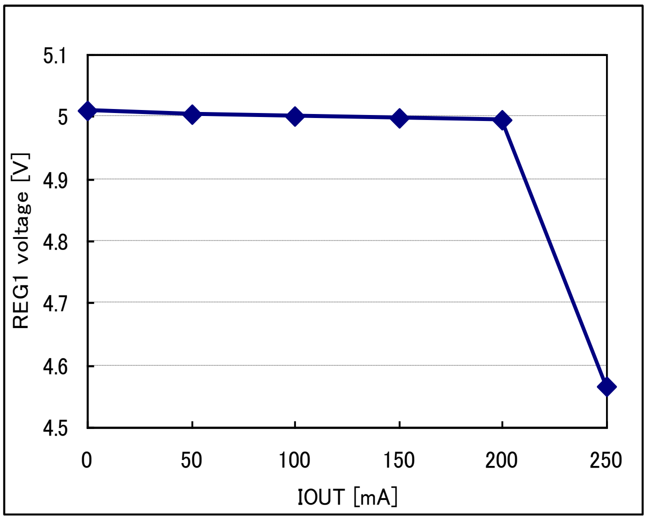


Figure 50. REG1 Load Regulation

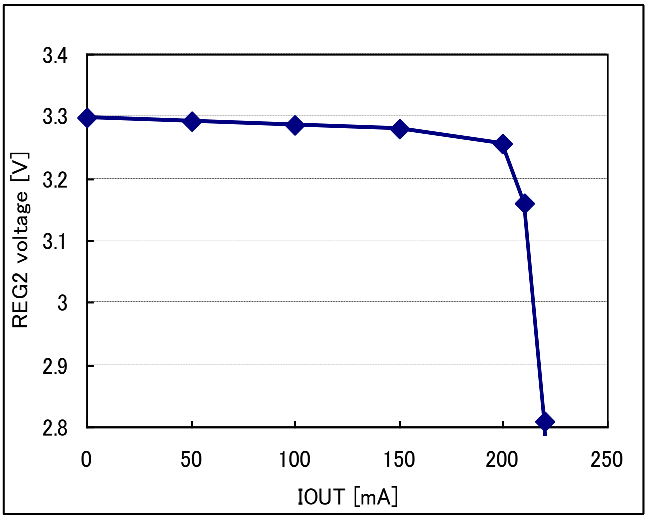
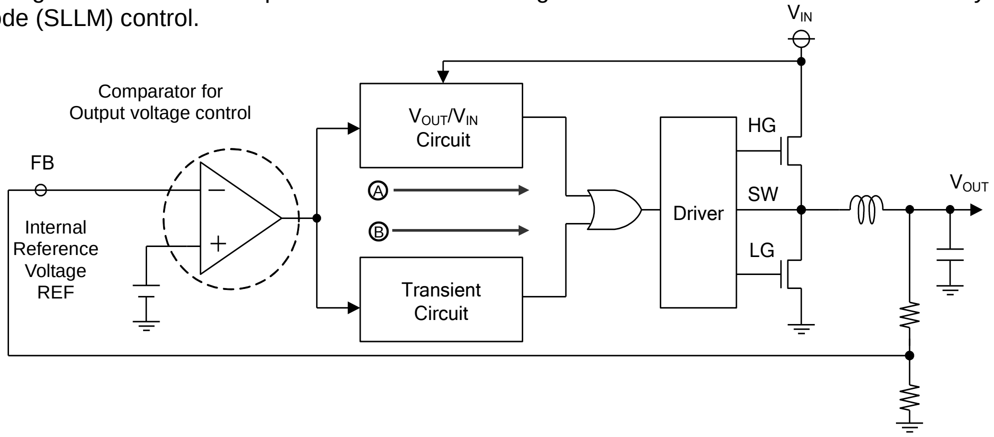


Figure 51. REG2 Load Regulation

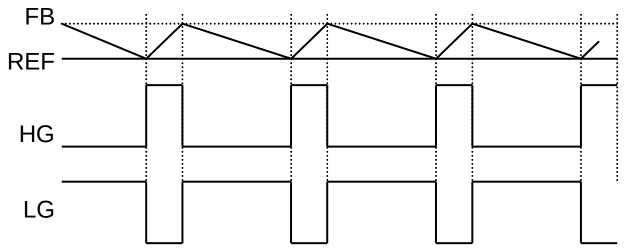
Description of Block

BD9528AMUV is a dual channel synchronous buck regulator using H3RegTM, Rohm's latest constant on-time controller technology. Fast load response is achieved by controlling the output voltage using a comparator without relying on the switching frequency.
When V_{OUT} drops due to a rapid load change, the system quickly restores V_{OUT} by extending the t_{ON} time interval. Thus, it serves to improve the regulator's transient response. Activation of the light load mode further increases efficiency by using Simple Light Load Mode (SLLM) control.

H3RegTM Control



(Normal operation)

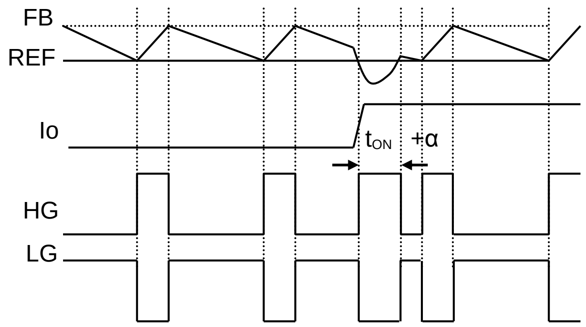


When FB falls to a reference voltage (REF), the drop is detected, activating the H3RegTM control system

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \cdot\cdot\cdot (1)$$

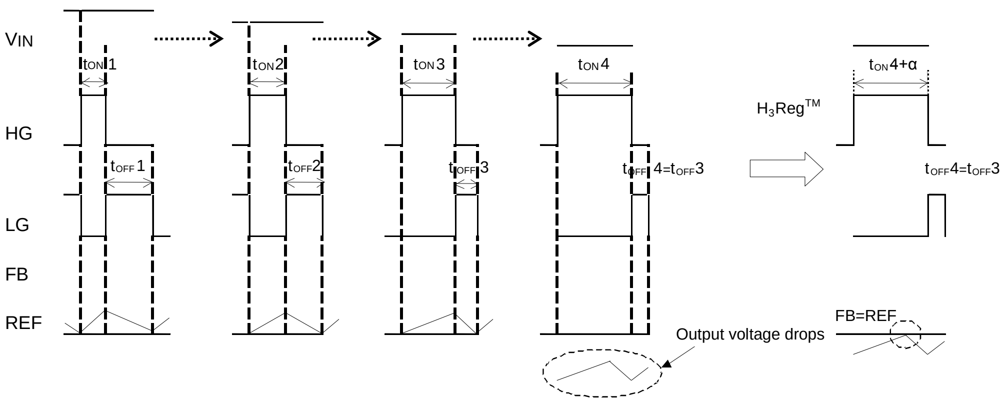
HG output on-time is determined by the formula (1).
When HG is off, LG is on until the output voltage becomes FB= REF.
After the status of HG is off, LG go on outputting until output voltage become FB= REF.

(V_{OUT} drops due to a rapid load change)



When V_{OUT} drops due to a rapid load change, and the voltage remains below the output setting following the programmed t_{ON} time, the system quickly restores V_{OUT} by extending the t_{ON} time, thus improving the transient response. Once V_{OUT} is restored, the controller continues normal operation.

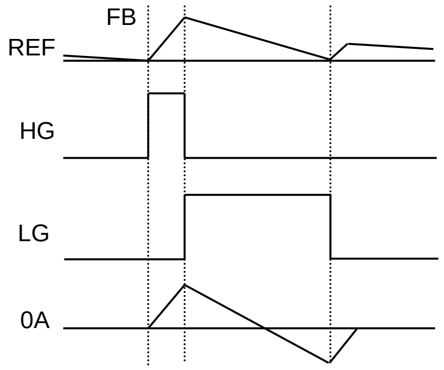
(When V_{IN} drops)



Based on the value of V_{IN}, the on-time t_{ON} and off-time t_{OFF} are determined by t_{ON}= V_{OUT} / V_{IN} x I/f and t_{OFF}= (V_{IN}- V_{OUT})/V_{IN}. As the V_{IN} voltage drops, in order to maintain the output voltage, t_{ON} becomes longer and t_{OFF} is shorter. However, for normal operation, if V_{IN} drops further, t_{ON} is longer and t_{OFF}= tminoff (minimum off- time is defined internally), the output voltage will decrease because t_{OFF} cannot be any shorter than the minimum off-time. With H3RegTM, if V_{IN} goes even lower, the output voltage is maintained as the t_{ON} time is extended. (t_{ON} time is extended until FB>REF). In this case, the switching frequency is lowered so that the t_{ON} time can be extended.

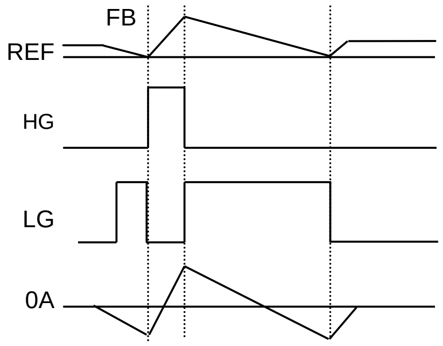
Description of Block - continued

Light Load Control
(SLLM)



SLLM will activate when the LG pin is off and the coil current is near 0A (current flows from V_{OUT} to SW).
When the FB input is lower than the REF voltage again, HG will be enabled once again.

(QLLM)

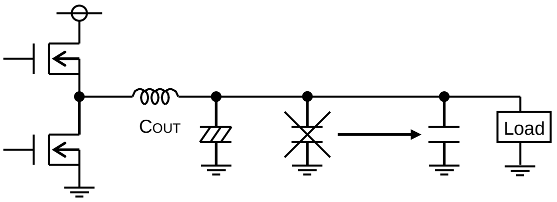


QLLM will activate when the LG pin is off and the coil current is near 0A (current flows from V_{OUT} to SW). In this case, the next HG is prevented. Then, when FB falls below the output programmed voltage within the programmed time (Typ= 40µs), HG will resume. In the case where FB doesn't fall in the programmed time, LG is forced on causing V_{OUT} to fall. As a result, the next HG is on.

MCTL1	MCTL2	Control Mode	Start-up
L	L	SLLM	PWM
L	H	QLLM	PWM
H	X	PWM	PWM

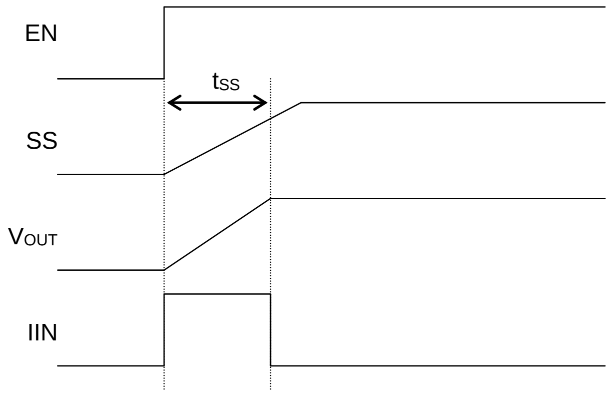
The BD9528AMUV operates in PWM mode until the SS input reaches the clamp voltage (2.5V), regardless of the control mode setting, this assures stable operation while the during soft start.

*Attention: To effect the rapid transient response, the H^3Reg^{TM} control monitors the current from the output capacitor to the load using the ESR of the output capacitor Do not use ceramic capacitors on C_{OUT} side of power supply. Ceramic bypass capacitors can be used near the individual loads if desired.



Timing Chart

・Soft Start Function



Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage "ramping start." Soft start timing and incoming current are calculated with formulas (2) and (3) below.

・Soft start time

$$t_{SS} = \frac{0.7(Typ) \times C_{SS}}{2.3\mu A(Typ)} < 100m \quad [sec] \quad \cdots (2)$$

C_{SS}(pF)	Soft start time(ms)
18000	5
33000	10
68000	20

・ Inrush current

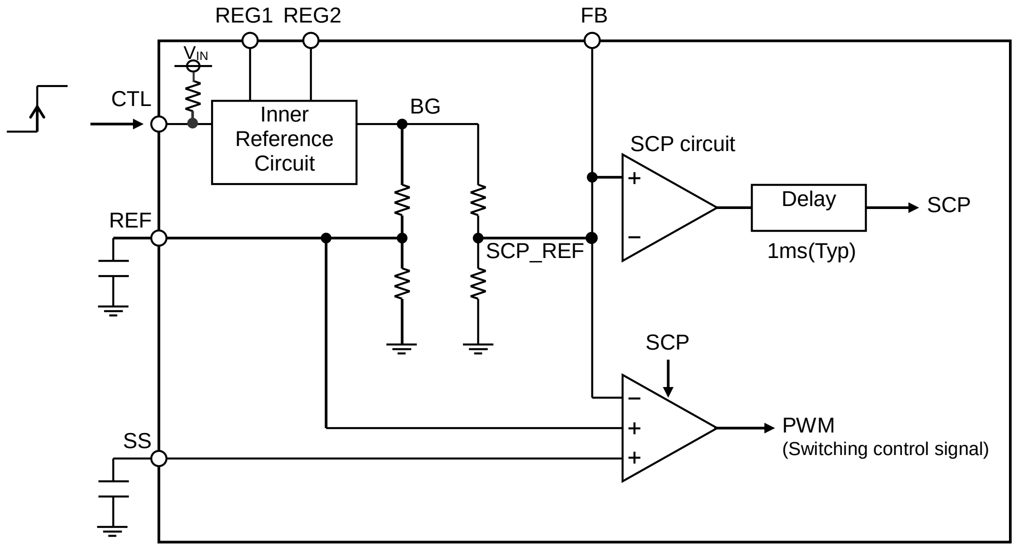
$$I_{in} = \frac{C_o \times V_{OUT}}{t_{SS}} \times \frac{V_{OUT}}{V_{IN}} \quad [A] \quad \cdots (3)$$

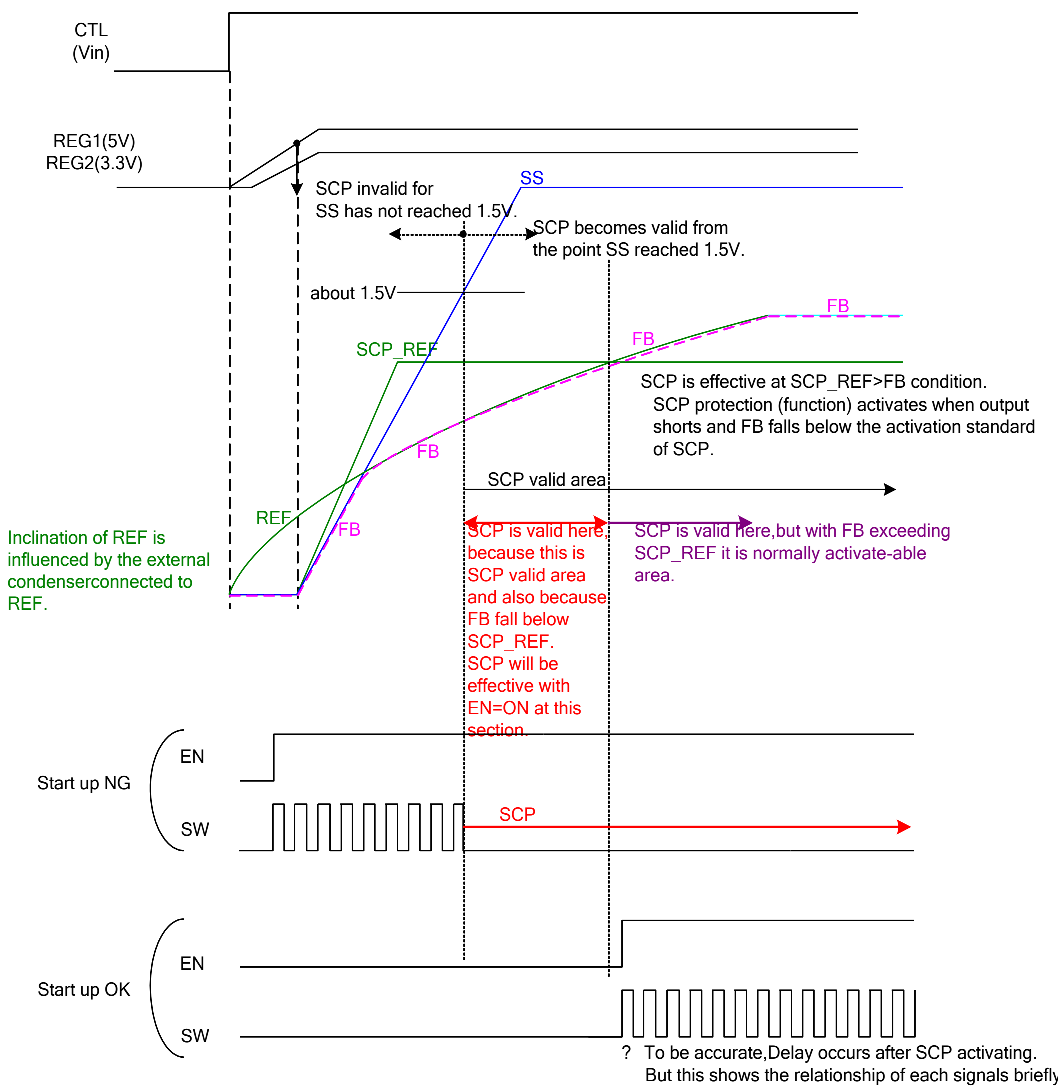
(Css: Soft start capacitor Co: Output capacitor)

*Notice : Max ontime function is disable by SS voltage reach to 2.5V.

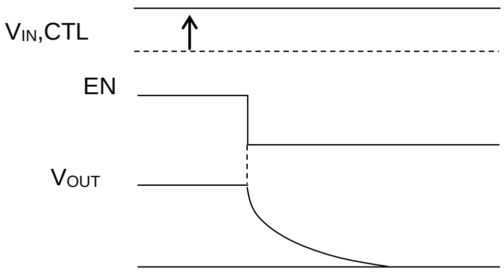
Timing Chart - continued

・Notes when waking up with CTL pin or V_{IN} pin
If EN pin is high or short (or pull up resistor) to REG1 pin, IC starts up by switching CTL pin, the IC might fail to start up (SCP function) with the reason below, please be careful of SS pin and REF pin capacitor capacity.



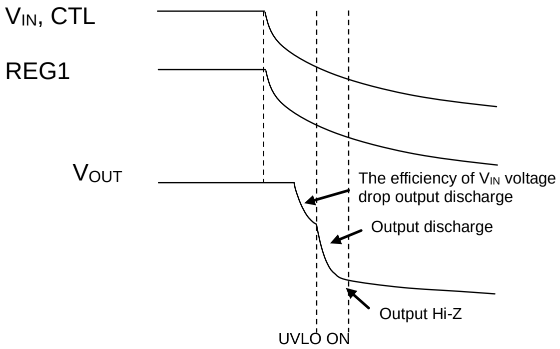


Output Discharge



It will be available to use if connecting V_{OUT} pin to DC/DC output. (about 100Ω) . Discharge function operates when <1> EN='L'
<2> UVLO= ON(If input voltage is low) <3> SCP latch
<4> TSD= ON.
The function at output discharge time is shown as left.

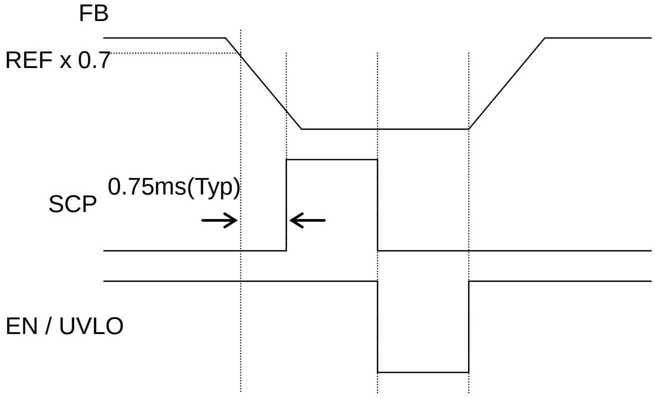
[1] When switch to low from high with EN pin.
If EN pin voltage is below than EN threshold voltage, output discharge function is operated, and discharge output capacitor charge.



[2] When switch to low from high with EN pin

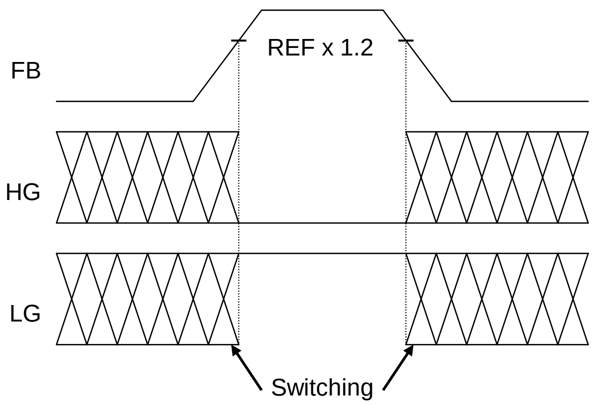
1) IC is in normal operation until REG1 voltage becomes lower than UVLO voltage. However, because V_{IN} voltage also becomes low, output voltage will drop, too.
2) If REG1 voltage reaches the UVLO voltage, output discharge function is operated, and discharge output capacitor charge.
3) In addition, if REG1 voltage drops, inner IC logic cannot operate, so that output discharge function does not work, and becomes output Hi-z. (In case, FB has resistor against ground, discharge at the resistor.)

・Timer Latch Type Output Short Circuit Protection



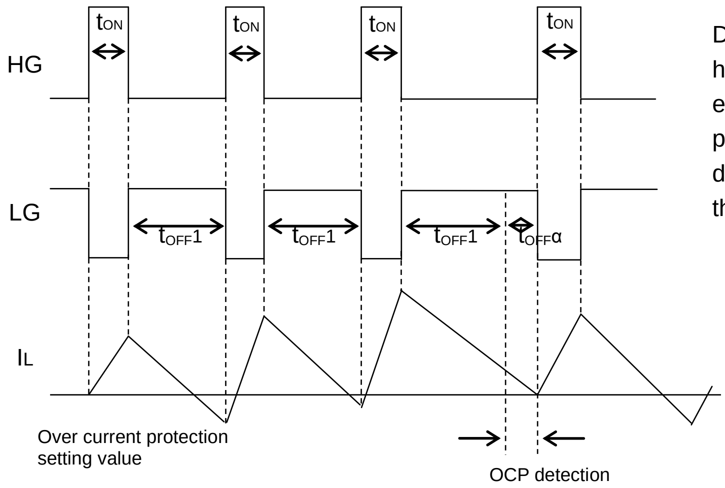
Short protection is enabled when the output voltage falls to or below REF X 0.7.
Once the programmed time period has elapsed, the output is latched off to prevent destruction of the circuit. (HG= Low, LG= Low) Output voltage can be restored either by cycling the EN pin or disabling UVLO.

・Over Voltage Protection



When the output voltage increases to or above REF x 1.2(Typ), output over voltage protection is enabled, and the Low-side FET turns on to reduce the output. (LG= High, HG= Low).
When the output falls to within normal operation, the function is restored to normal operation.

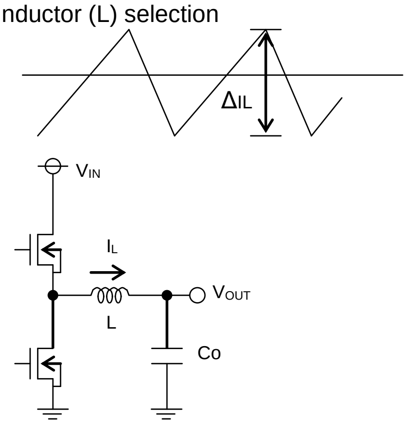
・Over current protection circuit



During normal operation, if FB is less than REF, HG is high during the time t_{ON}, but when the coil current exceeds the I_{LIMIT} threshold, HG is set to off. The next pulse returns to normal operation if the output voltage drops after the maximum on-time or I_L becomes lower than I_{LIMIT}.

Selection of Components Externally Connected

1.Inductor (L) selection



Output ripple current

The inductor value is a major influence on the output ripple current. As formula (4) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \ [A] \cdots (4)$$

Generally, lower inductance values offer faster response times but also result in increased output ripple and lower efficiency.

0.47µH to 2.2µH are recommended as appropriate setting value.

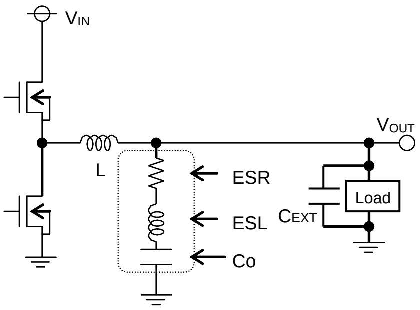
The peak current rating of coil is approximated by formula (5). Please select inductor which is higher than this value.

$$I_{LPEAK} = I_{OUTMAX} + \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{2 \times L \times V_{IN} \times f} \ [A] \cdots (5)$$

*Passing a current larger than inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.

*To minimize possible inductor damage and maximize efficiency, choose an inductor with a low (DCR, ACR) resistance.

2. Output Capacitor (CO) Selection



Output Capacitor

The output capacitor should be determined by equivalent series resistance and equivalent series inductance so that the output ripple voltage is 30mV or more.
The rating of the capacitor is selected with sufficient margin given the output voltage.

$$\Delta V_{OUT} = \Delta IL \times ESR + ESL \times \Delta IL / t_{ON} \cdots (6)$$

ΔIL: Output ripple current
ESR: Equivalent series resistance,
ESL: Equivalent series inductance

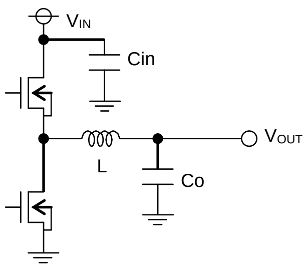
Please give due consideration to the conditions in formula (7) below for the output capacitor, bearing in mind that the output start-up time must be established within the soft start timeframe. Capacitors used as bypass capacitors are connected to the load side affect the overall output capacitance (C_{EXT}, figure above). Please set the soft start time or over-current detection value, regarding these capacities.

$$Co + C_{EXT} \leq \frac{T_{SS} \times (Limit - I_{OUT})}{V_{OUT}} \cdots (7)$$

T_{SS} : Soft start time
Limit : Over current detection

Note: If an inappropriate capacitor is used, OCP may be detected during activation and may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



Input Capacitor

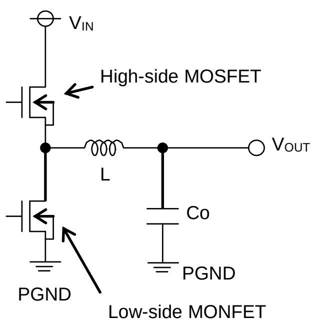
The input capacitor selected must have low enough ESR to fully support high output ripple so as to prevent extreme over current conditions. The formula for ripple current IRMS is given in (8) below.

$$IRMS = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}} \ [A] \cdots (8)$$

$$\text{Where } V_{IN} = 2 \times V_{OUT},\ IRMS = \frac{I_{OUT}}{2}$$

A ceramic capacitor is recommended to reduce ESR loss and maximize efficiency.

4.MOSFET Selection



High-side driver and Low-side driver are designed to activate N channel MOSFET's with low on-resistance.
The chosen MOSFET may result in the loss described below, please select a proper FET for each considering the input-output and load current.

< Loss of High-side MOSFET >

Pmain= P_{RON}+P_{TRAN}

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + \frac{(Tr+Tf) \times V_{IN} \times I_{OUT} \times f}{6} \quad \cdots (9)$$

(Ron: On-resistance of FET
f: Switching frequency
Tr: Rise time, Tf: Fall time)

< Loss of Low-side MOSFET >

Psyn= P_{RON}

$$= \frac{V_{IN} - V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 \quad \cdots (10)$$

The High-side MOSFET generates loss when switching, along with the loss due to on-resistance.
Good efficiency is achieved by selecting a MOSFET with low on-resistance and low Qg (gate total charge amount).
Recommended MOSFETs for various current values are as follows:

Output current	High-side MOSFET	Low-side MOSFET
to 5A	RQ3E080GN	RQ3E100GN
5 to 8A	RQ3E120GN	RQ3E150GN
8 to 10A	RQ3E150GN	RQ3E180GN

5. Output Voltage Set Point

This IC operates such that output voltage is REF ≅ FB.

<Output Voltage>

$$V_{OUT} = \frac{(R1+R2)}{R2} \times REF(0.7V) + \frac{1}{2}\Delta V_{OUT}$$

(ΔV_{OUT}: Output ripple voltage)

$$\Delta V_{OUT} = \Delta I_L \times ESR$$

(ΔI_L: ripple current of coil)

$$\Delta I_L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{(L \times V_{IN} \times f)}$$

L: inductance[H]   f: switching frequency[Hz]

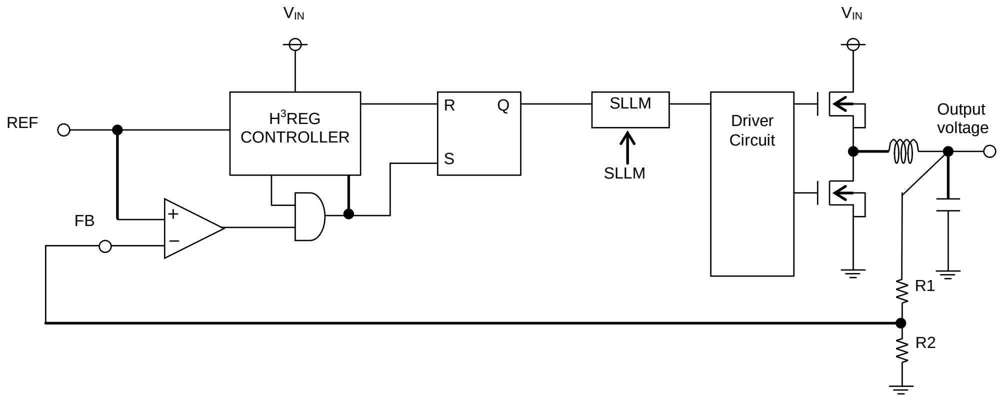
*(Notice)Please set output ripple voltage more than 30mV to 50mV.

(Example) V_{IN}= 20V, V_{OUT}= 5V, f= 300kHz, L= 2.5µH, ESR= 20mΩ, R1= 56kΩ, R2= 9.1kΩ

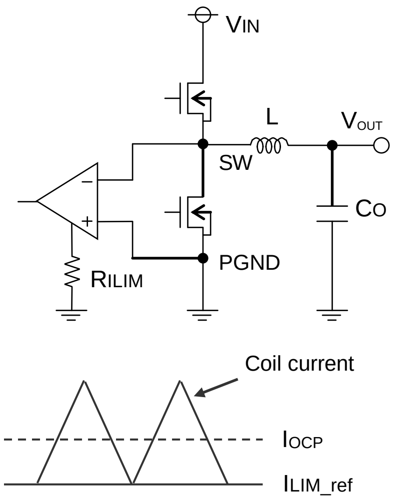
$$\Delta I_L = (20V-5V) \times \frac{5V}{(2.5 \times 10^{-6}H \times 20V \times 300 \times 10^{3}Hz)} = 5(A)$$

$$\Delta V_{OUT} = 5A \times 20 \times 10^{-3}\Omega = 0.1(V)$$

$$V_{OUT} = 0.7V \times \frac{(51k\Omega + 9.1k\Omega)}{9.1k\Omega} + \frac{1}{2} \times 0.1V = 5.057(V)$$



6. Setting over current protection



The on resistance (between SW and PGND) of the low side MOSFET is used to set the over current protection.
Over current reference voltage (I_{LIM_ref}) is determined as in formula(11) below.

$$I_{LIM\_ref} = \frac{10k}{R_{ILIM}[k\Omega] \times R_{ON}[m\Omega]} \text{ [A]} \cdots (11)$$

(R_{ILIM}: Resistance for setting of over current voltage protection value[kΩ]
R_{ON}: Low-side on resistance value of FET[mΩ])

Over current protection is actually determined by the formula (12) below.

$$I_{ocp} = I_{LIM\_ref} + \frac{1}{2}\Delta I_L$$
$$= I_{LIM\_ref} + \frac{1}{2} \times \frac{V_{IN} - V_O}{L} \times \frac{I}{f} \times \frac{V_O}{V_{IN}} \cdots (12)$$

ΔI_L:Coil ripple current[A]
V_{IN}:Input voltage[V]
V_O:Output voltage [V]
f:Switching frequency [Hz]
L:Inductance [H]

(Example)
If a load current 5A is desired with V_{IN}=6 to 19V, V_{OUT}=5V, f=400kHZ, L=2.5μH, RON=20mΩ, the formula would be:

$$I_{OCP} = \frac{10k}{R_{ILIM}[k\Omega] \times R_{ON}[m\Omega]} + \frac{1}{2} \times \frac{V_{IN} - V_O}{L} \times \frac{I}{f} \times \frac{V_O}{V_{IN}} > 5$$

When V_{IN}= 6V, I_{OCP} will be minimum(this is because the ripple current is also minimum) so that if each condition is input, the formula will be the following: RILIM<109.1[kΩ].

*To design the actual board, please consider enough margin for FET on resistance variation, Inductance variation, IC over current reference value variation, and frequency variation.

7. Relation between output voltage and t_{ON} time

For BD9528AMUV, both channels, are high efficiency synchronous regulator controllers with variable frequency. t_{ON} time varies with Input voltage [V_{IN}], output voltage [V_{OUT}], and RFS of FS pin resistance.

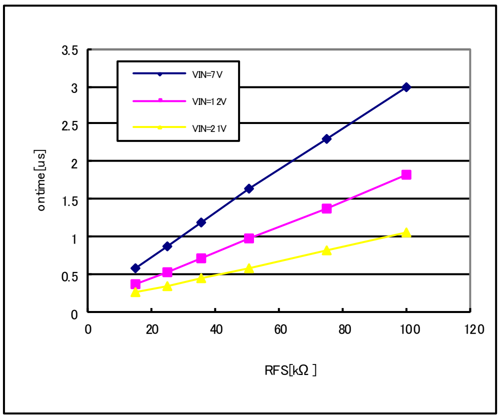


Figure55. RFS – ontime(V_{OUT}= 5V)

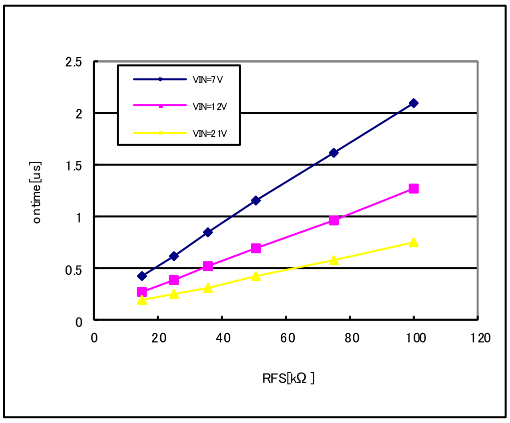


Figure56. RFS – ontime(V_{OUT}= 3.3V)

From t_{ON} time, frequency on application condition is following:

$$\text{Frequency} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{t_{ON}} \text{ [kHz]} \cdots (13)$$

However, real-life considerations (such as the external MOSFET gate capacitor and switching speed) must be factored in as they affect the overall switching rise and fall time, so please confirm by experiment.

Application Example (Vin= 12V, Vo1= 3.3V/8A, f1= 400kHz, Vo2= 2.5V/8A, f2= 400kHz)

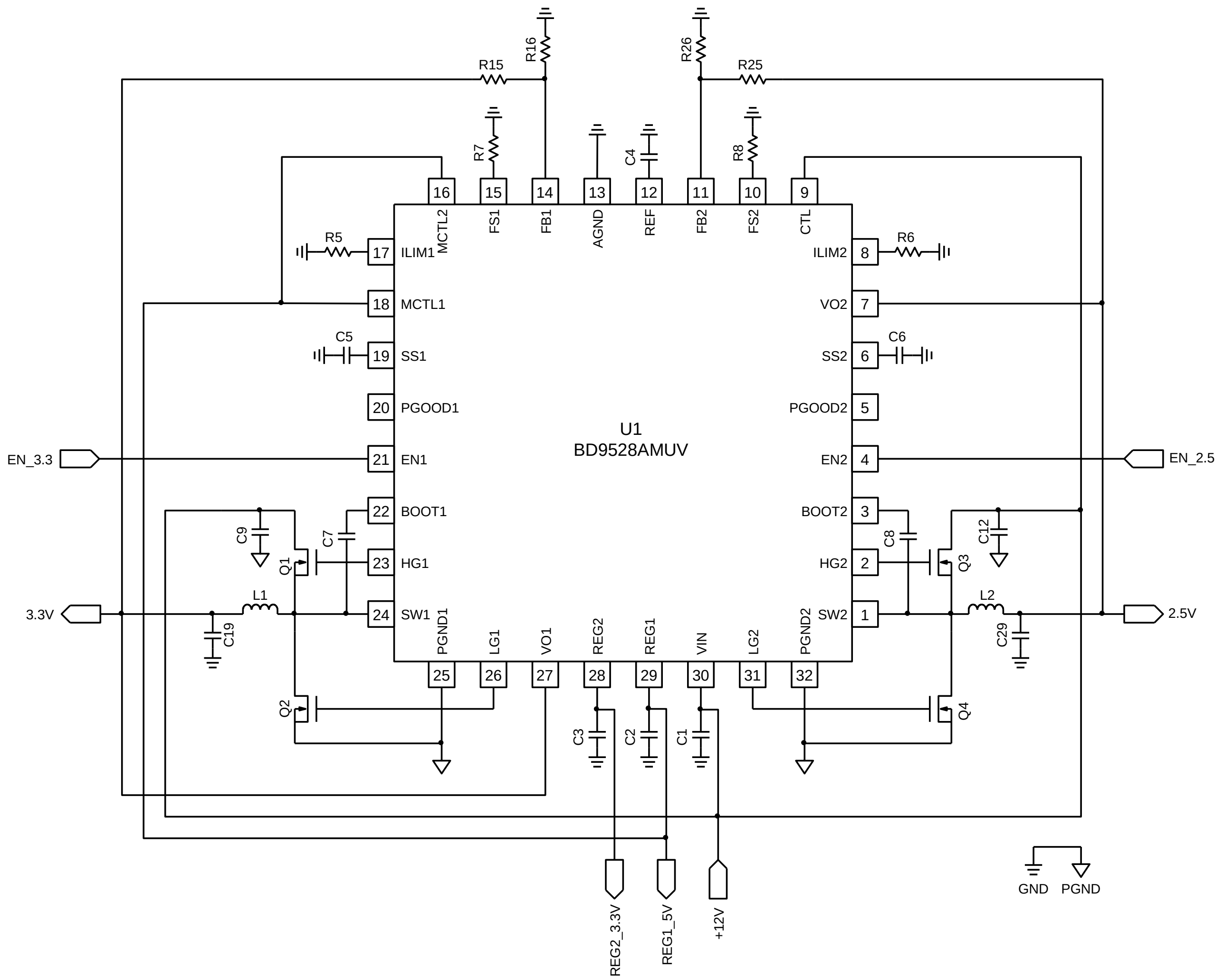
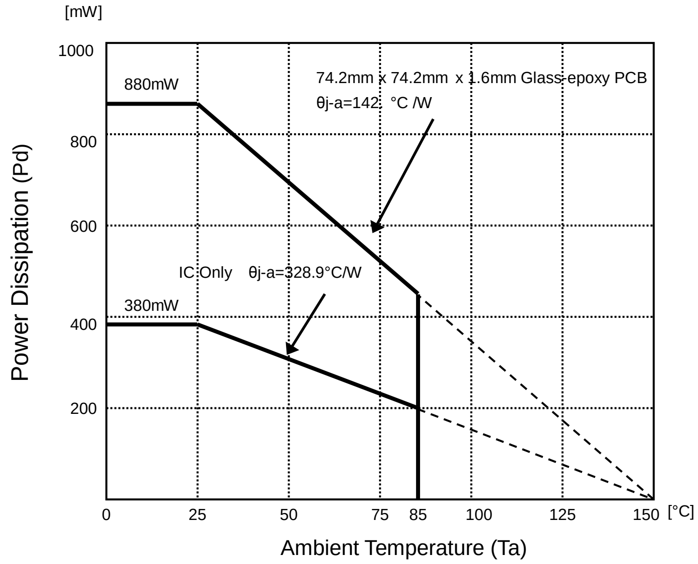


Figure 57. Application Example

Reference Designator	Type	Value	Description	Manufacturer Part Number	Manufacturer	Configuration (mm)
C1, C9, C10, C11, C12	Ceramic Capacitor	10µF	35V, X5R, ±10%	GRM32ER6YA106KA12	MURATA	3225
C2, C3	Ceramic Capacitor	10µF	16V, X5R, ±10%	GRM21BR61C106ME15	MURATA	2012
C4, C5, C6	Ceramic Capacitor	0.1µF	16V, X5R, ±10%	GRM155R61C104KA88	MURATA	1005
C7, C8	Ceramic Capacitor	0.47µF	10V, X5R, ±10%	GRM188R61A474KA61	MURATA	1608
C18, C19, C28, C29	POSCAP	330µF	6.3V, ±20%, ESR 18mΩmax	6TPE330MIL	SANYO	7343
L1,L2	Inductor	1µH	±20%,10A(L=-30%), DCR=5.8mΩ±10%	GLMC1R003A	ALPS	6565
Q1, Q3	MOSFET	-	N-ch, Vdss 30V, Id 15A, Ron 4.7mΩ	RQ3E150GN	ROHM	3333
Q2, Q4	MOSFET	-	N-ch, Vdss 30V, Id 18A, Ron 3.3mΩ	RQ3E180GN	ROHM	3333
R5, R6	Resistor	62kΩ	1/16W, 50V, 5%	MCR01MZPJ623	ROHM	1005
R7, R8	Resistor	51kΩ	1/16W, 50V, 5%	MCR01MZPJ513	ROHM	1005
R15	Resistor	16kΩ	1/16W, 50V, 0.5%	MCR01MZPD1602	ROHM	1005
R16	Resistor	4.3kΩ	1/16W, 50V, 0.5%	MCR01MZPD4301	ROHM	1005
R24	Resistor	100Ω	1/16W, 50V, 5%	MCR01MZPJ101	ROHM	1005
R25	Resistor	12kΩ	1/16W, 50V, 0.5%	MCR01MZPD1202	ROHM	1005
R26	Resistor	4.7kΩ	1/16W, 50V, 0.5%	MCR01MZPD4701	ROHM	1005
U1	IC	-	Buck DC/DC Controller	BD9528AMUV	ROHM	VQFN032V5050

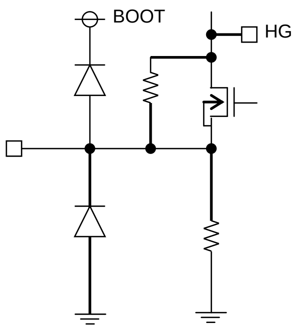
Without any ripple (about 10mV), there is a possibility that the FB signal is not stable due to the adoption of the comparator control method. Please ensure enough ripple voltage either by (1)reducing the L-value of inductor, or (2)using high ESR output capacitor. Ripple voltage can be generated in FB terminal by adding a capacitor in parallel to resistor (R17, R19) of the FB input, but the circuit will be sensitive to noise from the output (Vo1/Vo2) line and is not recommended. Stability of the circuit is influenced by the layout of the PCB, please pay careful attention to the layout.

Power Dissipation

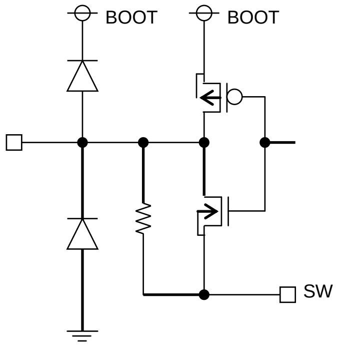


I/O equivalence circuits

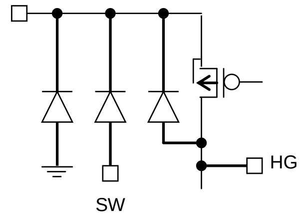
1, 24pin (SW2, SW1)



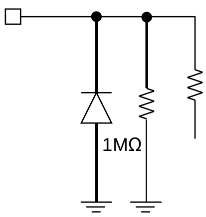
2, 23pin (HG2, HG1)



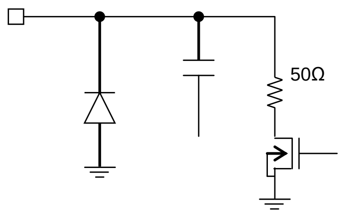
3, 22pin (BOOT2, BOOT1)



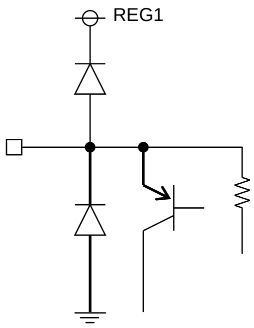
4, 21pin (EN2, EN1)



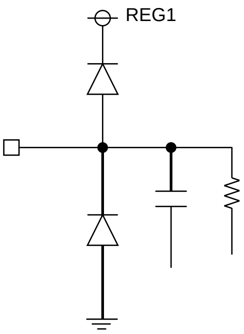
5, 20pin (PGOOD2, PGOOD1)



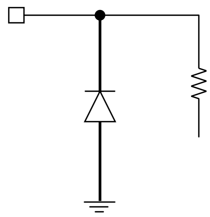
6, 19pin (SS2, SS1)



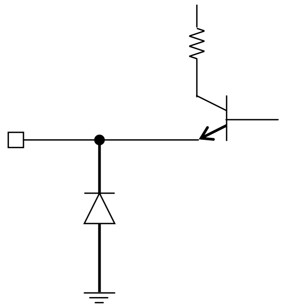
12pin (REF)



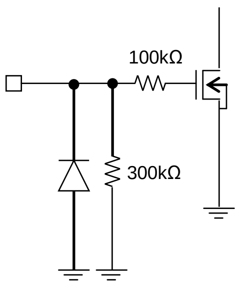
11, 14pin (FB2, FB1)



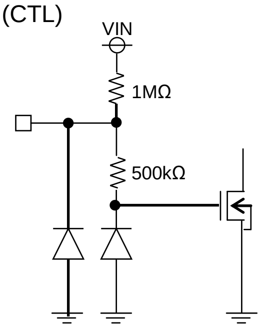
10, 15pin (FS2, FS1)



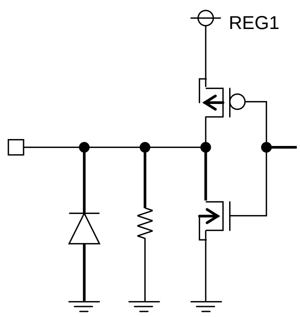
16, 18pin (MCTL2, MCTL 1)



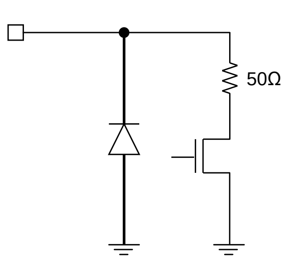
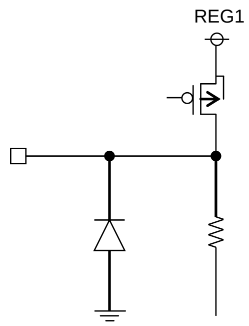
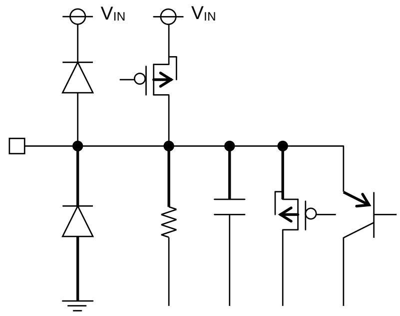
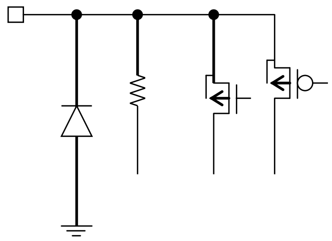
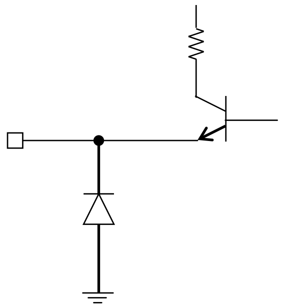
9pin (CTL)



26, 31pin (LG1, LG2)



I/O equivalence circuit(s) - continued

7, 27pin (Vo2, Vo1)  	28pin (REG2)  	29pin (REG1) 
30pin (VIN) 	8, 17pin (ILIM2, ILIM1) 	

Ordering Information

B D 9 5 2 8 A M U V - E 2

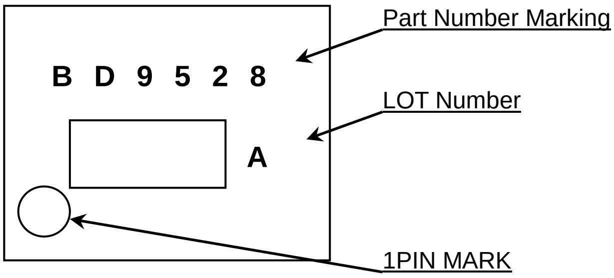
Part Number

Package
MUV: VQFN

Product class
LB for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel (VQFN032V5050)

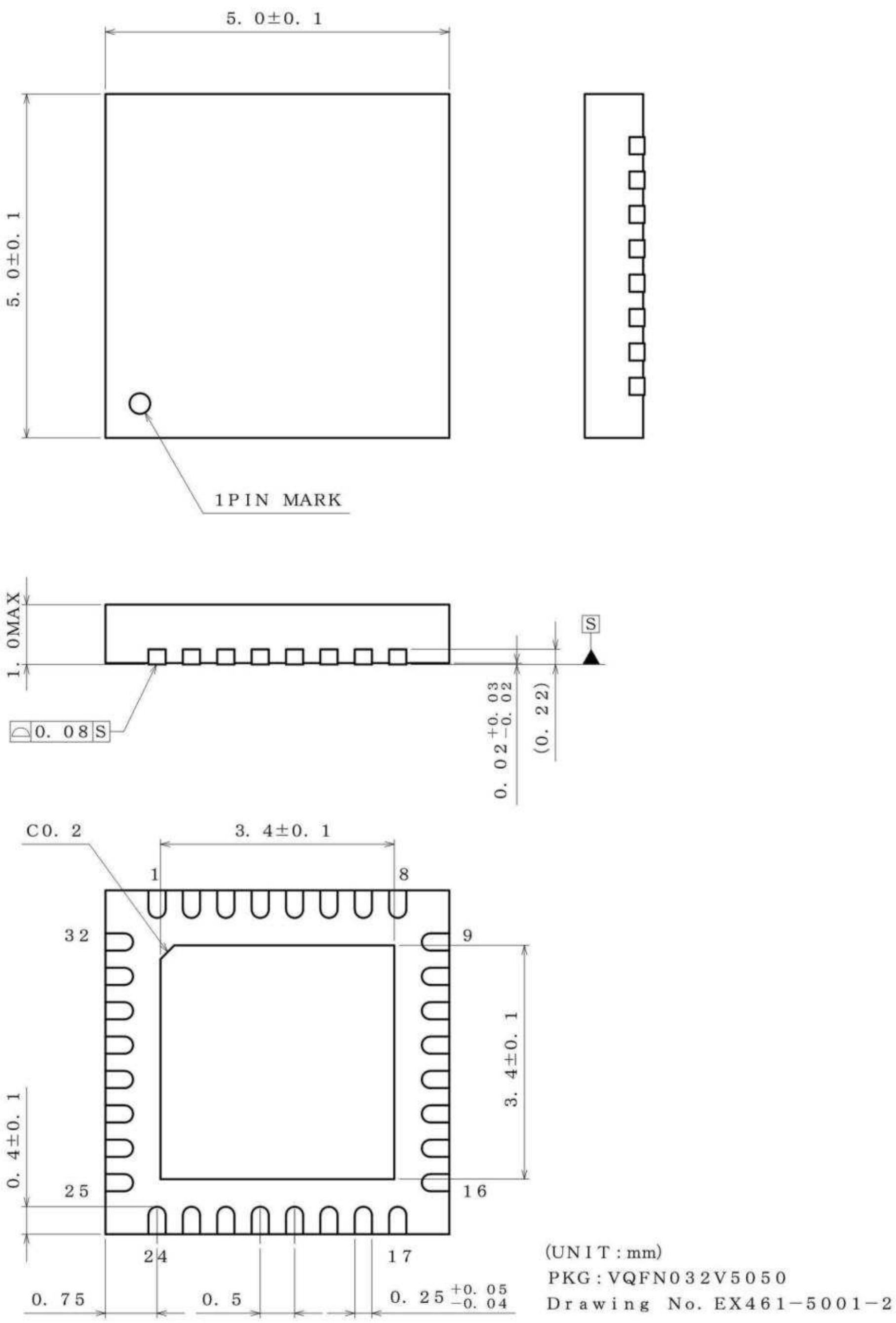
Marking Diagrams

VQFN032V5050
(TOP VIEW)



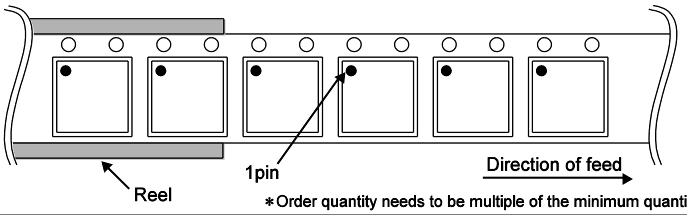
Physical Dimension, Tape and Reel Information

Package Name	VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
8.Jul.2016	001	New Release(Change Format)

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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