



BUK763R8-80E

N-channel TrenchMOS standard level FET

Rev. 2 — 16 May 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with VGS(th) rating of greater than 1V at 175 °C

1.3 Applications

- 12V, 24V and 48V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

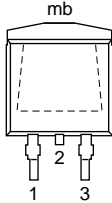
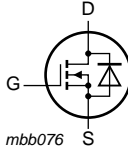
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	80	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	-	120	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	357	W
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11	-	3.1	3.8	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 64 V; see Figure 13 ; see Figure 14	-	51	-	nC

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK763R8-80E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
BUK763R8-80E	BUK763R8-80E

5. Limiting values

Table 5. Limiting values

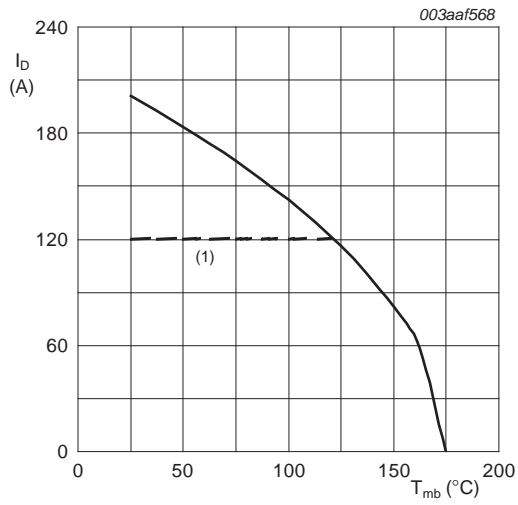
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	80	V	
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	80	V	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	[1]	-	120	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	[1]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 4	-	786	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	357	W	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	786	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; see Figure 3	[2][3]	-	488	mJ

[1] Continuous current is limited by package.

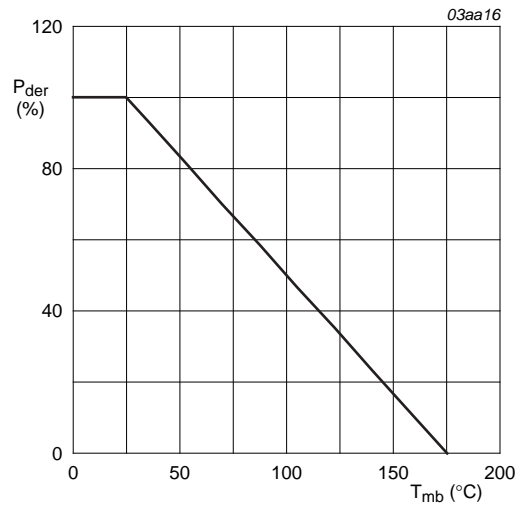
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Refer to application note AN10273 for further information.



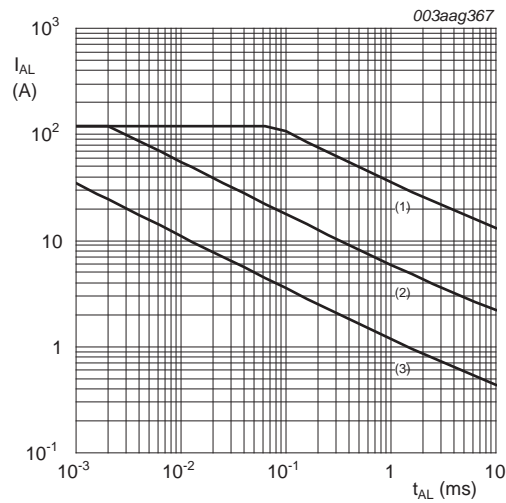
$V_{GS} \geq 10V$
 (1) Capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1) $T_j(amb) = 25^{\circ}C$; (2) $T_j(amb) = 150^{\circ}C$; (3) Repetitive Avalanche

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

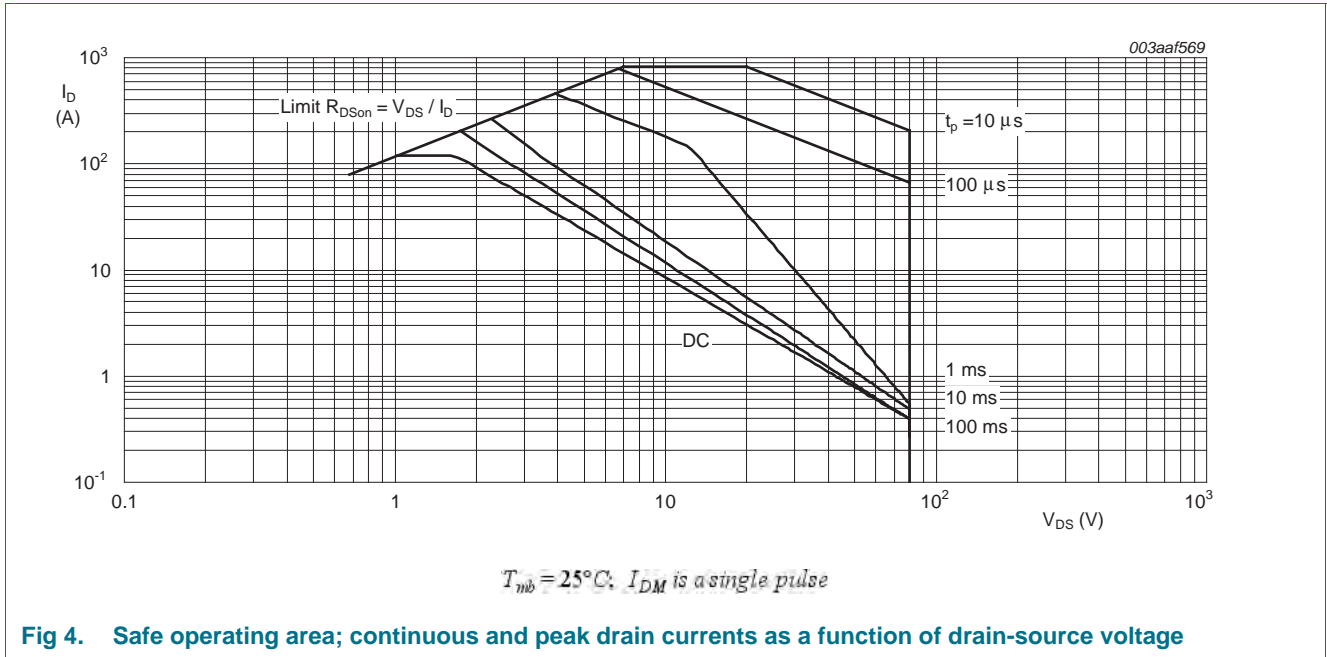


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.42	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

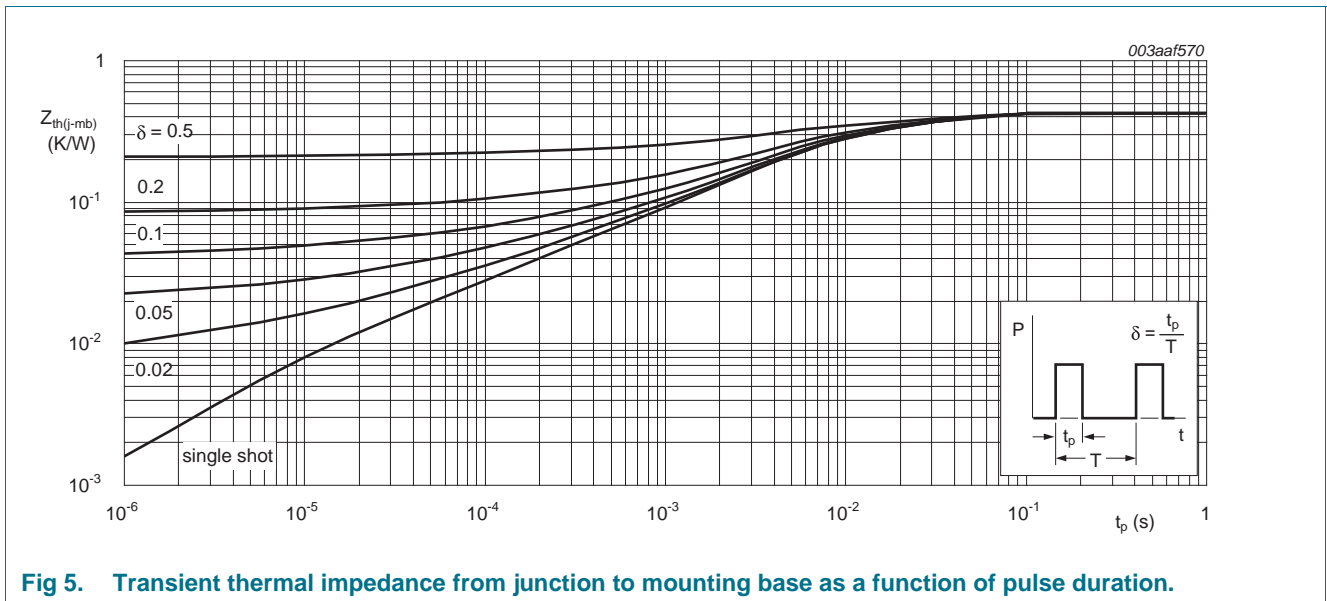


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \text{ mA}; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 9	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 9	-	-	4.5	V
I_{DSS}	drain leakage current	$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.15	2	μA
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 11	-	3.1	3.8	m Ω
		$V_{GS} = 10 V; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$; see Figure 12 ; see Figure 11	-	-	9.2	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 64 V; V_{GS} = 10 V$; see Figure 13 ; see Figure 14	-	169	-	nC
Q_{GS}	gate-source charge		-	37	-	nC
Q_{GD}	gate-drain charge		-	51	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz}$;	-	9020	12030	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$; see Figure 15	-	840	1010	pF
C_{rss}	reverse transfer capacitance		-	470	645	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60 V; R_L = 2.4 \text{ } \Omega; V_{GS} = 10 V$;	-	38	-	ns
t_r	rise time	$R_{G(ext)} = 5 \text{ } \Omega$	-	48	-	ns
$t_{d(off)}$	turn-off delay time		-	129	-	ns
t_f	fall time		-	65	-	ns
L_D	internal drain inductance	from upper edge of mounting base to centre of die	-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; $T_j = 25 \text{ }^\circ C$	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$; see Figure 16	-	0.77	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 V$;	-	58	-	ns
Q_r	recovered charge	$V_{DS} = 25 V$	-	121	-	nC

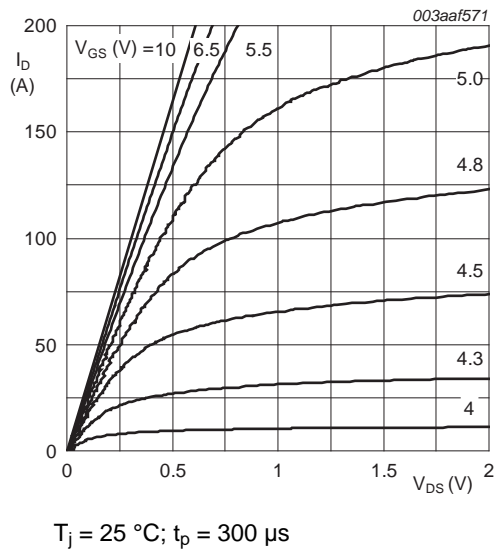


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

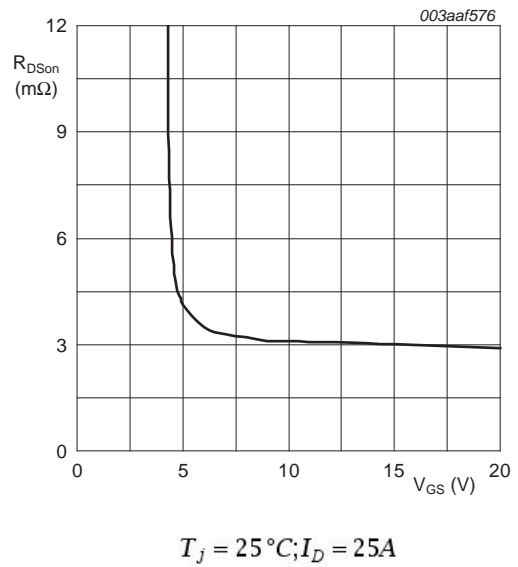


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

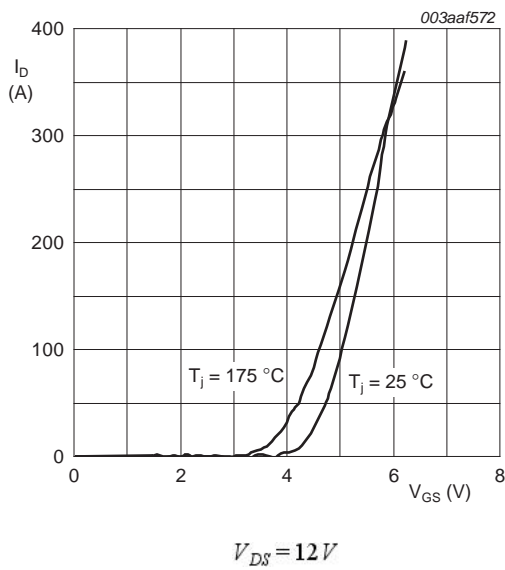


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

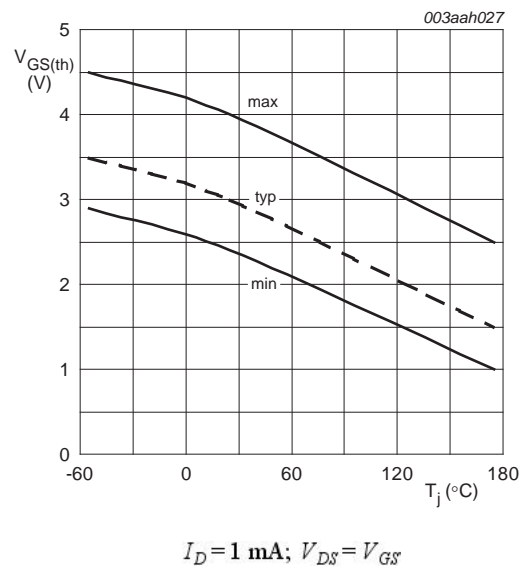


Fig 9. Gate-source threshold voltage as a function of junction temperature

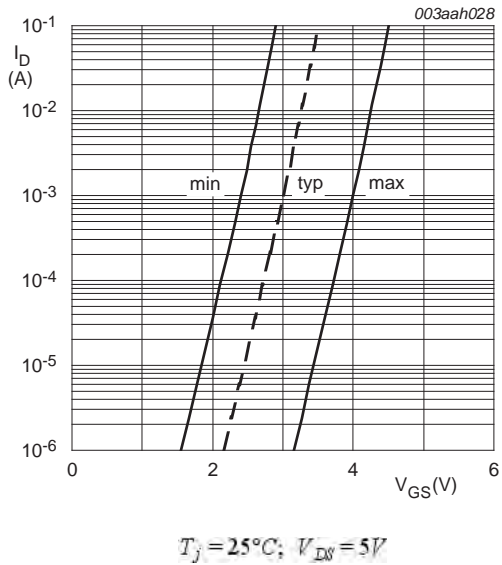


Fig 10. Sub-threshold drain current as a function of gate-source voltage

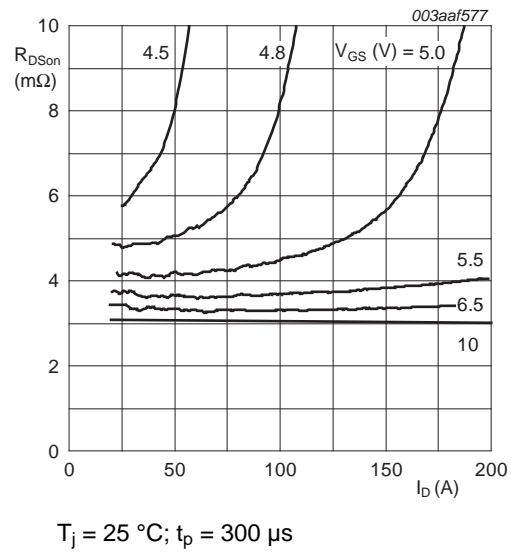


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

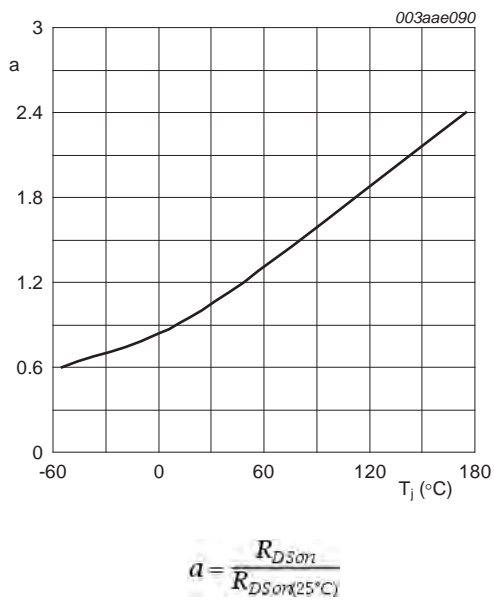


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

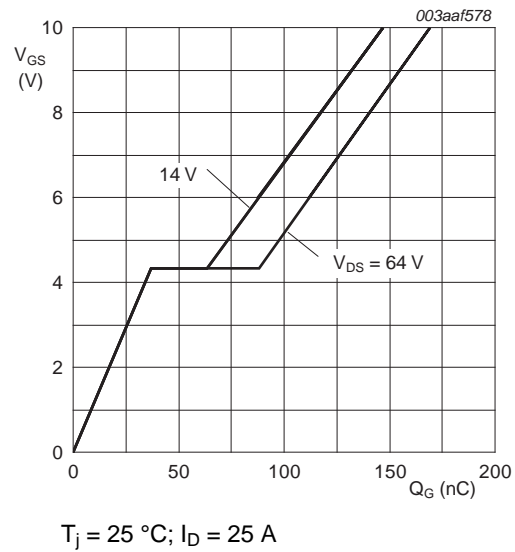


Fig 13. Gate-source voltage as a function of gate charge; typical values

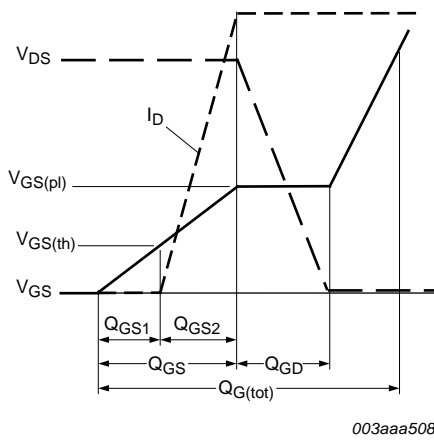


Fig 14. Gate charge waveform definitions

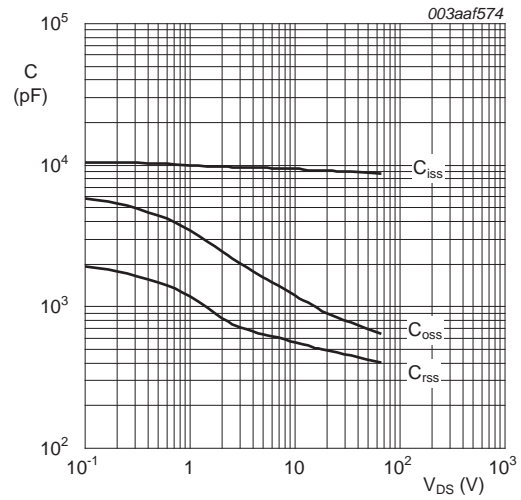
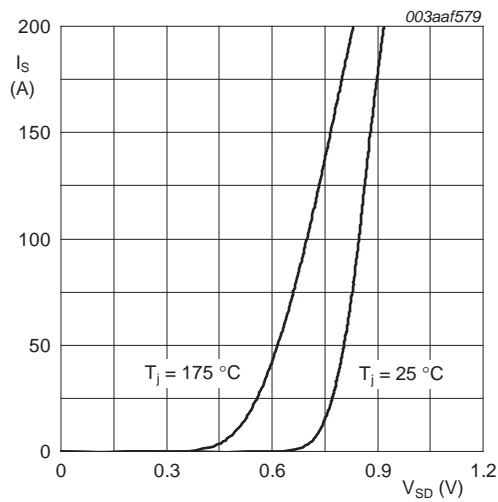


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values
 $V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



$V_{GS} = 0 \text{ V}$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



Fig 17. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK763R8-80E v.2	20120516	Product data sheet	-	BUK763R8-80E v.1
Modifications:	<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.			
BUK763R8-80E v.1	20120404	Objective data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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12. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	3
6	Thermal characteristics	5
7	Characteristics	6
8	Package outline	10
9	Revision history	11
10	Legal information	12
10.1	Data sheet status	12
10.2	Definitions	12
10.3	Disclaimers	12
10.4	Trademarks	13
11	Contact information	13

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