High Voltage Monolithic Inverter and Dual Boost

FEATURES

- **Ideal for CCD, LCD, LED Backlight and OLED Applications**
- **Easy Generation of 15V (50mA), –8V (100mA) and 20V (20mA) from a Li-Ion Cell**
- **V_{IN} Range: 2.5V to 6V**
- **Wide Output Ranges: Up to 32V for the Boosts and Up to –32V for the Inverter**
- Output Disconnect for the Boost Channels
- Boost3 Allows Voltage Programming and/or Current Programming for a 'One Wire Current Source'
- Overload Fault Protection with Fault I/O Pin Indicator
- Combined Soft-Start and Enable Pins
- Small 20-Pin 3mm × 3mm QFN Package

APPLICATIONS

- Digital Still and Video Cameras
- Scanner and Display Systems
- PDA, Cellular Phones and Handheld Computers
- LED Backlight and OLED Display Drivers
- CCD Imager Bias
- General High Voltage Supply Bias

DESCRIPTION

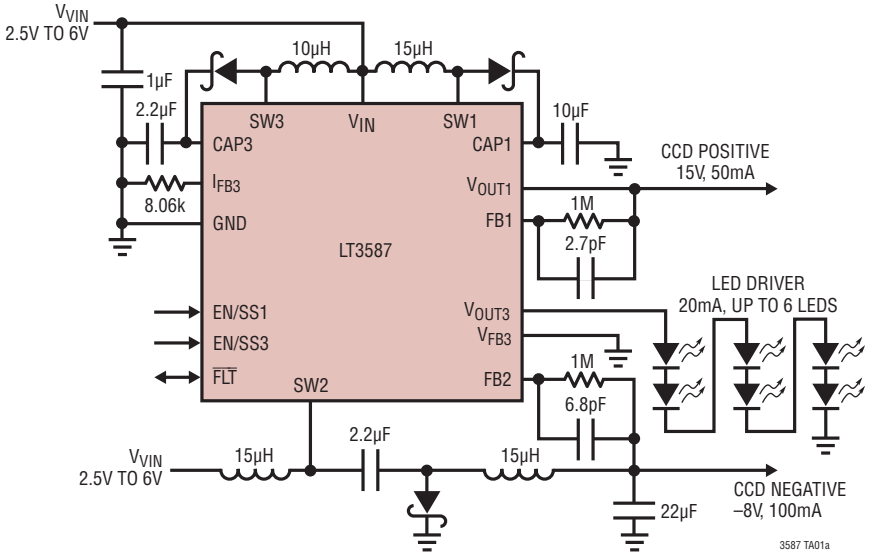
The LT®3587 provides a one chip solution for applications requiring two positive and one negative high voltage supplies. The LT3587 input voltage range of 2.5V to 6V makes it ideal for various battery-powered systems.

A single resistor programs each of the three output voltage levels and the output current of Boost3. The intelligent soft-start allows for sequential soft-start of the Boost1 output followed by the negative output with a single capacitor. Internal sequencing circuitry also disables the inverter until the Boost1 output has reached 87% of its final value.

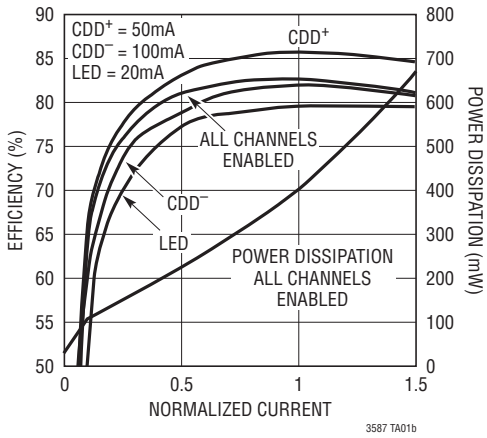
The LT3587 integrates all the power switches, soft-start, and output-disconnect circuits into a small 3mm × 3mm QFN package. This high level of integration combined with small external components makes the LT3587 ideal for space constrained applications.

TYPICAL APPLICATION

Li-Ion Powered Supply for CCD Imager and Six White Backlight LEDs



Efficiency Curve

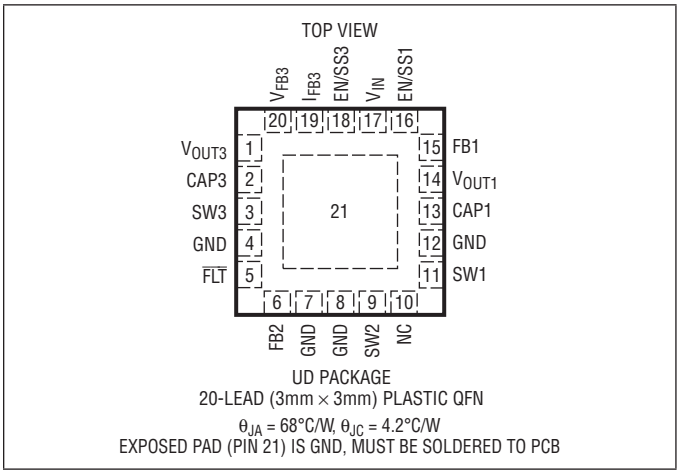


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 6V
Soft-Start Input Pins
EN/SS1, EN/SS3 .....6V
Feedback Pins
FB1, FB2, I_{FB3}, V_{FB3} ..... –0.2V to 6V
High Voltage Switch Pins
SW1, SW2, SW3.....40V
High Voltage Output Pins
CAP1, CAP3, V_{OUT1}, V_{OUT3} 32V
Bidirectional I/O Pin
$\overline{FLT}$ 6V
$\overline{FLT}$ Current 10mA
Operating Junction Temperature Range.. –40°C to 125°C
Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN
θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3587EUD#PBF	LT3587EUD#TRPBF	LDNC	20-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{VIN} = 3.6V, $V_{EN/SS1}$ = $V_{EN/SS3}$ = V_{VIN} unless otherwise noted (Note 2, 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage Range			2.5		6	V
Quiescent Current	$V_{EN/SS1}$ = 0V, $V_{EN/SS3}$ = V_{VIN} OR $V_{EN/SS1}$ = V_{VIN}, $V_{EN/SS3}$ = 0V OR $V_{EN/SS1}$ = $V_{EN/SS3}$ = V_{VIN} Not Switching			2.4	4	mA
	$V_{EN/SS1}$ = $V_{EN/SS3}$ = 0V, In Shutdown			5.5	9	µA
Switching Frequency		●	0.8	1	1.2	MHz
Maximum Duty Cycle		●	87	93		%
Minimum On Time				50	70	ns
Power Fault Delay from Any Output to $\overline{FLT}$				16		ms
$\overline{FLT}$ Input Threshold Low		●	0.4	1.0	1.6	V
$\overline{FLT}$ Leakage Current	$V_{\overline{FLT}}$ = 5V	●			±1	µA
$\overline{FLT}$ Voltage Output Low	$I_{\overline{FLT}}$ = 1mA	●			0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $V_{EN/SS1}$ = $V_{EN/SS3}$ = V_{IN} unless otherwise noted (Note 2, 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Boost1						
CAP1 Bias Current	V_{CAP1} = 15V, V_{OUT1} = Open			60	150	µA
FB1 Reference Voltage		●	1.19	1.22	1.25	V
V_{OUT1} Output Voltage	R_{FB1} = 1MΩ	●	14.25	15	15.75	V
SW1 Current Limit			800	990		mA
SW1 V_{CESAT}	I_{SW1} = 400mA			200		mV
SW1 Leakage Current	V_{SW1} = 15V			0.1	5	µA
EN/SS1 for Full Inductor Current	V_{FB1} = 1.1V, V_{FB2} = 0.1V				2.5	V
EN/SS1 Shutdown Voltage Threshold		●	0.2			V
EN/SS1 Pin Bias Current	$V_{EN/SS1}$ = 0V		–0.5	–1	–1.5	µA
V_{OUT1} Current Limit	V_{CAP1} = 15V		100	155		mA
CAP1 to V_{OUT1} On-Resistance (R_{DISC1})	V_{CAP1} = 15V, I_{VOUT1}= 50mA			5	8	Ω
V_{OUT1} Disconnect Leakage	V_{IN} = V_{CAP1} = 6V, V_{VOUT1} = 0V			0.1	1	µA
Inverter						
FB2 Reference Voltage		●	–10	5	20	mV
Output Voltage	R_{FB2} = 1MΩ	●	–7.5	–8	–8.5	V
SW2 Current Limit			900	1090		mA
SW2 V_{CESAT}	I_{SW2} = 600mA			250		mV
SW2 Leakage Current	V_{SW2} = 15V			0.1	5	µA
FB1 Threshold to Start Negative Channel	Percent of Final Regulation Value			87	90	%
Boost3						
CAP3 Bias Current	V_{CAP3} = 15V, V_{OUT3} = Open			70	150	µA
Boost3 Programmed Current	R_{IFB3} = 8.06kΩ	●	18	20	22	mA
V_{FB3} Reference Voltage	R_{VFB3} = 1MΩ, I_{VOUT3} = 20mA	●	0.77	0.8	0.83	V
V_{OUT3} Output Voltage	R_{VFB3} = 1MΩ, I_{VOUT3} = 20mA	●	14	15	16	V
SW3 Current Limit			400	480		mA
SW3 V_{CESAT}	I_{SW3} = 200mA			250		mV
SW3 Leakage Current	V_{SW3} = 15V			0.1	5	µA
EN/SS3 for Full Inductor Current	V_{VFB3} = V_{IFB3} = 0.6V				2	V
EN/SS3 Shutdown Voltage Threshold		●	0.2			V
EN/SS3 Pin Bias Current	$V_{EN/SS3}$ = 0V		–0.5	–1	–1.5	µA
V_{OUT3} Current Limit	V_{CAP3} = 15V, V_{IFB3} = 0V		70	110		mA
CAP3 to V_{OUT3} On Resistance (R_{DISC3})	V_{CAP3} = 15V, I_{VOUT3} = 20mA			10	15	Ω
V_{OUT3} Disconnect Leakage	V_{IN} = V_{CAP3} = 6V, V_{VOUT3} = 0V			0.1	1	µA
CAP3 Pin Overvoltage Clamp			27	29	31	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

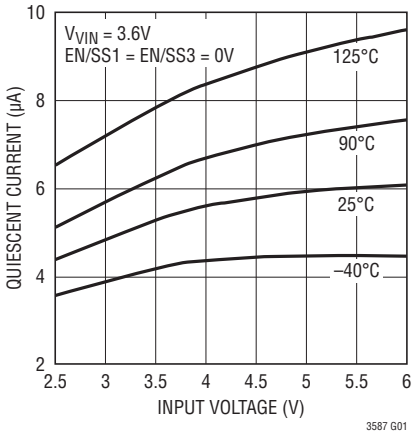
Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3: The LT3587 is guaranteed to meet specified performance from 0°C to 125°C. Specifications over the –40°C to 125°C operating range are assured by design, characterization and correlation with statistical process controls.

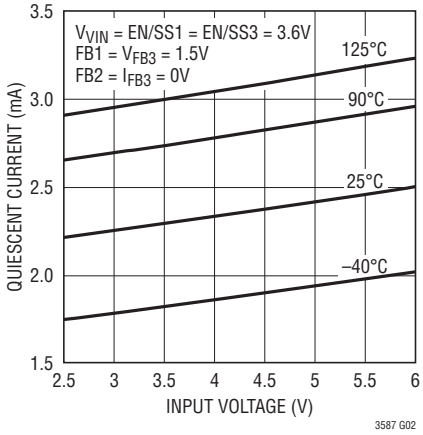
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

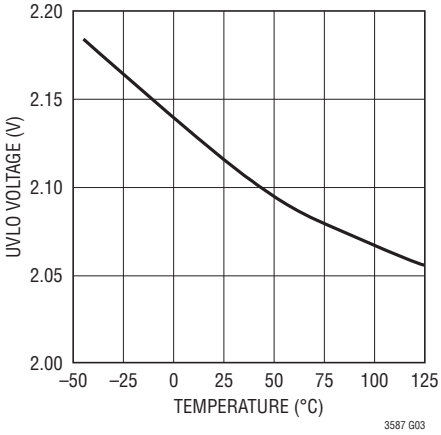
Shutdown Quiescent Current vs Input Supply Voltage



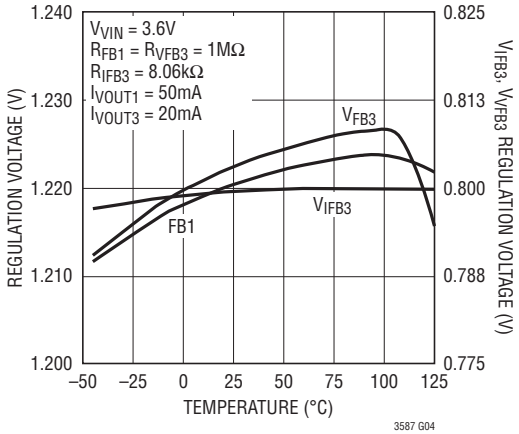
Quiescent Current When On But Not Switching vs Input Supply Voltage



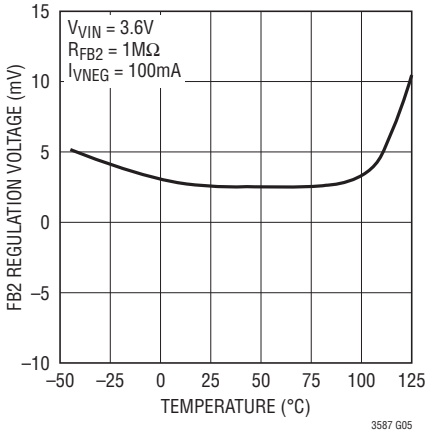
V_{IN} UVLO Voltage vs Temperature



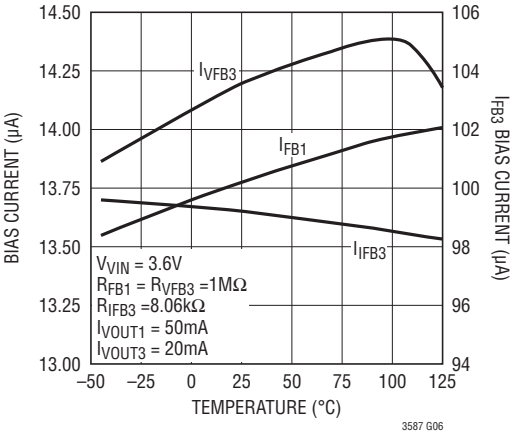
FB1, V_{FB3} and I_{FB3} Regulation Voltage vs Temperature



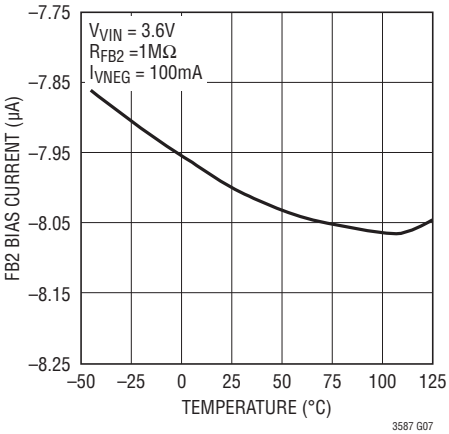
FB2 Regulation Voltage vs Temperature



FB1, V_{FB3}, I_{FB3} Bias Current in Regulation vs Temperature



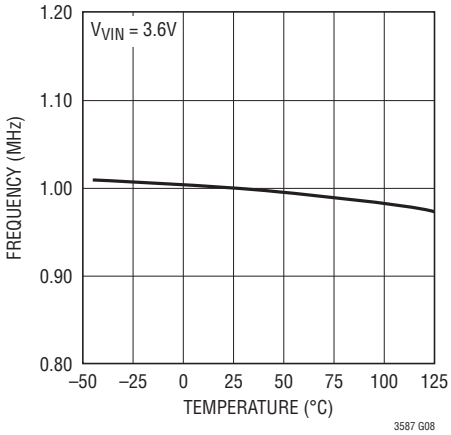
FB2 Bias Current in Regulation vs Temperature



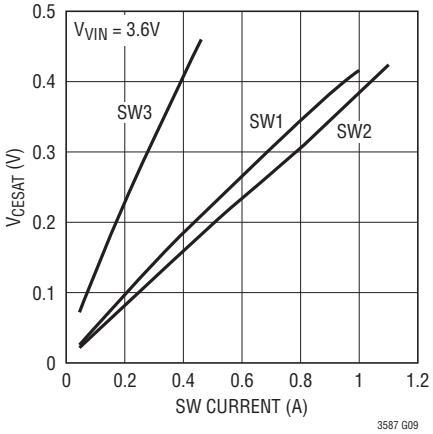
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

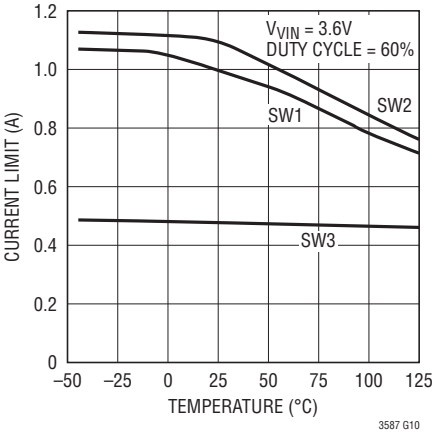
Switching Frequency vs Temperature



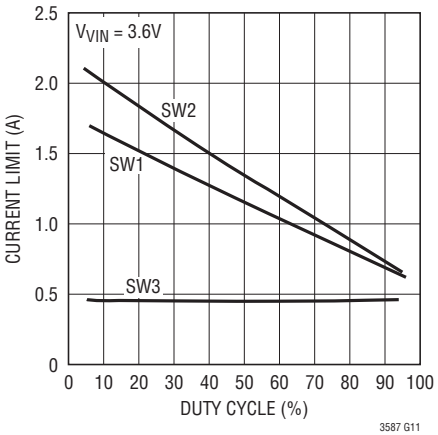
Switches V_{CESAT} vs Current



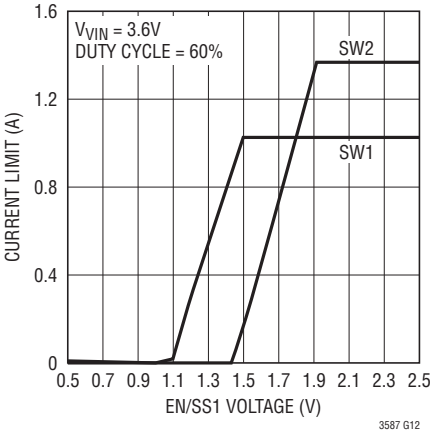
Switches Current Limit vs Temperature



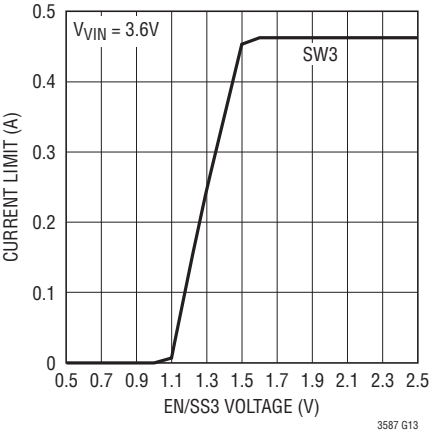
Switches Current Limit vs Duty Cycle



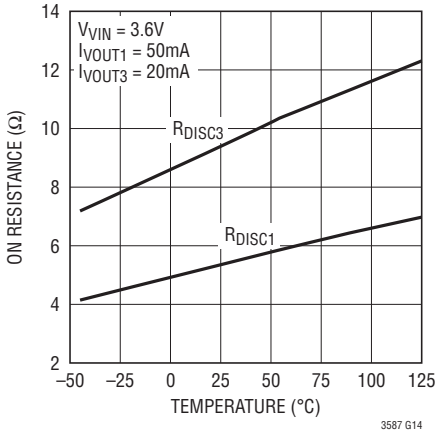
SW1 and SW2 Current Limit vs EN/SS1 Voltage



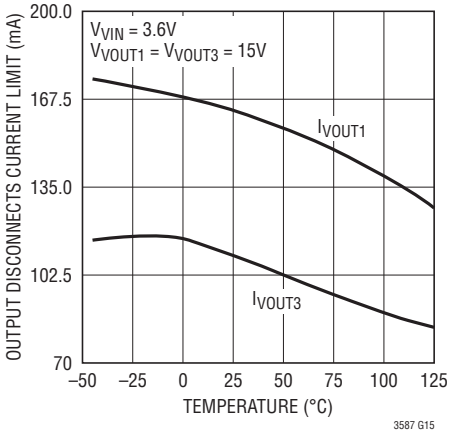
SW3 Current Limit vs EN/SS3 Voltage



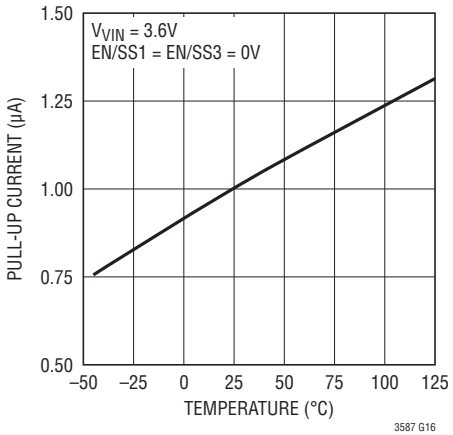
Output Disconnects On Resistance vs Temperature (R_{DISC1}, R_{DISC3})



Output Disconnects Current Limit vs Temperature



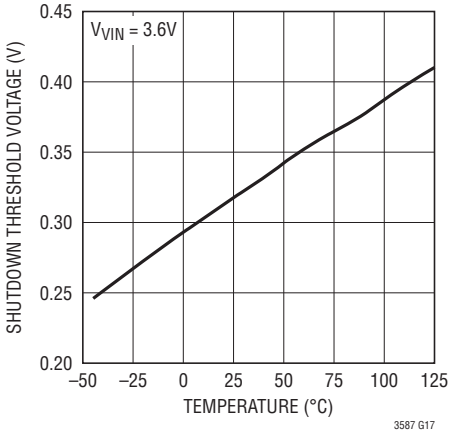
EN/SS1, EN/SS3 Pull-Up Current In Shutdown vs Temperature



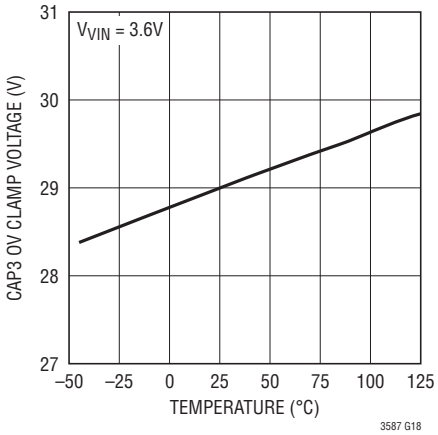
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

EN/SS1, EN/SS3 Shutdown Threshold vs Temperature



CAP3 Overvoltage Clamp vs Temperature



PIN FUNCTIONS

V_{OUT3} (Pin 1): Boost3 Output Pin. This pin is the drain of an output disconnect PMOS transistor.

CAP3 (Pin 2): Boost3 Output Capacitor Pin. This pin is the source of an output PMOS disconnect. Connect a capacitor from this pin to ground.

SW3 (Pin 3): Boost3 Switch Pin. Connect an inductor from this pin to V_{IN}. Minimize trace area at this pin to minimize EMI.

GND (Pin 4, 7, 8, 12): Ground Pins.

$\overline{FLT}$ (Pin 5): Fault Pin. This pin is a bidirectional open-drain pull-down pin. This pin pulls low when any of the enabled outputs fall out of regulation for more than 16ms. Each output is ignored during start-up until its respective enable/soft-start pin allows for full inductor current. This pin can also be externally forced low to disable all the supply outputs. Once this pin goes low (either due to an out of regulation condition or externally forced low), the pin latches low until the inputs to EN/SS1 and EN/SS3 are set low or the input supply pin is recycled. Pull up this pin to V_{IN} with a 200k resistor when not used.

FB2 (Pin 6): Inverter Output Voltage Feedback Pin. Connect a resistor R_{FB2} from this pin to the Inverter Output (V_{NEG}) such that:

$$R_{FB2} = |V_{NEG}|/8\mu A$$

Note that FB2 pin voltage is about 0V when in regulation. There is an internal 153k resistor from the FB2 pin to the internal reference.

SW2 (Pin 9): Inverter Switch Pin. Connect an inductor between this pin and V_{IN}, as well as the flying capacitor from this pin to the anode of the Inverter ground return diode. Minimize trace area at this pin to minimize EMI.

NC (Pin 10): No Connect Pin. Leave open or connect to ground.

SW1 (Pin 11): Boost1 Switch Pin. Connect an inductor from this pin to V_{IN}. Minimize trace area at this pin to minimize EMI.

CAP1 (Pin 13): Boost1 Output Capacitor Pin. This pin is the source of an output PMOS disconnect. Connect a capacitor from this pin to ground.

PIN FUNCTIONS

V_{OUT1} (Pin 14): Boost1 Output Pin. This pin is the drain of an output disconnect PMOS transistor.

FB1 (Pin 15): Boost1 Output Voltage Feedback Pin. Connect a resistor R_{FB1} from this pin to V_{OUT1} (or CAP1) such that:

$$R_{FB1} = ((V_{VOUT1}/1.22V) – 1) • 88.5k$$

There is an internal 88.5k resistor from the FB1 pin to ground.

EN/SS1 (Pin 16): Boost1/Inverter Shutdown and Soft-Start Pin. Boost1 and Inverter are enabled when the voltage on this pin is greater than 2.5V. They are disabled when the voltage is below 0.2V. An internal 1µA current source in conjunction with an external capacitor can be used to ramp this pin and provide soft-start.

V_{IN} (Pin 17): Input Supply Pin. Must be locally bypassed with an X5R or X7R type ceramic capacitor.

EN/SS3 (Pin 18): Boost3 Shutdown and Soft-Start Pin. Boost3 is enabled when the voltage on this pin is greater than 2V. It is disabled when the voltage is below 0.2V. An internal 1µA current source in conjunction with an external capacitor can be used to ramp this pin and provide soft-start.

I_{FB3} (Pin 19): Boost3 Output Current Programming Pin. Connect a resistor R_{IFB3} from this pin to ground such that:

$$R_{IFB3} = 200 • (0.8V/I_{VOUT3})$$

If Boost3 output is configured as a voltage regulator, R_{IFB3} can be optionally used to limit the maximum output current to I_{LIMIT}:

$$R_{IFB3} = 200 • (0.8V/I_{LIMIT})$$

Note: Tie I_{FB3} to GND when no current limit is desired.

V_{FB3} (Pin 20): Boost3 Output Voltage Feedback Pin. Connect a resistor R_{VFB3} from this pin to V_{OUT3} (or CAP3) such that:

$$R_{VFB3} = ((V_{VOUT3}/0.8V) – 1) • 56.3k$$

There is an internal 56.3k resistor from the V_{FB3} pin to ground. In the current regulator configuration, R_{VFB3} can be optionally used to limit the maximum output voltage to V_{CLAMP}, such that:

$$R_{VFB3} = ((V_{CLAMP}/0.8V) – 1) • 56.3k$$

Note: When no voltage clamp is desired in the current regulator configuration, tie V_{FB3} to GND.

Exposed Pad (Pin 21): Ground Pin. Connect to PCB ground plane. Ground plane connection through multiple vias under the package is recommended for optimum electrical and thermal performance.

BLOCK DIAGRAM

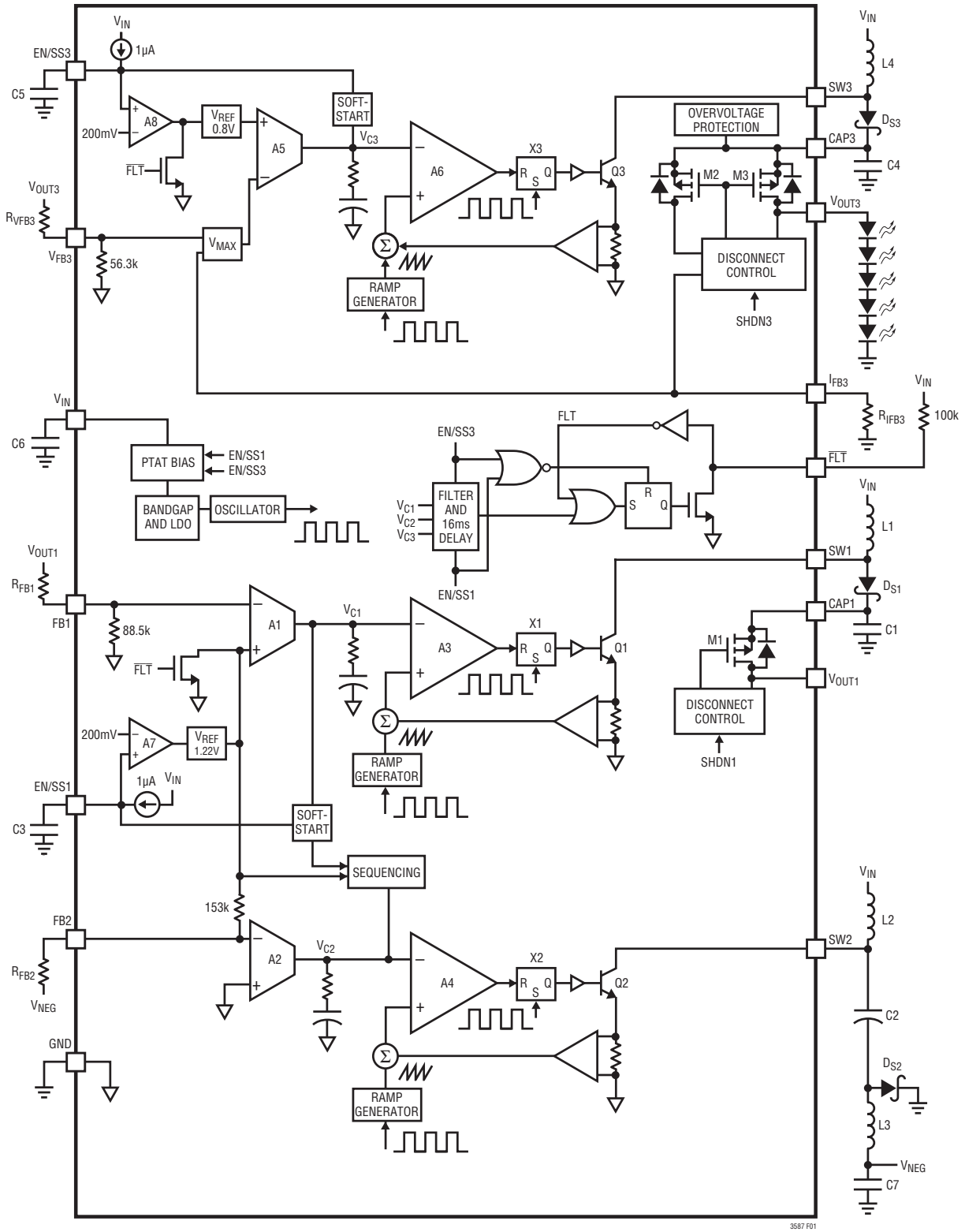


Figure 1. Block Diagram

OPERATION

All three channels of the LT3587 use a constant frequency, current mode control scheme to provide voltage and/or current regulation at the output. Operation can be best understood by referring to the Block Diagram in Figure 1.

If EN/SS1 is pulled higher than 200mV, the bandgap reference, the start-up bias and the oscillator are turned on. At the start of each oscillator cycle, the SR latch X1 is set, which turns on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When this voltage exceeds the level at the negative input of A3, the SR latch X1 is reset, turning off the power switch Q1. The level at the negative input of A3 is set by the error amplifier A1, which is simply an amplified version of the difference between the reference voltage of 1.22V and the feedback voltage. In this manner, the error amplifier sets the correct peak switch current level to keep the output voltage in regulation. If the error amplifier output increases, more current is delivered to the output; if it decreases, less current is delivered.

The second channel is an inverting converter. This channel is also enabled through the EN/SS1 pin. The basic operation of this second channel is the same as the positive channel. The SR latch X2 is also set at the start of each oscillator cycle. The power switch Q2 is turned on at the same time as Q1. Q2 turns off based on its own feedback loop, which consists of error amplifier A2 and PWM comparator A4. The reference voltage of this negative channel is ground.

Voltage clamps (not shown) on the output of the error amplifiers A1 and A2 enforce current limit on Q1 and Q2 respectively.

Similar to the first channel, the third channel is also a positive boost regulator. If EN/SS3 is pulled higher than 200mV, the bandgap reference, the start-up bias and the oscillators are also turned on. The SR latch X3 is set at the start of each oscillator cycle which turns on the power switch Q3. Q3 turns off based on its own feedback loop, which consists of error amplifier A5 and PWM comparator A6. The level at the negative input of A6 is set by the error amplifier A5, and is an amplified version of the difference between the reference voltage of 0.8V and the maximum of the two feedback voltages at V_{FB3} and I_{FB3}. A separate comparator (not shown) sets the maximum current limit on Q3.

The I_{FB3} pin is pulled up internally with a current that is (1/200) times the load current out of the V_{OUT3} pin. Therefore, an external resistor connected from this pin to ground generates a feedback voltage proportional to the V_{OUT3} output load current at the I_{FB3} pin. When the voltage at V_{FB3} is higher than the voltage at I_{FB3}, the third channel regulates to the feedback voltage at V_{FB3}, which in normal application is a divided down voltage from V_{OUT3}. In this state, the third channel behaves as a boost voltage regulator. On the other hand if the voltage at I_{FB3} is higher, the third channel regulates to the feedback voltage at I_{FB3}, which therefore regulates the V_{OUT3} output load current to a particular value. In this state, the third channel behaves as a boost current regulator.

PMOS M1 is used as an output disconnect pass transistor for the first channel. M1 disconnects the load (V_{OUT1}) from the input as long as the voltage between CAP1 and V_{IN} is less than 2.5V (typical) and the voltage between CAP1 and V_{OUT1} is less than 10V (typ). Similarly, PMOS M3 is used as an output disconnect pass transistor for the third channel. M3 disconnects the load (V_{OUT3}) from the input when the third channel is in shutdown (EN/SS3 voltage is lower than 200mV) and the voltage between CAP3 and V_{OUT3} is less than 10V (typical).

APPLICATIONS INFORMATION

Inductor Selection

A 15µH inductor and a 10µH inductor are recommended for the LT3587 Boost1 channel and Boost3 channel respectively. The inverting channel can use 15µH or 22µH inductors. Although small size is the major concern for most applications, for high efficiency the inductors should have low core losses at 1MHz and low DCR (copper wire resistance). The inductor DCR should be on the order of half of the switch on resistance for its channel: 0.5Ω for Boost1, 0.4Ω for the inverter and 1Ω for Boost3. For robust applications, the inductors should have current ratings corresponding to their respective peak current during regulation. Furthermore, with no soft-start, the inductor should also be able to withstand temporary high start-up currents of 1A, 1.1A and 480mA for the Boost1, inverter and Boost3 channels respectively (typ, refer to the Typical Performance Characteristics curves).

Capacitor Selection

The small size of ceramic capacitors makes them suitable for LT3587 applications. X5R and X7R types of ceramic capacitors are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 1µF input capacitor is sufficient for most LT3587 applications. The output capacitors required for stability depend on the application. For most applications, the output capacitor values required are: 10µF for the Boost1 channel, 22µF for the inverter channel and 2.2µF for the Boost3 channel. The inverter requires a 2.2µF flying capacitor. Note that this flying capacitor needs a voltage rating of at least $V_{IN} + |V_{NEG}|$.

Inrush Current

When a supply voltage is abruptly applied to the V_{IN} pin, the voltage difference between the V_{IN} pin and the CAP pins generates inrush current. For the case of the Boost1 channel, the inrush current flows from the input through the inductor L1 and the Schottky D_{S1} to charge the Boost1 output capacitor C1. Similarly for the Boost3 channel, the inrush current flows from the input through the inductor L4 and the Schottky D_{S3} to charge the output capacitor C4.

For the inverting channel, the inrush current flows from the input through inductor L2, charging the flying capacitor C2 and returning through the Schottky diode D_{S2}.

The selection of inductor and capacitor values should ensure that the peak inrush current is below the rated momentary maximum current of the Schottky diodes. The peak inrush current can be estimated as follows:

$$I_P = \frac{(V_{VIN} - 0.6) \bullet e^{\frac{-1}{\varphi}\tan^{-1}(\varphi)}}{\sqrt{\frac{L}{C}}}$$

$$\varphi = \sqrt{\frac{4L}{R^2C} - 1}$$

where L is the inductance, C is the capacitance and R is the total series resistance in the inrush current path, which includes the resistance of the inductor and the Schottky diode. Note that in this equation, we model the Schottky as having a fixed 0.6V drop.

Table 1 gives inrush peak currents for some component selections. Note that inrush current is not a concern if the input voltage rises slowly.

Table 1. Inrush Peak Current

V_{VIN} (V)	R (Ω)	L (µH)	C (µF)	I_P (A)
5	0.68	15	10	2.48
5	0.68	22	2.2	1.19
5	0.68	10	2.2	1.64
3.6	0.745	15	10	1.64
3.6	0.745	22	2.2	0.80
3.6	0.745	10	2.2	1.10

Schottky Diode Selection

For any of the external diode (D_{S1}, D_{S2} and D_{S3}) selections, besides having sufficiently high reverse breakdown voltage to withstand the output voltage, both forward voltage drop and diode capacitance need to be considered. Schottky diodes rated for higher current usually have lower forward voltage drops and larger capacitance. Although lower forward voltage drop is good for efficiency, a large

APPLICATIONS INFORMATION

capacitance will slow down the switching waveform, which can cause significant switching losses at 1MHz switching frequency. Some recommended Schottky diodes are listed in Table 2.

Table 2. Recommended Schottky Diodes

PART NUMBER	FORWARD CURRENT (mA)	FORWARD VOLTAGE DROP (V)	DIODE CAPACITANCE (pF at 10V)	MANUFACTURER
RSX051VA-30	1000	0.35	30	ROHM www.rohm.com
PMEG4010CEJ	500	0.49	25	NXP/Phillips www.nxp.com
PMEG2005EB	500	0.43	8	
IR05H40CSPTR	500	0.48	39	Vishay www.vishay.com
B0540WS	500	0.48	20	Diodes Inc. www.diodes.com
ZLLS400	520	0.53	17	Zetex www.zetex.com

Smaller Footprint Inverter Topology

In certain applications with higher tolerance of current ripple at the output of the inverter, the inductor L3 can be replaced with a Schottky diode. Since the Schottky diode footprint is usually smaller than the inductor footprint, this alternate topology is recommended if a smaller overall solution is a must. Note that this topology is only viable if the absolute value of the inverter output is greater than V_{IN}.

This Schottky diode is configured with the anode connected to the output of the inverter and the cathode to the output end of the flying capacitor C2 as shown in Figure 2.

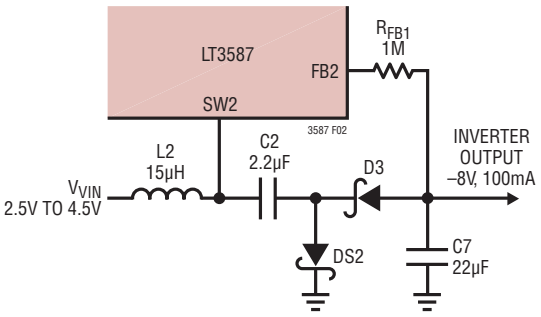


Figure 2. Inverter Configured with a Schottky Diode in Place of the Output Inductor

The same constraints as the other Schottky diodes apply for selecting D3. Therefore, the same recommended Schottky diodes in Table 2 can be used for D3.

Boost3 Overcurrent and Overvoltage Protection

As briefly discussed in the Operation section, the regulation loop of Boost3 uses the maximum of the two voltages at V_{FB3} and I_{FB3} as feedback information to set the peak current of its power switch Q3. This allows for the Boost3 loop to be configured as either a boost voltage regulator or a boost current regulator (Figure 3). Furthermore, this architecture also allows for a programmable current limit on voltage regulation or voltage limit on current regulation.

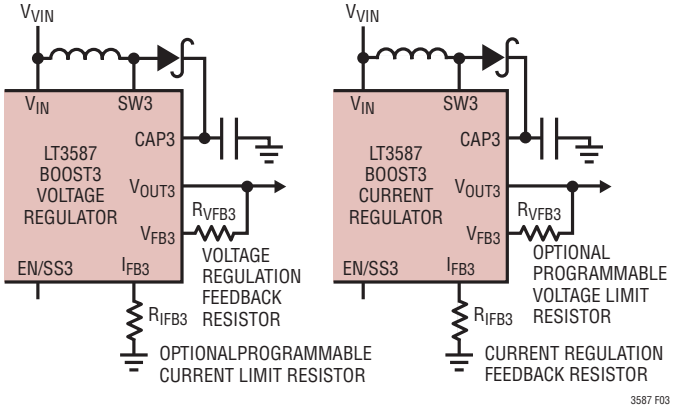


Figure 3. Boost3 Configured as a Voltage Regulator and as a Current Regulator

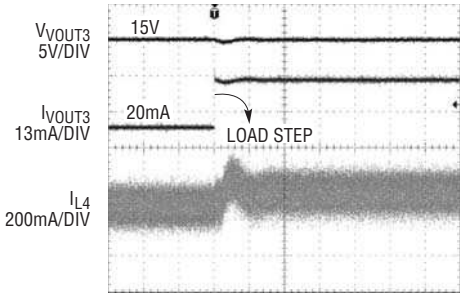
When configured as a boost voltage regulator, a feedback resistor from the output pin V_{OUT3} to the V_{FB3} pin sets the voltage level at V_{OUT3} at a fixed level. In this case, the I_{FB3} pin can either be grounded if no current limiting is desired or connected to ground with a resistor such that:

$$I_{LIMIT} = 200 \bullet (0.8V/R_{IFB3})$$

where I_{LIMIT} is the desired output current limit value. Recall that the pull-up current on the I_{FB3} pin is controlled to be typically 1/200 of the output load current at the V_{OUT3} pin. In this case, when the load current is less than I_{LIMIT}, the Boost3 loop regulates the voltage at the V_{FB3} pin to 0.8V. When there is an increase in load current beyond I_{LIMIT}, the voltage at V_{FB3} starts to drop and the voltage at I_{FB3} rises above 0.8V. The Boost3 loop then regulates the voltage at the I_{FB3} pin to 0.8V, limiting the output

APPLICATIONS INFORMATION

current at V_{OUT3} to I_{LIMIT}. Figure 4 compares the transient responses with and without current limit when a current overload occurs.



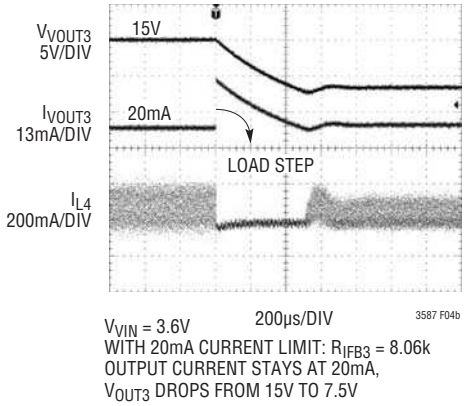


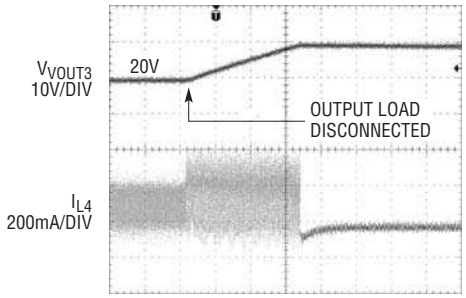
Figure 4. Boost3 Waveform in an Output Current Overload Event with and Without Output Current Limit

The LT3587 CAP3 pin has an internal overvoltage protection. When the voltage at the CAP3 pin is driven above 29V (typ), the Boost3 loop is disabled and the SW3 pin stops switching.

When configured as a boost current regulator, a feedback resistor from the I_{FB3} pin to ground sets the output current at V_{OUT3} at a fixed level. In this case, if the V_{FB3} pin is grounded then the overvoltage protection defaults to the open-circuit clamp voltage level of 29V. A voltage clamp lower than 29V is obtained by connecting a resistor from the V_{OUT3} pin to the V_{FB3} pin such that:

$$R_{FB3} = ((V_{CLAMP}/0.8V) - 1) \bullet 56.3k$$

where V_{CLAMP} is the desired output voltage clamp level. In this case, when the voltage level is less than V_{CLAMP}, the Boost3 loop regulates the voltage at the I_{FB3} pin to 0.8V. When the output load fails open-circuit or is disconnected, the voltage at I_{FB3} drops to reflect the lower output current and the voltage at V_{FB3} starts to rise. When the voltage at V_{OUT3} rises to V_{CLAMP}, the Boost3 loop then regulates the voltage at the V_{FB3} pin to 0.8V, limiting the voltage level at V_{OUT3} to V_{CLAMP}. Figure 5 contrasts the transient responses with and without programmed V_{CLAMP} when the output load is disconnected.



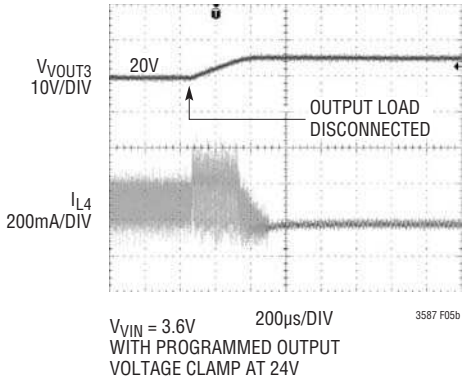


Figure 5. Boost3 Output Open-Circuit Waveform with and Without Programmed Output Voltage Clamp

APPLICATIONS INFORMATION

Setting The Output Voltages and The Boost3 Output Current

The LT3587 has a trimmed internal feedback resistor. A 1M feedback resistor from each output pin to its corresponding feedback pin sets the outputs to 15V for Boost1, –8V for the inverter and 15V for Boost3. Note that only one resistor is needed to set the output voltage for each channel. Set the output voltages according to the following formulas:

$$R_{FB1} = ((V_{VOUT1}/1.22V) – 1) • 88.5k$$

$$R_{FB2} = |V_{NEG}|/8\mu A$$

$$R_{VFB3} = ((V_{VOUT3}/0.8V) – 1) • 56.3k$$

As described in previous sections, Boost3 can be configured as a boost current regulator. When configured as such, set the output current according to the following formula:

$$R_{IFB3} = 200 • (0.8V/I_{VOUT3})$$

In order to maintain accuracy, use high precision resistors when setting any of the channels output voltage and/or the Boost3 output current (1% is recommended).

Soft-Start

The LT3587 has two soft-start control pins: EN/SS1 and EN/SS3. The EN/SS1 pin controls the soft-start for both the Boost1 and the inverter, while the EN/SS3 pin controls the soft-start for the Boost3. Each of these soft-start pins is pulled up internally with a 1µA current source.

Connecting a capacitor from the EN/SS1 pin to ground programs a soft-start ramp for the Boost1 and the inverter channels. Use an open-drain transistor to pull this pin low to shut down both the Boost1 and the inverter. Turning off this transistor allows the 1µA pull-up current to charge the soft-start capacitor. When the voltage at the EN/SS1 pins goes above 200mV, the regulation loops for Boost1 and the inverter are enabled. The V_{C1} node voltage follows the EN/SS1 voltage as it continues to ramp up to ensure slow start-up on the Boost1 channel. The V_{C2} node follows the ramp voltage minus 0.7V. This ensures that the inverter starts up after the Boost1, but still has a slow ramping output to avoid large start-up currents. The Boost1 and the inverter regulation loops are free running with full inductor current when the voltage at the EN/SS1 pin is above 2.5V.

Connecting a capacitor from the EN/SS3 pin to ground sets up a soft-start ramp for the Boost3 channel. As the 1µA current charges up the capacitor, the Boost3 regulation loop is enabled when the EN/SS3 pin voltage goes above 200mV. The V_{C3} node voltage follows the EN/SS3 voltage as it ramps up ensuring slow start-up on the Boost3 channel. When the voltage at the EN/SS3 pin is above 2V, the Boost3 regulation loop is free running with full inductor current.

Start Sequencing

The LT3587 also has internal sequencing circuitry that inhibits the inverter channel from operating until the feedback voltage of the Boost1 voltage (at the FB1 pin) reaches about 1.1V (87% of the final voltage). This ensures that the Boost1 output voltage is near regulation before any negative voltage is generated at the inverter output.

Figure 6 contrasts the start-up sequencing without any soft-start capacitor, and with a 10nF soft-start capacitor.

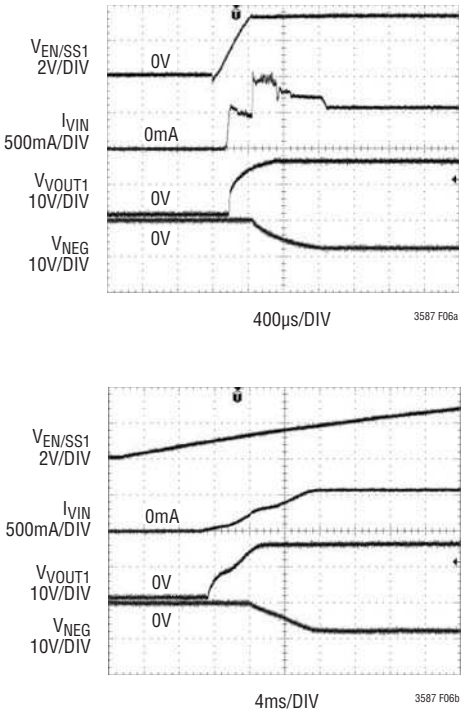


Figure 6. $V_{EN/SS1}$, V_{OUT1}, V_{NEG}, I_{VIN} with No Soft-Start Capacitor, and with a 10nF Soft-Start Capacitor

APPLICATIONS INFORMATION

Output Disconnect

Both the Boost1 and the Boost3 channels have an output disconnect between their respective CAP pin and V_{OUT} pin. This disconnect feature prevents a DC path from V_{IN} to V_{OUT}.

For Boost1, this output disconnect feature is implemented using a PMOS (M1) as shown in the Block Diagram in Figure 1. When turned on, M1 is driven hard in the linear region to reduce power dissipation when delivering current between the CAP1 pin and the V_{OUT1} pin. M1 stays on as long as the voltage difference between CAP1 and V_{IN} is greater than 2.5V. This allows for the positive bias to stay high for as long as possible as the negative bias discharges during turn off.

The disconnect transistor M1 is current limited to provide a maximum output current of 155mA (typ). However, there is also a protection circuit for M1 that limits the voltage drop across CAP1 and V_{OUT1} to about 10V. When the voltage at CAP1 is greater than 10V, in an overload or a short-circuit event, M1 current is limited to 155mA until the voltage across CAP1 to V_{OUT1} grows to about 10V. Then M1 is turned on hard without any current limit to allow for the voltage on CAP1 to discharge as fast as possible. When the voltage across CAP1 and V_{OUT1} reduces to less than 10V, the output current is then again limited to 155mA. Figure 7 shows the output voltage and current during an overload event with V_{CAP1} initially at 15V.

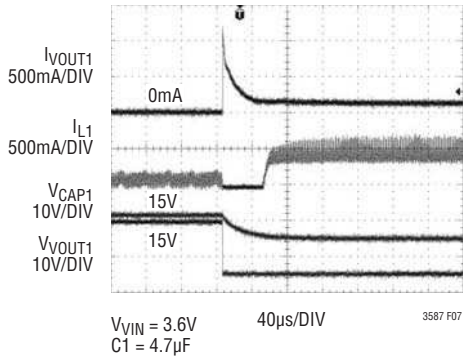


Figure 7. V_{CAP1}, V_{VOUT1}, I_{VOUT1} and I_{L1} During a Short-Circuit Event

The output disconnect feature on Boost3 is implemented similarly using M3. However, in this case M3 is only turned off when the EN/SS3 pin voltage is less than 200mV and the Boost3 regulation loop is disabled.

The disconnect transistor M3 is also current limited, providing a maximum output current at V_{OUT3} of 110mA (typ). M3 also has a similar protection circuit as M1 that limits the voltage drop across CAP3 and V_{OUT3} to about 10V. Figure 8 shows the output voltage and current during an overload event with V_{CAP3} initially at 24V.

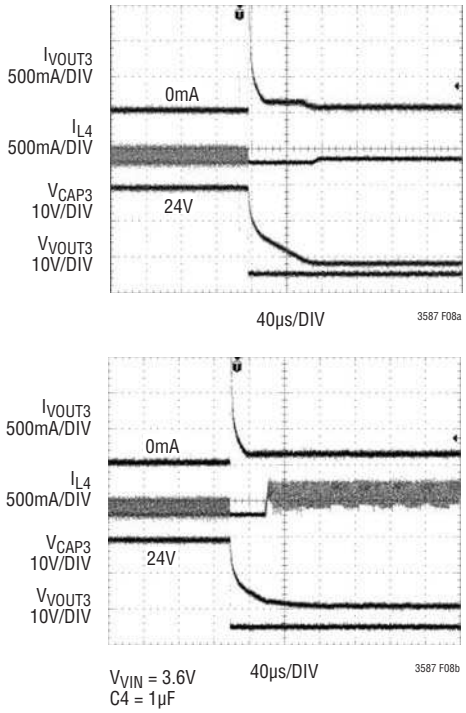


Figure 8. V_{CAP3}, V_{VOUT3}, I_{VOUT3} and I_{L4} During a Short-Circuit Condition with and Without Programmed 20mA Current Limit

Choosing A Feedback Node

Boost1 feedback resistor, R_{FB1}, may be connected to the V_{OUT1} pin or the CAP1 pin (see Figure 9). Similarly for Boost3 in a boost voltage regulator configuration, the feedback resistor, R_{VFB3}, may be connected to the V_{OUT3} pin or the CAP3 pin. Regulating the V_{OUT1} and V_{OUT3} pins eliminates the output offset resulting from the voltage drop across the output disconnect PMOS transistors.

APPLICATIONS INFORMATION

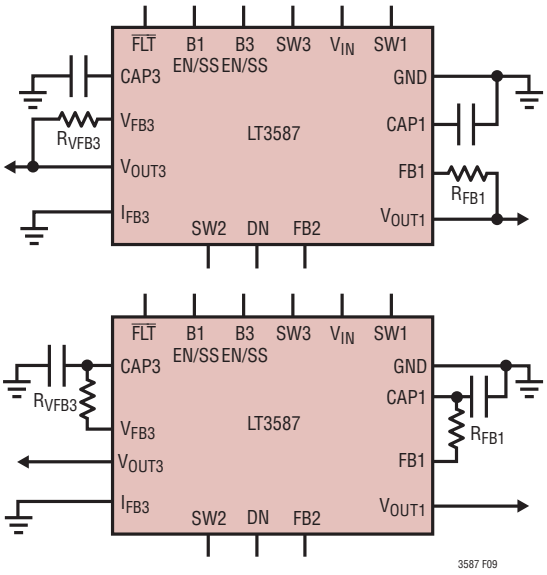


Figure 9. Feedback Connection Using the V_{OUT} and CAP Pins

However, in the case of a short-circuit fault at the V_{OUT} pins, the LT3587 will switch continuously because the FB1 or the V_{FB3} pin is low. While operating in this open-loop condition, the rising voltage at the CAP pins is limited only by the protection circuit of their respective output disconnects. At the worst case, the CAP pin rises to 10V above the corresponding V_{OUT} pin. So in the case of short-circuit fault to ground, the voltage on the CAP pins may reach 10V. When the short-circuit condition is removed, the V_{OUT} pins rise up to the voltage on the CAP pins, potentially exceeding the programmed output voltage until the capacitor voltages fall back into regulation. While this is harmless to the LT3587, this should be considered in the context of the external circuitry if short-circuit events are expected.

Regulating the CAP pins ensures that the voltage on the V_{OUT} pins never exceeds the set output voltage after a short-circuit event. However, this setup does not compensate for the voltage drop across the output disconnect, resulting in an output voltage that is slightly lower than the voltage set by the feedback resistor. This voltage drop is equal to the product of the output current and the on resistance of the PMOS disconnect transistor. This drop can be accounted for when using the CAP pin as the feedback node by setting the output voltage according to the following formula:

$$R_{FB1} = \frac{V_{VOUT1} + I_{VOUT1} \bullet R_{DISC1} - 1.22V}{13.8\mu A}$$

$$R_{FB3} = \frac{V_{VOUT3} + I_{VOUT3} \bullet R_{DISC3} - 0.8V}{14.3\mu A}$$

Fault Detection and Indicator

The LT3587 features fault detection on all its outputs and a fault indicator pin ($\overline{FLT}$). The fault detection circuitry is enabled only when at least one of the channels has completed the soft-start process and is free running with full inductor current. Once the fault detection is enabled, the Fault pin pulls low when any of the feedback voltages (V_{FB1}, V_{FB2} or Max(V_{VFB3},V_{IFB3})) fall below their regulation value for more than 16ms.

One particularly important case is an overload or short-circuit condition on any of the channel outputs. In this case, if the corresponding loop is unable to bring the output back into regulation within 16ms, a fault is detected and the Fault pin is pulled low.

Note that the fault condition is latched. Once the Fault pin is pulled low, all the three channels are disabled. In order to enable any of the channels again, reset the part by shutting it down and then turning it on again. This is done by first forcing both the EN/SS1 and EN/SS3 pins low below 200mV and then either letting them go high again in a soft-start process or forcing them high immediately if no soft-start is desired. Figure 10 shows the waveforms when a short-circuit condition occurs at Boost1 for more than 16ms as well as the subsequent resetting of the part.

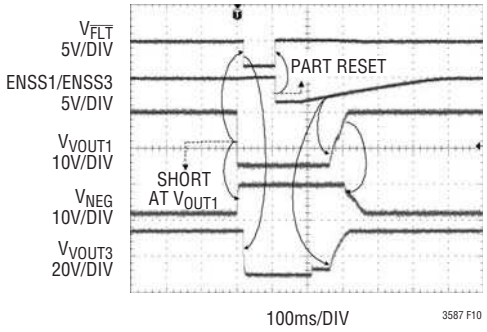


Figure 10. Waveforms During Fault Detection of a Short-Circuit Event

APPLICATIONS INFORMATION

Besides acting as a fault output indicator, the Fault pin is also an input pin. If this pin is externally forced low below 400mV, the LT3587 behaves as if a fault event has been detected and all the channels turn off. In order to turn the part back on, remove the external voltage that forces the pin low and reset the part. Figure 11 shows the waveforms when the Fault pin is externally forced low and the subsequent resetting of the part.

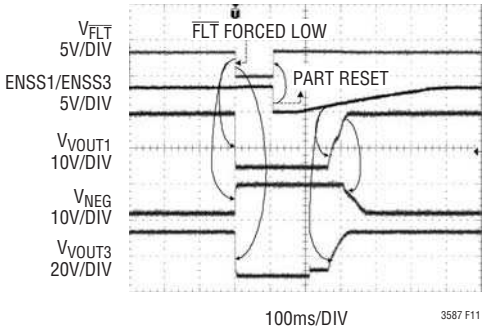


Figure 11. Waveforms When the Fault Pin is Externally Forced Low

Dimming Control For Boost3 Current Regulator as an LED Driver

As shown on the front page application and the Block Diagram, one of the most common applications for the Boost3 channel when configured as a boost current regulator is a backlight LED driver. In an LED driver application, there are two different ways to implement a dimming control of the LED string. The LED current can be adjusted either by using a digital to analog converter (DAC) with a resistor R_{IFB3} or by using a PWM signal.

Using a DAC and a Resistor

For some applications, the preferred method of brightness control is using a DAC and a resistor. The Boost3 configuration for using this method is shown in Figure 12.

Since the programmed V_{OUT3} current is proportional to the current through R_{IFB3}, the LED current can be adjusted according to the following formula:

$$I_{VOUT3} = (0.8V – V_{DAC\text{-}OUT}) \bullet 200/R_{IFB3}$$

A higher DAC output voltage level results in lower LED current and hence lower overall brightness. Conversely, a lower DAC output voltage results in higher LED current and higher brightness. Note that the DAC output impedance should be low enough to be able to sink approximately 1/200 of the desired maximum LED current without any appreciable error for accurate dimming control.

Note also that the maximum output current is limited by the output disconnect current limit to 110mA (typ).

PWM Dimming

Changing the forward current flowing in the LEDs not only changes the brightness intensity of the LEDs, it also changes the color. The chromaticity of the LEDs changes with the change in forward current. Many applications cannot tolerate any shift in the color of the LEDs. Controlling the intensity of the LEDs with a direct PWM signal allows dimming of the LEDs without changing the color. In addition, direct PWM dimming offers a wider dimming range to the user.

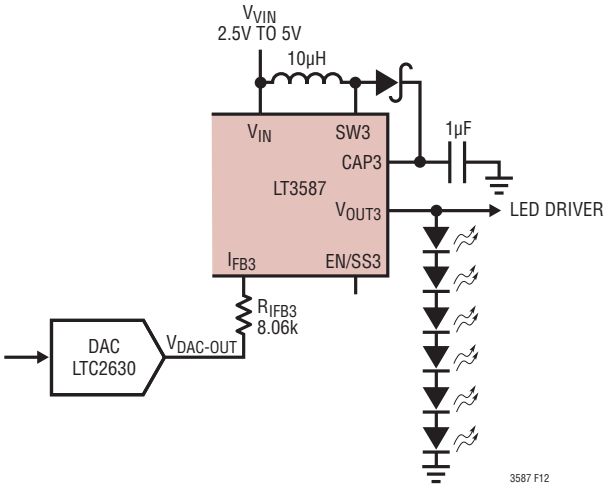


Figure 12. Dimming Using a DAC and a Resistor

APPLICATIONS INFORMATION

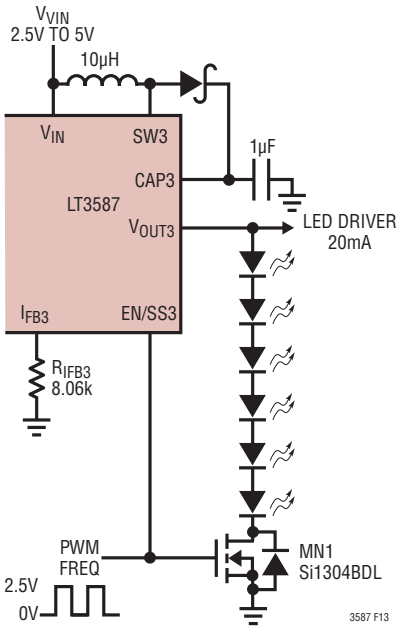


Figure 13. Six White LEDs Driver With PWM Dimming

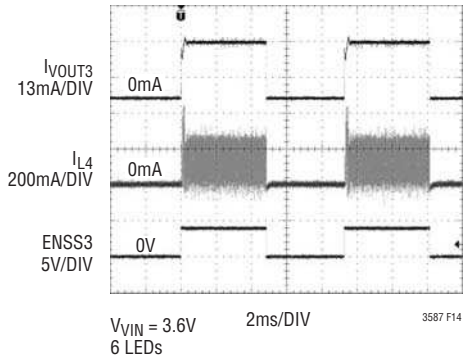


Figure 14. PWM Dimming Waveforms

Dimming the LEDs via a PWM signal essentially involves turning the LEDs on and off at the PWM frequency. The typical human eye has a sensitivity limit of ~60Hz. By increasing the PWM frequency to ~80Hz or higher, the eye will interpret that the pulsed light source is continuously on. Additionally, by modulating the duty cycle (amount of "on-time"), intensity of the LEDs is controlled. The color of the LEDs remains unchanged in this scheme since the LED current is either zero or a constant value.

Figure 13 shows a partial application showing an LED driver for six white LEDs. If the voltage at the CAP3 pin is higher than 10V when the LEDs are on, direct PWM dimming method requires an external NMOS. This external NMOS is tied between the cathode of the lowest LED in the string and ground as shown in Figure 13.

A Si1304 logic-level MOSFET can be used since its source is connected to ground, and it is able to withstand the open-circuit voltage at the V_{OUT3} pin across its drain and source. The PWM signal must be applied to the EN/SS3 pin of the LT3587 and the gate of the NMOS. The PWM signal should traverse between 0V to 2.5V, to ensure proper turn on and off of the Boost3 regulation loop and the NMOS transistor MN1. When the PWM signal goes high, the LEDs are connected to ground and a current of $I_{VOUT3} = 160V/R_{IFB3}$ flows through the LEDs. When the PWM signal goes low, the LEDs are disconnected and turned off.

The output disconnect feature and the external NMOS ensure that the LEDs quickly turn off without discharging the output capacitor. This allows the LEDs to turn on faster. Figure 14 shows the PWM dimming waveforms for the circuit in Figure 13.

APPLICATIONS INFORMATION

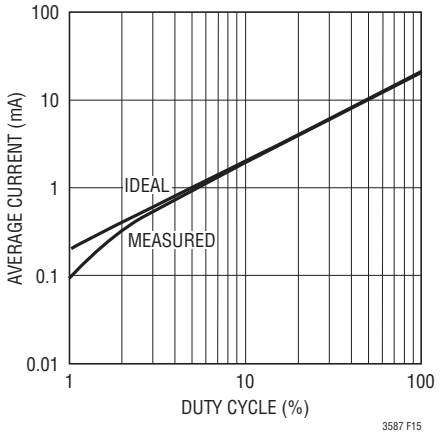


Figure 15. Average LED Current Variation with PWM Duty Cycle at 100Hz PWM Frequency

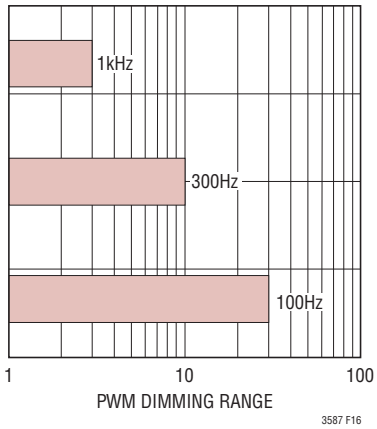


Figure 16. Dimming Range Comparison of Three PWM Frequencies

The time it takes for the LED current to reach its programmed value sets the achievable dimming range for a given PWM frequency. Figure 15 shows the average current variation over duty cycle for a 100Hz PWM frequency with the circuit in Figure 13.

Notice that at lower end of the duty cycle, the linear relation between the average LED current and the PWM duty cycle is no longer preserved. This indicates that the loop requires a fixed amount of time to reach its final current. When the duty cycle is reduced such that the amount of on time is in the order of or less than this settling time, the loop no longer has the time to regulate to its final current before it is turned off again and the initial current before settling is a larger proportion of the average current.

Depending on how much linearity on the average LED current is required, the minimum LED on time is chosen based on the graphs in Figure 15. For example, for approximately 10% deviation from linearity at the lower duty cycle, the minimum on time of the LED current is approximately 320µs for a 3.6V input voltage.

The achievable dimming range for this application with a 100Hz PWM frequency can be determined using the following method.

Example:

$f = 100Hz \rightarrow t_{PERIOD} = 1/f = 0.01s$, $t_{MIN-ON} = 320\mu s$

$Dim\ Range = t_{PERIOD}/t_{MIN-ON} = 0.01s/320\mu s \approx 30:1$

$Min\ Duty\ Cycle = (t_{MIN-ON}/t_{PERIOD}) \bullet 100 = 3.2\%$

$Duty\ Cycle\ Range = 100\% \rightarrow 3.2\%\ at\ 100Hz$

The calculations show that for a 100Hz signal the dimming range is 30 to 1. In addition, the minimum PWM duty cycle of 3.2% ensures that the LED current varies linearly with duty cycle to within 10%. Figure 16 shows the dimming range achievable for three different frequencies with a minimum on time of 320µs.

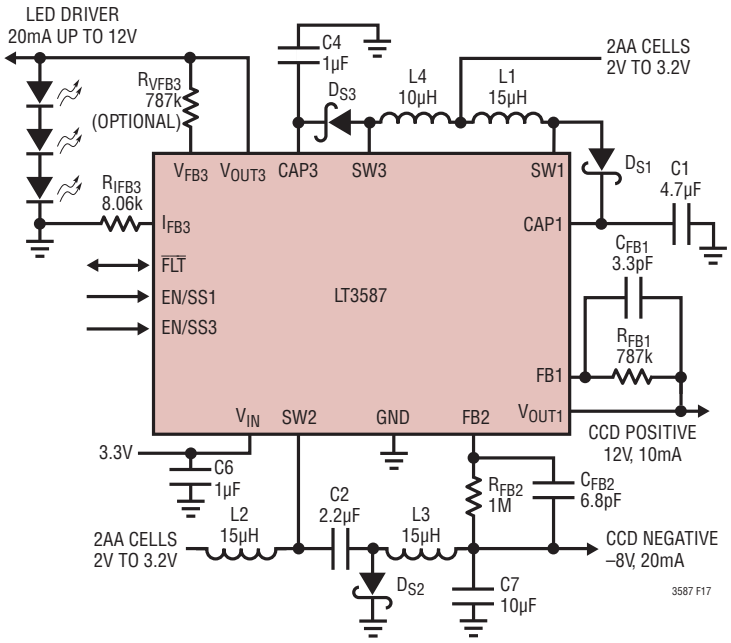
The dimming range can be further extended by combining this PWM method with the DAC and resistor method discussed previously. In this manner both analog dimming and PWM dimming extend the dimming range for a given application. The color of the LEDs no longer remains constant because the forward current of the LED changes with the output voltage of the DAC. For the six LED application described above, the LEDs can be dimmed first by modulating the duty cycle of the PWM signal with the DAC output at 0V. Once the minimum duty cycle is reached, the value of the DAC output voltage can be increased to further dim the LEDs. The use of both techniques together allows the average LED current for the six LED application to be varied from 20mA down to less than 1µA.

APPLICATIONS INFORMATION

Lower Input Voltage Applications

The LT3587 can be used in lower input voltage applications. The V_{IN} supply voltage to the LT3587 must be 2.5V to 6V. However, the inductors can be run off a lower voltage. This allows the outputs to be powered off two alkaline cells. Most portable devices and systems have a 3.3V logic supply voltage which can be used to power the LT3587. The outputs can be driven straight from the battery, resulting in higher efficiency.

Figure 17 shows a typical digital still camera application with CCD positive and negative supply as well as an LED driver powered by two AA cells. The battery is connected to the input inductors and the chip is powered with a 3.3V logic supply voltage.



C1: MURATA GRM21BR61E475KA12L
C2: MURATA GRM188R61C225KE15D
C4: MURATA GRM188R61E105KA12B
C6: MURATA GRM155R61A105KE15D
C7: MURATA GRM21BR71A106KE51L
C_{FB1}: MURATA GRM1555C1H3R3BZ01D
C_{FB2}: MURATA GRM1555C1H6R3BZ01D
L1, L2, L3: SUMIDA CDRH2D18/HP-150N
L4: TOKO 1071AS-100M
D_{S1}, D_{S2}, D_{S3}: NXP PMEG2005EB

Figure 17. 2 AA Cells Providing CCD Positive and Negative Supply and a Three White Backlight LED Driver

APPLICATIONS INFORMATION

Board Layout Consideration

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential.

In order to minimize magnetic field radiation, reduce the parasitic inductance by keeping the traces that conduct high switching currents short, wide and with minimal overall loop area. These are typically the traces associated with the switches. Figure 18 outlines the critical paths.

The voltage signals of the SW1, SW2 and SW3 pins have rise and fall times of a few ns. Minimize the length and area of all traces connected to the SW1, SW2 and SW3 pins to reduce capacitive coupling between these fast nodes and other circuitry. In particular, keep all the traces of the feedback voltage pins (FB1, FB2, V_{FB3} and I_{FB3}) away from the switching node. Always use a ground plane under the switching regulator to minimize interplane coupling.

Finally, place as much of the output capacitors of each channel close to their respective CAP pins. Recommended component placement is shown in Figure 19.

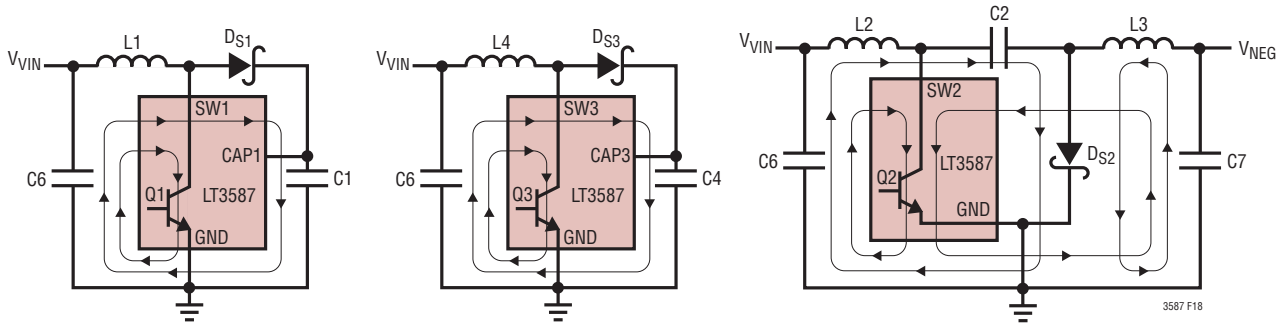


Figure 18. High Current Paths

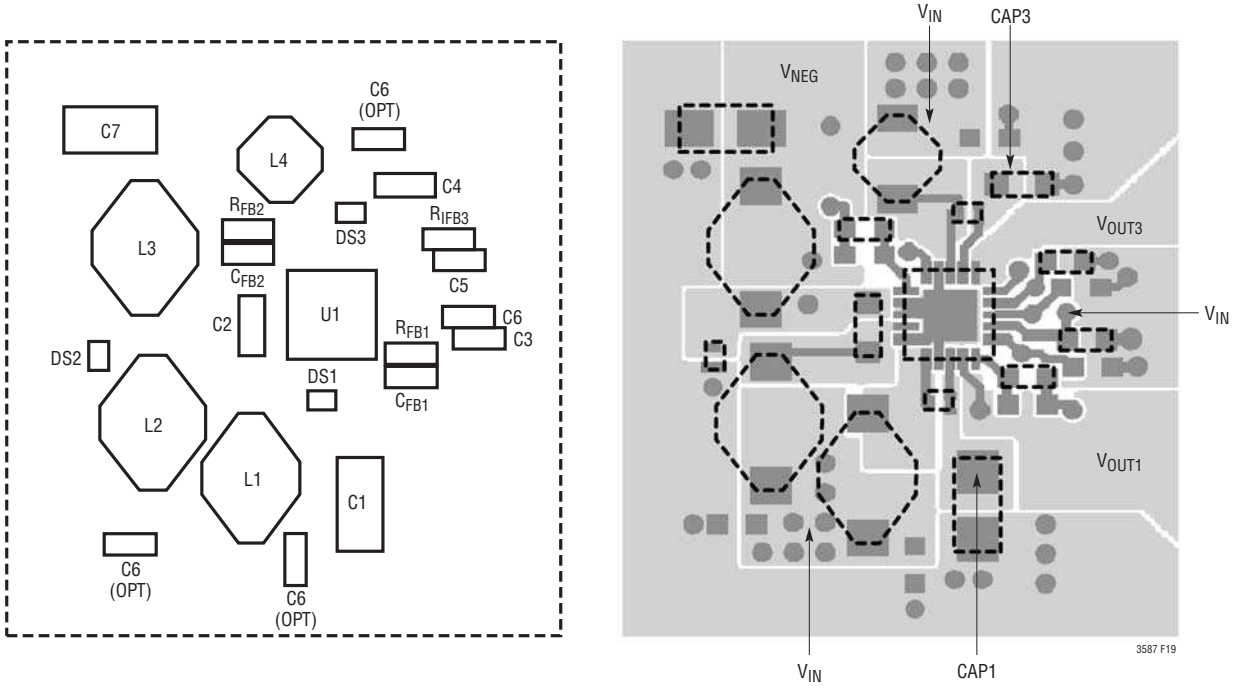
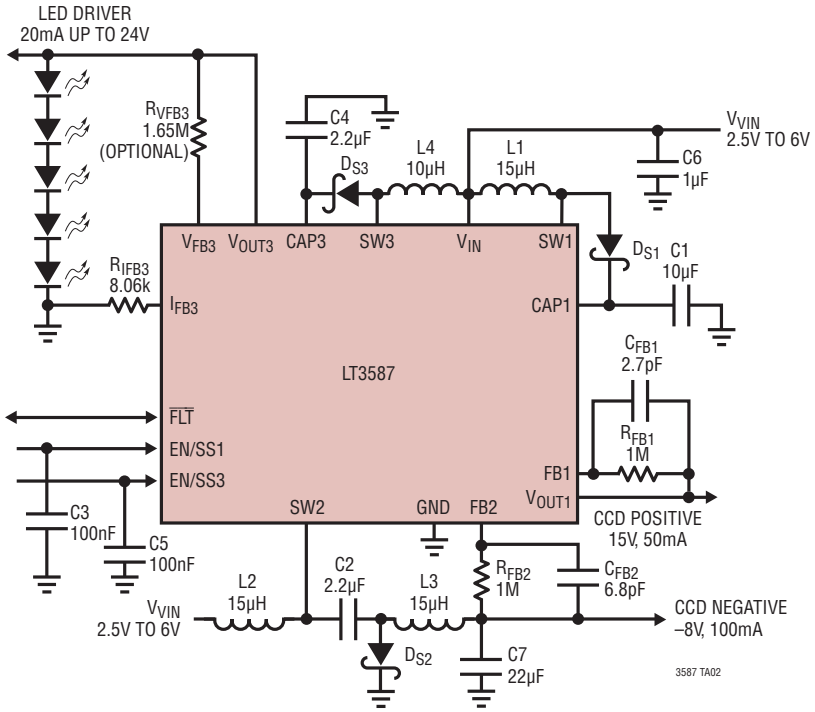


Figure 19. Recommended Component Placement

TYPICAL APPLICATIONS

Li-Ion Powered Supply for CCD Imager and Five White Backlight LEDs

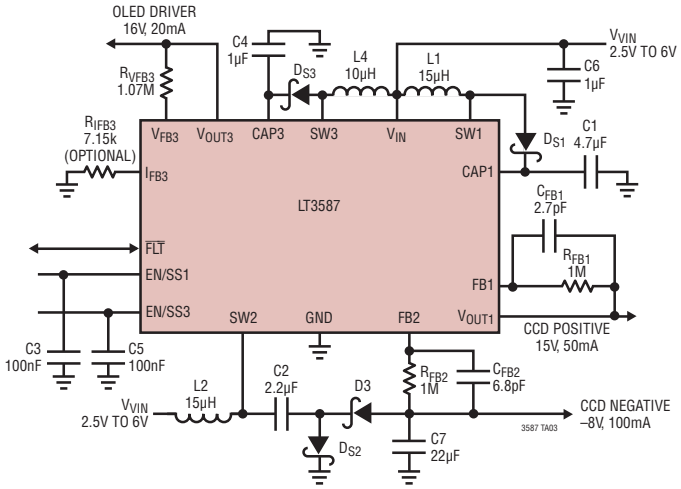


C1: MURATA GRM21BR61C106KE15L
C2: MURATA GRM188R61C225KE15D
C3, C5: MURATA GRM033R60J104KE19D
C4: MURATA GRM21BR71E225KA73L
C6: MURATA GRM155R61A105KE15D
C7: TAIYO YUDEN LMK212BJ226MG-T

C_{FB1}: MURATA GRM1555C1H2R7BZ01D
C_{FB2}: MURATA GRM1555C1H6R8BZ01D
L1, L2, L3: SUMIDA CDRH2D18/HP-150N
L4: TOKO 1071AS-100M
D_{S1}, D_{S2}, D_{S3}: IR IR05H40CSPTR

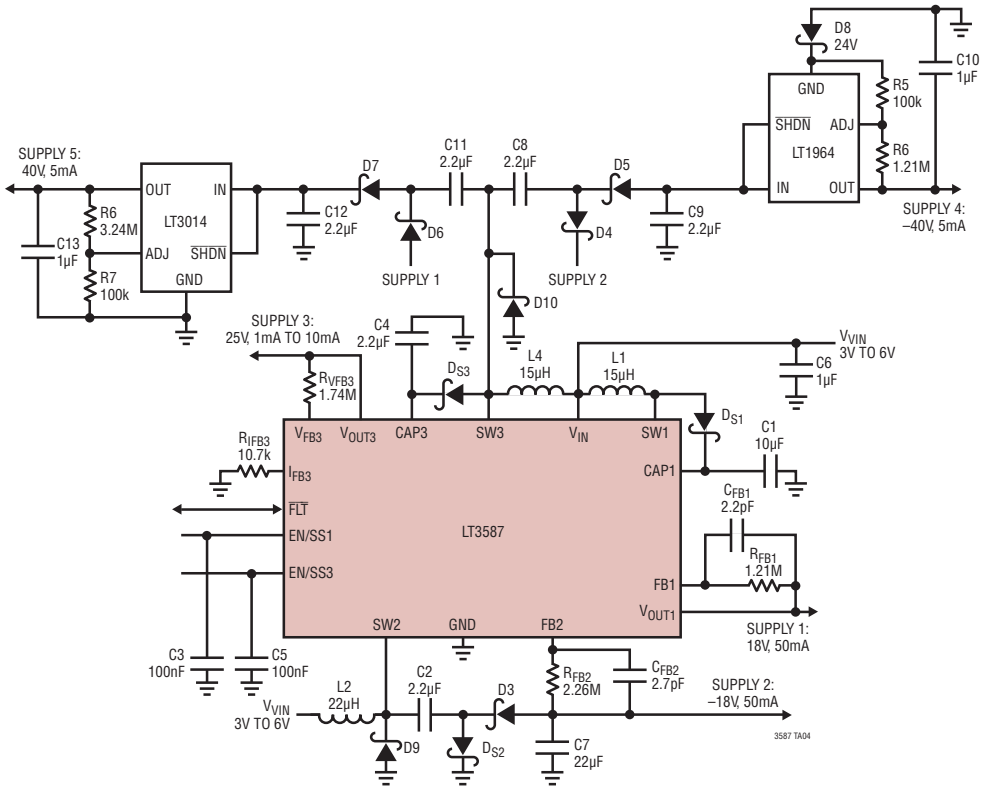
TYPICAL APPLICATIONS

Driver For a CCD Imager and an OLED Display Panel with Soft-Start



C1: TAIYO YUDEN TMK212BJ475KG-T
C2: TAIYO YUDEN EMK107BJ225KA-T
C3, C5: TAIYO YUDEN JMK063BJ104KP-F
C4: TAIYO YUDEN GMK107BJ105KA-T
C6: TAIYO YUDEN LMK105BJ105KV-F
C7: TAIYO YUDEN LMK212BJ226MG-T
C_{FB1}: TAIYO YUDEN EMK105SK2R7JW-F
C_{FB2}: TAIYO YUDEN EMK105SH6R8JW-F
L1, L2: SUMIDA CDRH2D18/HP-150N
L4: TOKO 1071AS-100M
D_{S1}, D_{S2}, D_{S3}, D3: NXP PMEG2005EB

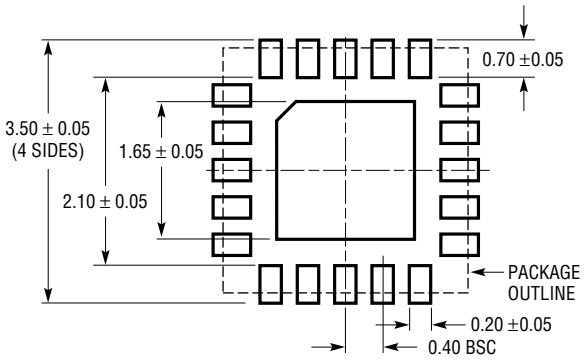
Extending the High Voltage Range and the Number of Independently Controlled Regulated Outputs



C1: MURATA GRM31CR71E106KA12L
C2, C8, C11: MURATA GCM21BR71E225KA73L
C3, C5: MURATA GRM033R60J104KE19D
C4: MURATA GRM21BR71E225KA73L
C6: MURATA GRM155R61A105KE15D
C7: MURATA GRM32ER61E226KE15L
C9, C12: MURATA GRM31CR71H225KA55L
C10, C13: MURATA GRM21BR71H105KA12L
C_{FB1}: MURATA GRM1555C1H2R2BZ01D
C_{FB2}: MURATA GRM1555C1H2R7BZ01D
L1, L4: COILCRAFT LPS4018-153
L2, L3: COILCRAFT LPS4018-223
D_{S1}, D_{S2}, D_{S3}, D3, D4, D5, D6, D7, D9, D10: IR IR05H40CSPTR
D8: DIODES INC DDZ9709T

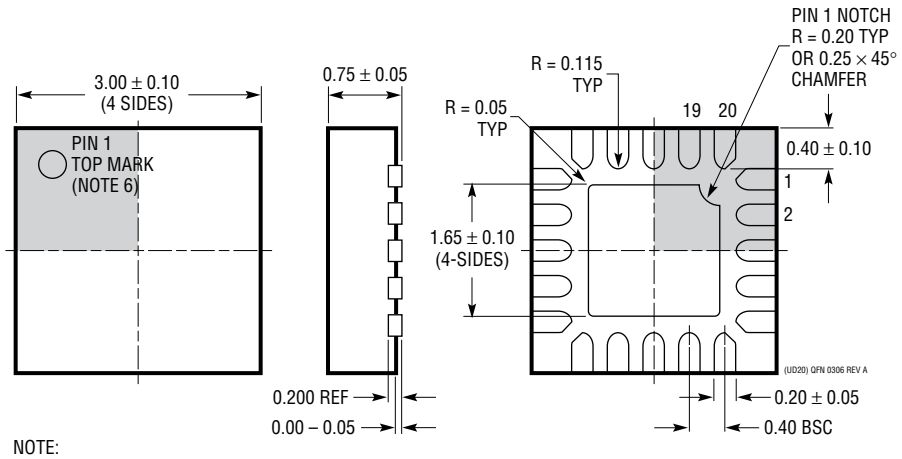
PACKAGE DESCRIPTION

UD Package
20-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1720 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

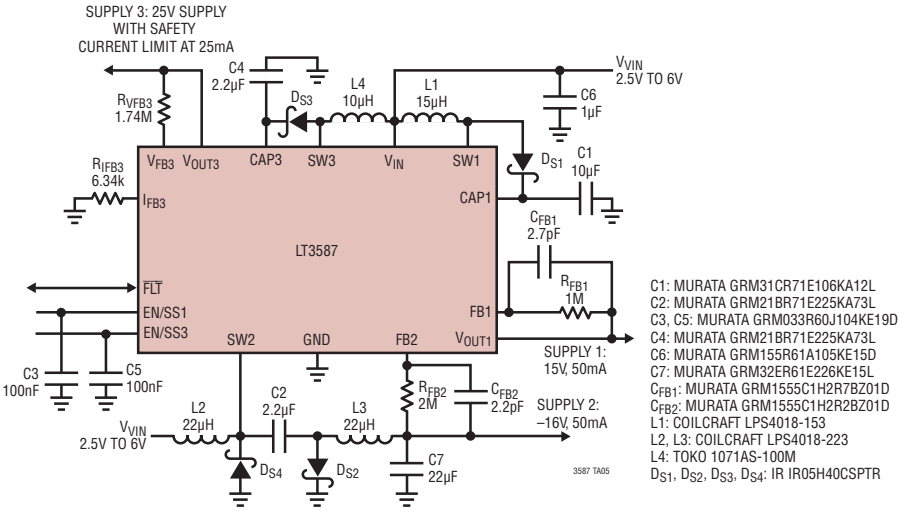
BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

General Purpose High Voltage Supplies Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1944	Dual Output, Boost/Inverter, 350mA I_{SW}, High Efficiency Boost-Inverting DC/DC Converter	$V_{IN(MIN)}$ = 1.2V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 20, I_{SD} < 1µA, MSOP-10 Package
LT1945	Dual Output, Boost/Inverter, 350mA I_{SW}, High Efficiency Boost-Inverting DC/DC Converter	$V_{IN(MIN)}$ = 1.2V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 20, I_{SD} < 1µA, MSOP-10 Package
LT3463/LT3463A	Dual Output, Boost/Inverter, 250mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter with Integrated Schottkys	$V_{IN(MIN)}$ = 2.3V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MAX)}$ = 40V, I_Q = 40µA, I_{SD} < 1µA, 3 × 3 DFN-10 Package
LT3466/LT3466-1	Dual Constant Current, 2MHz, High Efficiency White LED Boost Regulator with Integrated Schottky Diode	$V_{IN(MIN)}$ = 2.7V, $V_{IN(MAX)}$ = 24V, $V_{OUT(MAX)}$ = 40V, I_Q = 5mA, I_{SD} < 16µA, 3 × 3 DFN-10 Package
LT3471	Dual Output, Boost/Inverter, 1.3A I_{SW}, 1.2MHz, High Efficiency Boost-Inverting DC/DC Converter	$V_{IN(MIN)}$ = 2.4V, $V_{IN(MAX)}$ = 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 2.5mA, I_{SD} < 1µA, 3 × 3 DFN-10 Package
LT3472/LT3472A	Dual Output, Boost/Inverter, 400mA I_{SW}, 1.2MHz, High Efficiency Boost-Inverting DC/DC Converter	$V_{IN(MIN)}$ = 2.2V, $V_{IN(MAX)}$ = 16V, $V_{OUT(MAX)}$ = ±34V I_Q = 2.8mA, I_{SD} < 1µA, 3 × 3 DFN-10 Package
LT3473/LT3473A	40V, 1A, 1.2MHz Micropower Low Noise Boost Converter with Output Disconnect	$V_{IN(MIN)}$ = 2.2V, $V_{IN(MAX)}$ = 16V, $V_{OUT(MAX)}$ = 36V, I_Q = 150µA, I_{SD} < 1µA, 3 × 3 DFN-12 Package
LT3494/LT3494A	40V, 180mA/350mA Micropower Low Noise Boost Converter with Output Disconnect	$V_{IN(MIN)}$ = 2.3V, $V_{IN(MAX)}$ = 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 65µA, I_{SD} < 1µA, 3 × 2 DFN-8 Package
LT3497	Dual 2.3MHz, Full Function LED Driver with Integrated Schottkys and 250:1 True Color PWM Dimming	$V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 10V, $V_{OUT(MAX)}$ = 32V, I_Q = 6mA, I_{SD} < 12µA, 2 × 3 DFN-10 Package
LT3580	40V, 2A, 2.5MHz Boost/Inverter DC/DC Converter	V_{IN}: 2.5V to 32V, $V_{OUT(MAX)}$ = 40V, I_Q = 1mA, I_{SD} < 1µA, MSOP-8E, 3mm × 3mm DFN-8 Packages

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