FAIRCHILD
SEMICONDUCTOR®

August 2010

FDMS8025S

N-Channel PowerTrench® SyncFETᵀᴹ

30 V, 49 A, 2.8 mΩ

Features

- Max $r_{DS(on)}$ = 2.8 mΩ at V_{GS} = 10 V, I_D = 24 A

- Max $r_{DS(on)}$ = 3.5 mΩ at V_{GS} = 4.5 V, I_D = 21 A

- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency

- SyncFET Schottky Body Diode

- MSL1 robust package design

- 100% UIL tested

- RoHS Compliant

General Description

The FDMS8025S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters

- Notebook Vcore/GPU low side switch

- Networking Point of Load low side switch

- Telecom secondary side rectification

Top

Bottom

Pin 1

Power 56

D	5		4	G
D	6		3	S
D	7		2	S
D	8		1	S
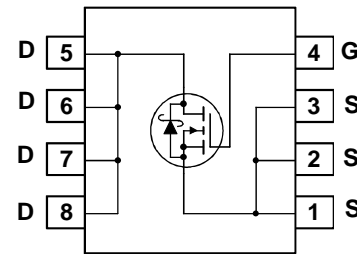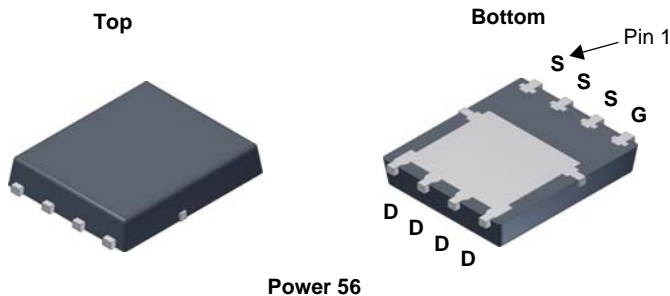
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		49	A
	-Continuous (Silicon limited)	T_C = 25°C		109	
	-Continuous	T_A = 25°C	(Note 1a)	24	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	66	mJ
P_D	Power Dissipation	T_C = 25°C		50	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case			2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8025S	FDMS8025S	Power 56	13 "	12 mm	3000 units

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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C		19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			500	µA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 24 A		2.2	2.8	mΩ
		V_{GS} = 4.5 V, I_D = 21 A		3.0	3.5	
		V_{GS} = 10 V, I_D = 24 A, T_J = 125°C		3.1	4.0	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 24 A		145		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1MHz		2255	3000	pF
C_{oss}	Output Capacitance			815	1085	pF
C_{rss}	Reverse Transfer Capacitance			85	125	pF
R_g	Gate Resistance			1.0	2.5	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 24 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		11	19	ns
t_r	Rise Time			4.5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			29	46	ns
t_f	Fall Time			3.7	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V		34	47	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		16	23	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 24 A		5.9		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.6		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.62	0.8	V
		V_{GS} = 0 V, I_S = 24 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 24 A, di/dt = 300 A/µs		26	42	ns
Q_{rr}	Reverse Recovery Charge			27	44	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
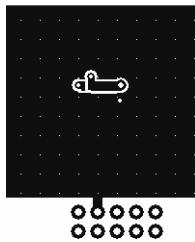
a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.
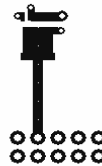
b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. E_{AS} of 66 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 21 A, V_{DD} = 27 V, V_{GS} = 10 V.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

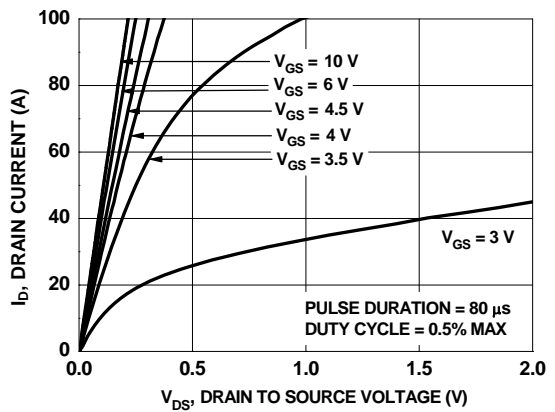## Typical Characteristics T_J = 25°C unless otherwise noted
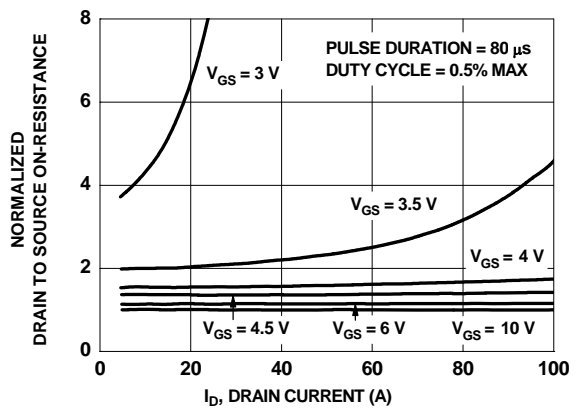

Figure 1. On Region Characteristics

Figure 2. Normalized On-Resistance
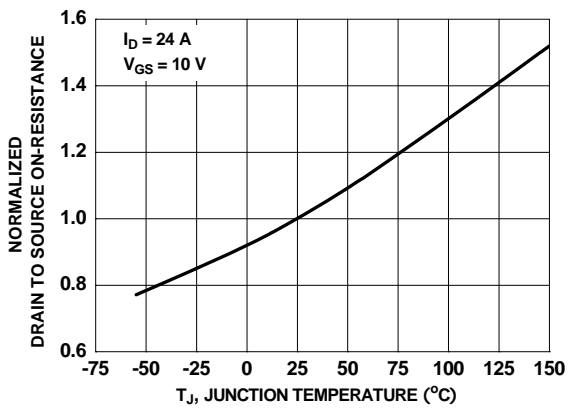vs Drain Current and Gate Voltage

Figure 3. Normalized On Resistance
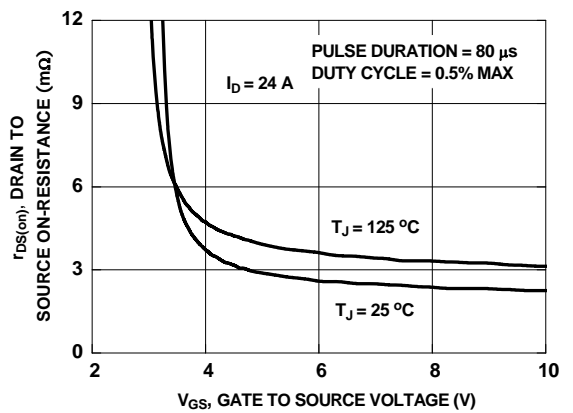vs Junction Temperature

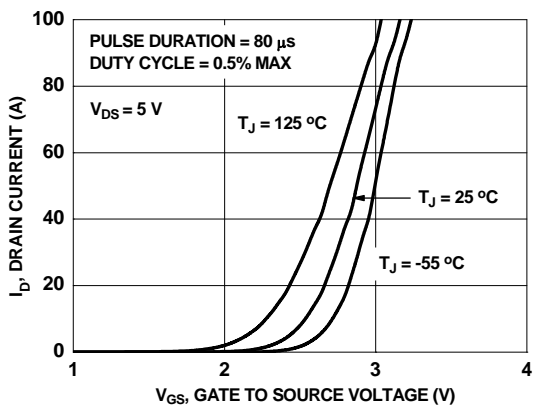
Figure 4. On-Resistance vs Gate to
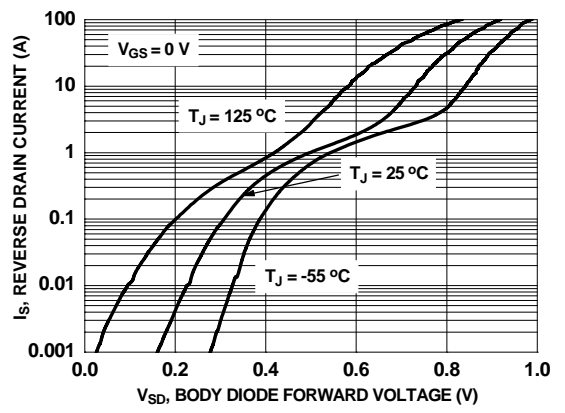Source Voltage

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode
Forward Voltage vs Source Current

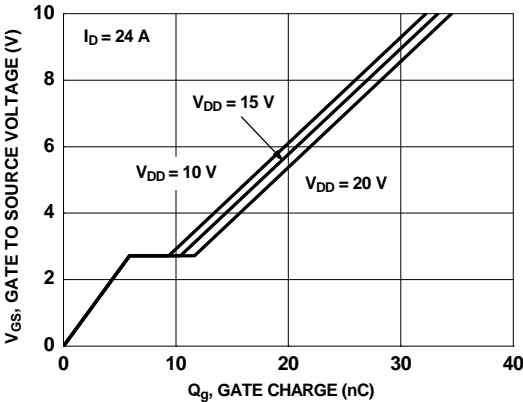**Typical Characteristics** T_J = 25°C unless otherwise noted

Figure 7. Gate Charge Characteristics
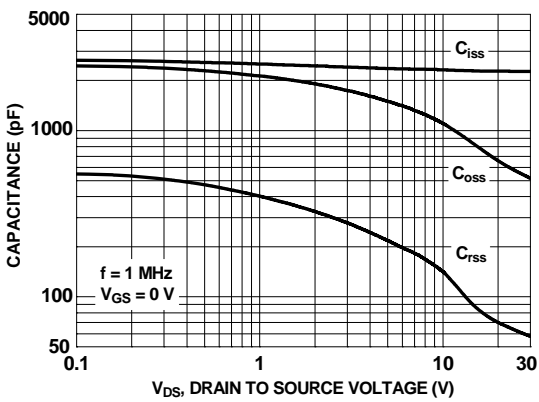
Figure 8. Capacitance vs Drain to Source Voltage
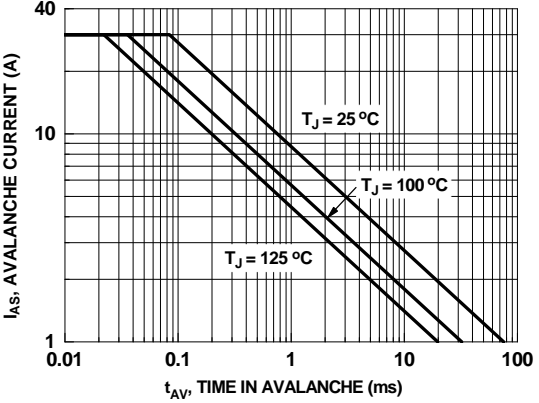
Figure 9. Unclamped Inductive Switching Capability
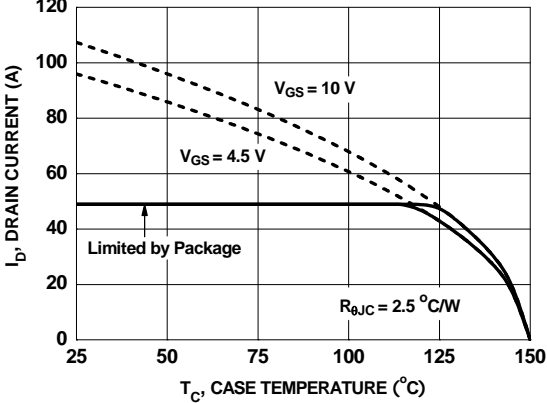
Figure 10. Maximum Continuous Drain Current vs Case Temperature
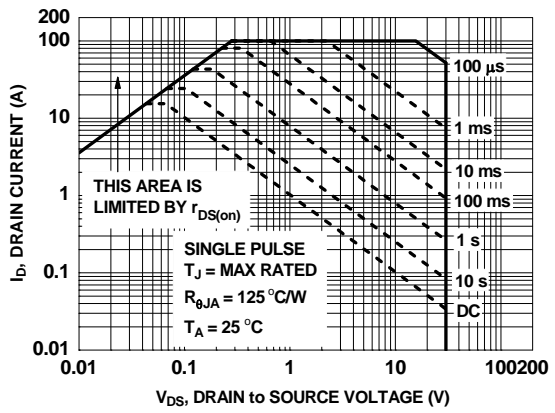
Figure 11. Forward Bias Safe Operating Area
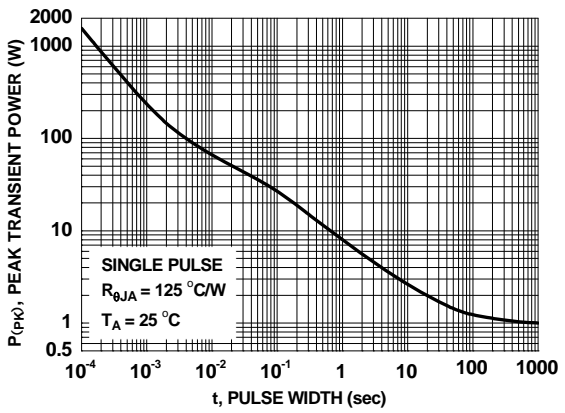
Figure 12. Single Pulse Maximum Power Dissipation

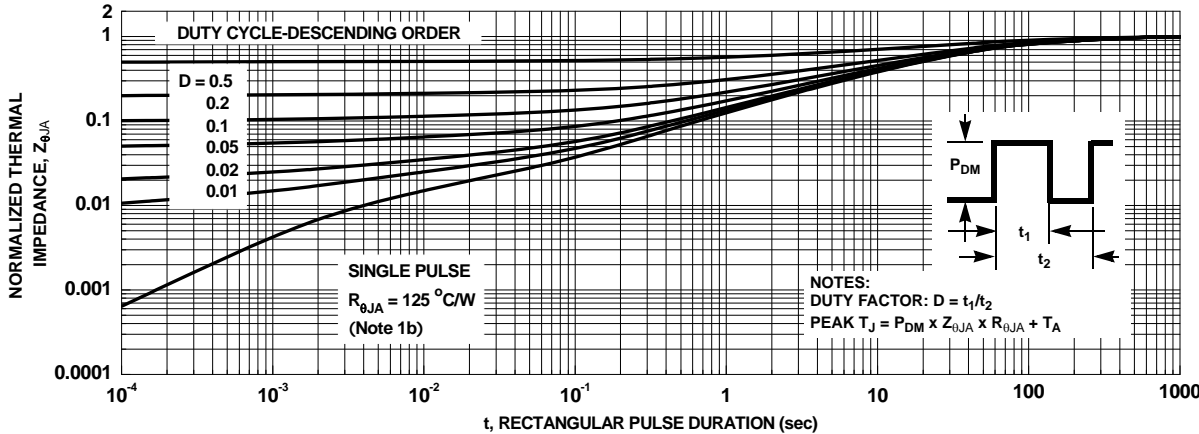## Typical Characteristics $T_J = 25°C$ unless otherwise noted

Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8025S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.
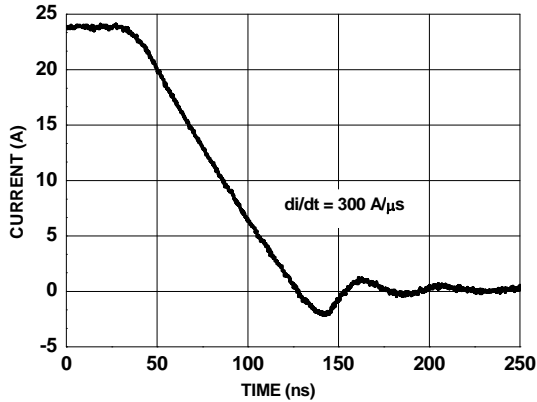
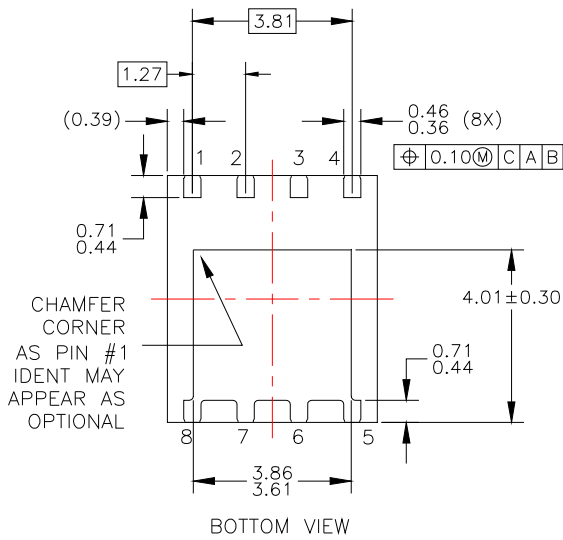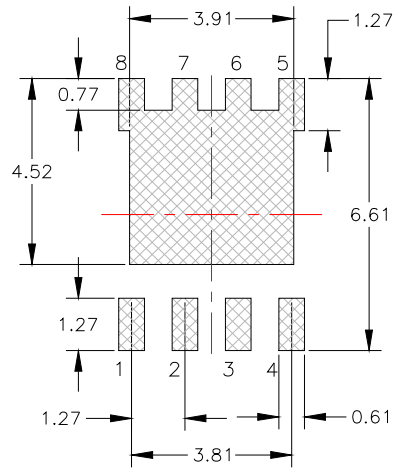**Figure 14. FDMS8025S SyncFET body diode reverse recovery characteristic**
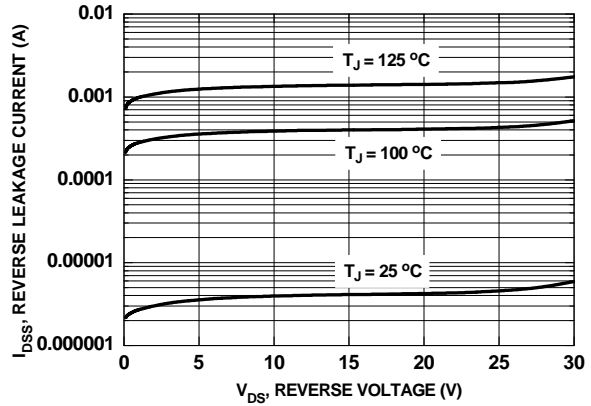
Figure 15. SyncFET body diode reverse leakage versus drain-source voltage

Dimensional Outline and Pad Layout

TOP VIEW

5.00 — [A]

PKG ℄

8   5   [B]

PKG ℄   6.00

PIN #1
IDENT MAY
APPEAR AS
OPTIONAL

1   4

SIDE VIEW

SEE
DETAIL A

LAND PATTERN
RECOMMENDATION

3.91   1.27

8 7 6 5

0.77

4.52   6.61

1.27

1   2   3   4

1.27   0.61

3.81

BOTTOM VIEW

3.81

1.27

(0.39)   0.46
0.36 (8X)

1 2   3 4   ⊕ 0.10 Ⓜ C A B

0.71
0.44

CHAMFER
CORNER
AS PIN #1
IDENT MAY
APPEAR AS
OPTIONAL

4.01±0.30

0.71
0.44

8 7 6 5

3.86
3.61

5.00

6.15   5.75

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE

6°

OPTIONAL TIE BARS MAY
APPEAR ON THESE AREAS (MAX.
TIE BAR PROTRUSION: 0.15mm)

// 0.10 C

⌒ 0.08 C

1.10
0.90

0.30
0.20

0.05
0.00

[C]

SEATING
PLANE

DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE:
    JEDEC MO-240, ISSUE A, VAR. AA,
    DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS
    OR MOLD FLASH. MOLD FLASH OR
    BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER
    ASME Y14.5M-1994.
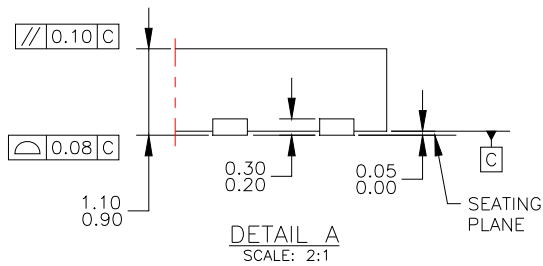
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DEUXPEED®	ISOPLANAR™	™	TINYOPTO™
Dual Cool™	MegaBuck™		TinyPower™
EcoSPARK®	MICROCOUPLER™	Saving our world, 1mW/W/kW at a time™	TinyPWM™
EfficentMax™	MicroFET™	SignalWise™	TinyWire™
ESBC™	MicroPak™	SmartMax™	TriFault Detect™
F®	MicroPak2™	SMART START™	TRUECURRENT™*
	MillerDrive™	SPM®	μSerDes™
Fairchild®	MotionMax™	STEALTH™	
Fairchild Semiconductor®	Motion-SPM™	SuperFET™	
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FACT®	OPTOLOGIC®	SuperSOT™-6	Ultra FRFET™
FAST®	OPTOPLANAR®	SuperSOT™-8	UniFET™
FastvCore™	®	SupreMOS™	VCX™
FETBench™		SyncFET™	VisualMax™
FlashWriter® *	PDP SPM™	Sync-Lock™	XS™
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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