

**FEATURES**

- 2.0V~5.5V Power supply.
- Thermal shutdown Protection.
- Low current shutdown mode
- No output capacitors and networks or bootstrap capacitors required
- Low noise during turn-on and turn-off transitions
- Lead free and green package available. (RoHS Compliant)
- Space Saving Package  
-- 8-pin MSOP package.

**GENERAL DESCRIPTION**

The LY8891 is a 2.0W audio power amplifier. It is capable of driving 4Ω speaker load at a continuous average output of 2.0W with less than 10% distortion (THD+N) from a 5.5V power supply and 8Ω speaker load at a continuous average output of 1.4W with less than 10% distortion (THD+N) from a 5.0V power supply.

The LY8891 primarily designed for high quality application in other portable communication device. And the LY8891 audio amplifier features low power consumption shutdown mode. It is achieved by driving the shutdown pin with logic low.

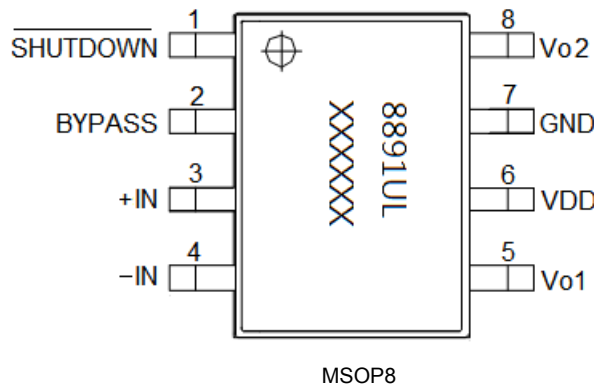
And the LY8891 has an internal thermal shutdown protection feature.

The LY8891 audio amplifier was designed specifically to provide high quality output power with a minimal amount of external components. The LY8891 does not require output capacitors, and the LY8891 is ideally suited for other low voltage applications or portable electronic devices where minimal power consumption is a primary requirement.

**APPLICATION**

- Portable electronic devices
- Mobile Phones
- PDAs

**PIN CONFIGURATION**





#### PIN DESCRIPTION

SYMBOL	Pin No.	DESCRIPTION
	MSOP8	
SHUTDOWN	1	Shutdown the device. (when <b>LOW</b> level is shutdown mode)
BYPASS	2	Bypass pin
+IN	3	Positive Input
-IN	4	Negative Input
Vo1	5	Negative output
V <sub>DD</sub>	6	Power Supply
GND	7	Ground
Vo2	8	Positive Output

#### ORDERING INFORMATION

Ordering Code	Packing Type	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)	Input Type	Output Type
LY8891ULT	Tape & Reel	Mono	MSOP8	2.0W/4Ω @5.5V_BTL 1.8W/4Ω @5.0V_BTL 1.7W/8Ω @5.5V_BTL 1.4W/8Ω @5.0V_BTL	SE/ DF	BTL

### APPLICATION CIRCUIT

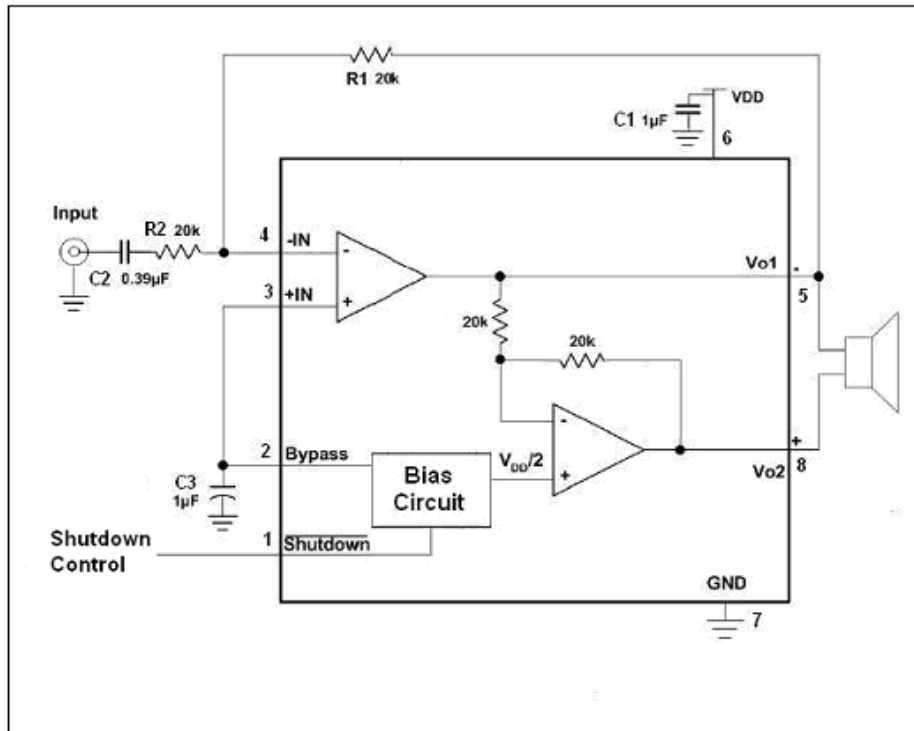


Figure 1. LY8891 application schematic with Single -Ended input

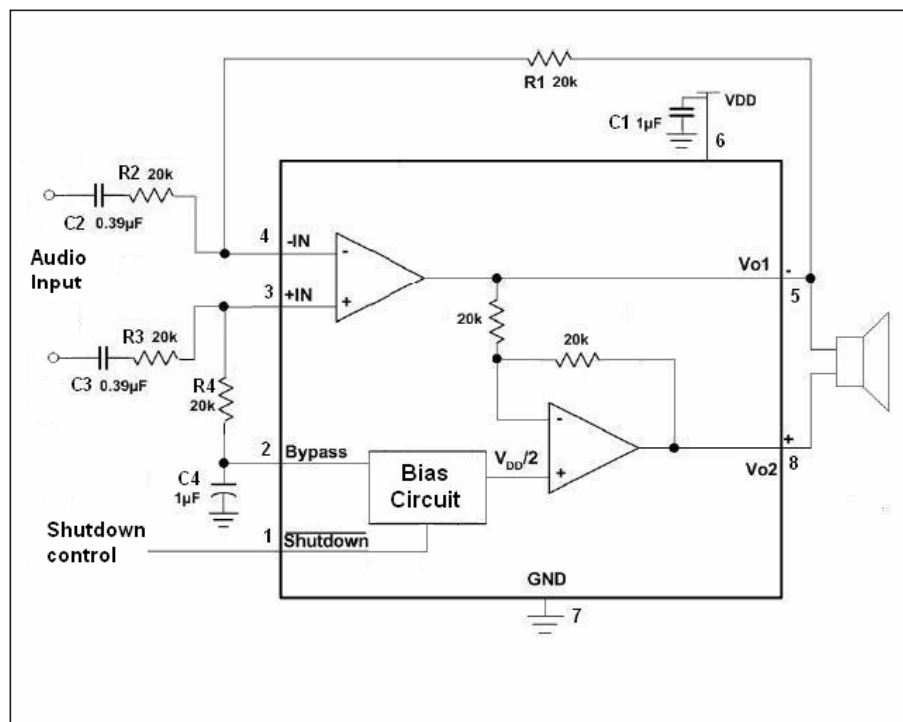


Figure 2. LY8891 application schematic with Differential input



#### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	6.0	V
Operating Temperature	T <sub>A</sub>	-40 to 85 (I grade)	°C
Input Voltage	V <sub>I</sub>	-0.3V to V <sub>DD</sub> +0.3V	V
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	Internally Limited	W
ESD Susceptibility	V <sub>ESD</sub>	2000	V
Junction Temperature	T <sub>JMAX</sub>	150	°C
Soldering Temperature (under 10 sec)	T <sub>SOLDER</sub>	260	°C

#### DC ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=5.0V, T<sub>A</sub>=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>(*)</sup>	MAX.	UNIT
Power Supply Current	I <sub>DD</sub>	V <sub>IN</sub> = 0V, I <sub>o</sub> = 0A, 8Ω Load	-	5.0	15.0	mA
Shutdown Current	I <sub>SD</sub>	V <sub>SHUTDOWN</sub> = 0V	-	0.1	2.0	μA
Shutdown Voltage Input High	V <sub>SDIH</sub>	V <sub>SD Mode</sub> = V <sub>DD</sub>	1.2	-	-	V
Shutdown Voltage Input Low	V <sub>SDIL</sub>	V <sub>SD Mode</sub> = GND	-	-	0.4	
Output Offset Voltage	V <sub>OS</sub>		-	7.0	50.0	mV
Resistor Output to GND	R <sub>OUT-GND</sub>		-	9.5	-	kΩ
Output Power	P <sub>o</sub>	THD = 10% , f = 1 kHz R <sub>L</sub> =4Ω (at 5.5V)	-	2.0	-	W
		THD = 10% , f = 1 kHz R <sub>L</sub> =4Ω (at 5.0V)	-	1.8	-	
		THD = 1% , f = 1 kHz R <sub>L</sub> =4Ω (at 5.0V)	-	1.4	-	
		THD = 10% , f = 1 kHz R <sub>L</sub> =8Ω (at 5.5V)	-	1.7	-	
		THD = 10% , f = 1 kHz R <sub>L</sub> =8Ω (at 5.0V)	-	1.4	-	
		THD = 1% , f = 1 kHz R <sub>L</sub> =8Ω (at 5.0V)	-	1.0	-	
Total Harmonic Distortion+ Noise	THD+N	P <sub>o</sub> = 635 mWrms; f = 1kHz	-	0.1		%
Power Supply Rejection Ratio	PSRR	V <sub>ripple</sub> = 200mV sine p-p, Input with floating.	-	66 (f = 217Hz) 66 (f = 1kHz)	-	dB
Wake-up time	T <sub>WU</sub>	Bypass Cap.=1.0uF, 5.0V	-	145		ms
Thermal Shutdown Temperature	T <sub>SD</sub>		150	170	190	°C
Shut Down Time	T <sub>SDT</sub>	8 Ω load		1.0		ms

(\*1)Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at VCC = VCC(TYP.) and TA = 25°C



#### DC ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=3.6V, T<sub>A</sub>=25°C)

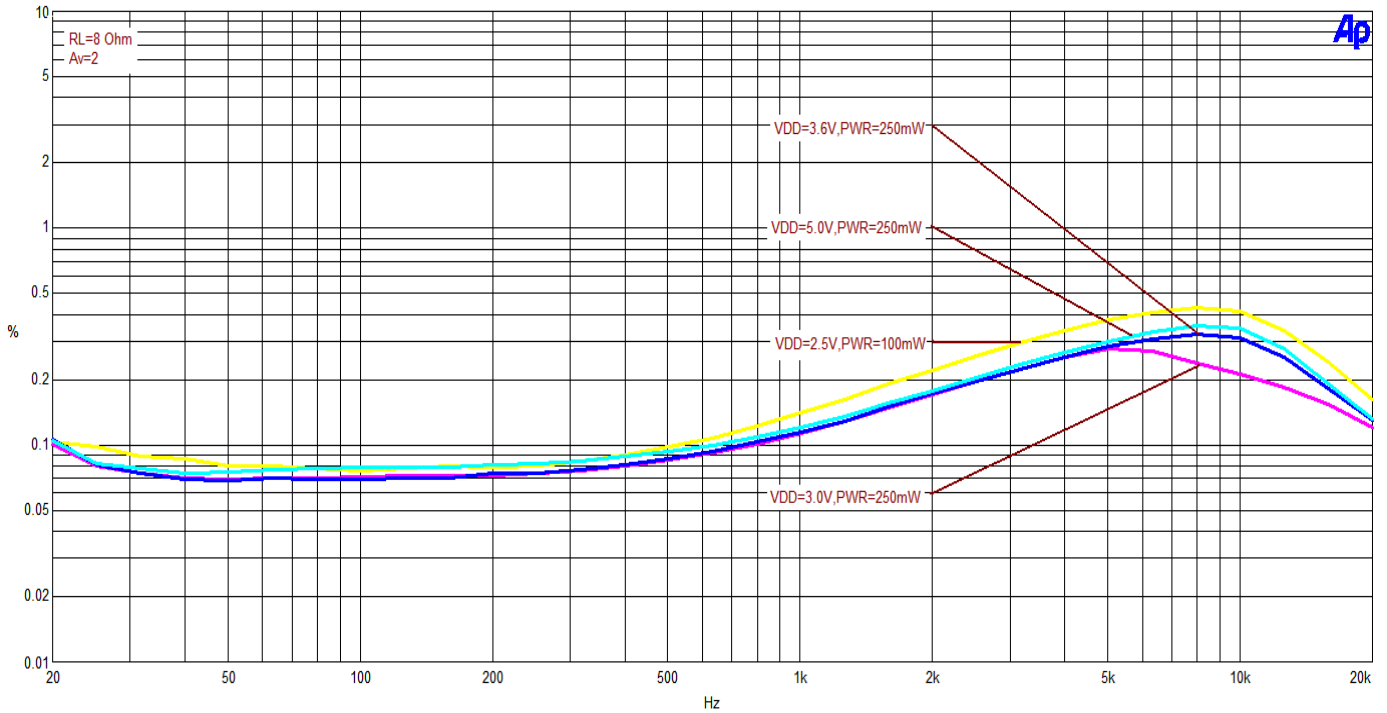
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>(*)</sup>	MAX.	UNIT
Power Supply Current	I <sub>DD</sub>	V <sub>IN</sub> = 0V, I <sub>o</sub> = 0A, 8Ω Load	-	4.5	14.0	mA
Shutdown Current	I <sub>SD</sub>	V <sub>SHUTDOWN</sub> = 0V	-	0.1	2.0	μA
Shutdown Voltage Input High	V <sub>SDIH</sub>	V <sub>SD Mode</sub> = V <sub>DD</sub>	1.2	-	-	V
Shutdown Voltage Input Low	V <sub>SDIL</sub>	V <sub>SD Mode</sub> = GND	-	-	0.4	
Output Offset Voltage	V <sub>OS</sub>		-	7.0	50.0	mV
Resistor Output to GND	R <sub>OUT-GND</sub>		7.0	8.5	9.7	kΩ
Output Power	P <sub>o</sub>	THD = 10% , f = 1 kHz R <sub>L</sub> =4Ω	-	900	-	mW
		THD = 1% , f = 1 kHz R <sub>L</sub> =4Ω	-	700	-	
		THD = 10% , f = 1 kHz R <sub>L</sub> =8Ω	-	700	-	
		THD = 1% , f = 1 kHz R <sub>L</sub> =8Ω	-	550	-	
Total Harmonic Distortion+ Noise	THD+N	P <sub>o</sub> = 280 mW <sub>rms</sub> , f = 1kHz	-	0.11	-	%
Power Supply Rejection Ratio	PSRR	V <sub>ripple</sub> = 200mV sine p-p, Input with floating.	-	62 (f = 217Hz) 62 (f = 1kHz)	-	dB
Wake-up time	T <sub>WU</sub>		-	82		ms
Thermal Shutdown Temperature	T <sub>SD</sub>		150	170	190	°C

(\*1)Typical values are included for reference only and are not guaranteed or tested.

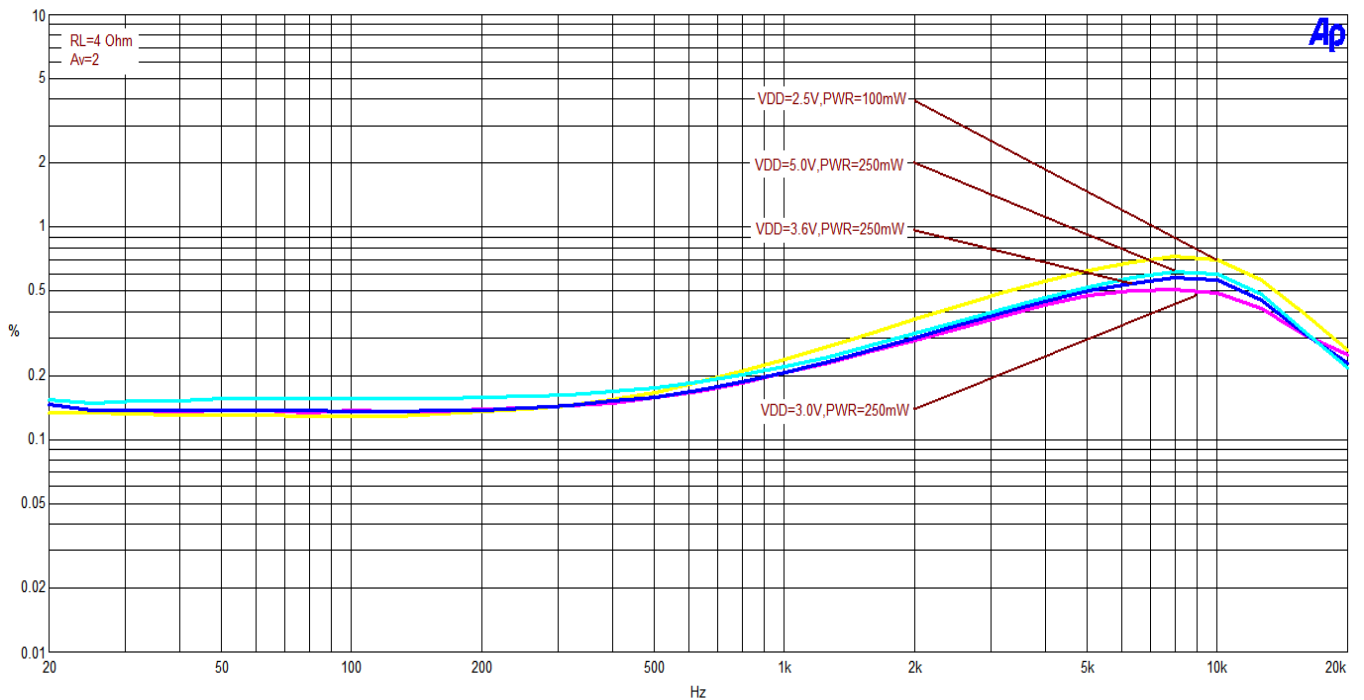
Typical values are measured at VCC = VCC(TYP.) and TA = 25°C

**TYPICAL PERFORMANCE CHARACTERISTICS**

**Figure 3**  
THD+N vs Frequency (at  $R_L=8\Omega$ ,  $A_V=2$ )

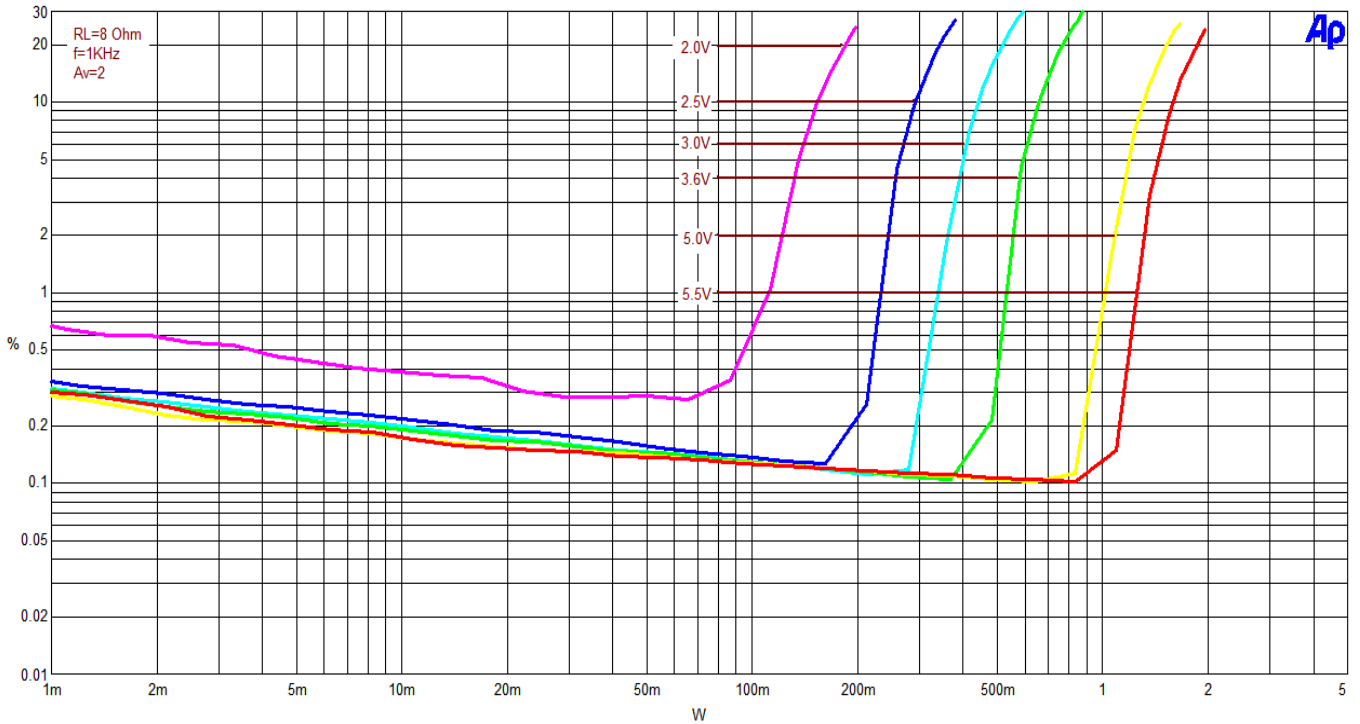


**Figure 4**  
THD+N vs Frequency (at  $R_L=4\Omega$ ,  $A_V=2$ )

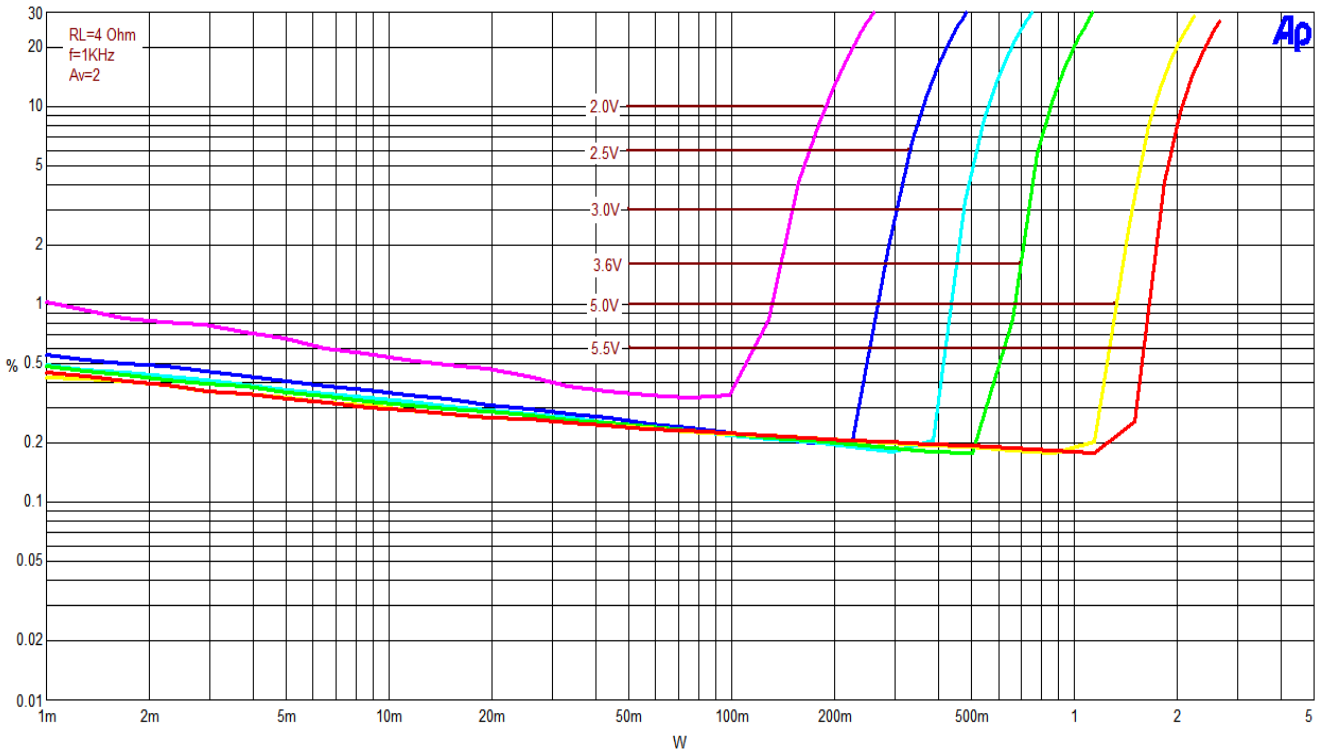




**Figure 5**  
THD+N vs Power Out (@  $RL=8\Omega$ ,  $f=1kHz$ ,  $Av=2$ )

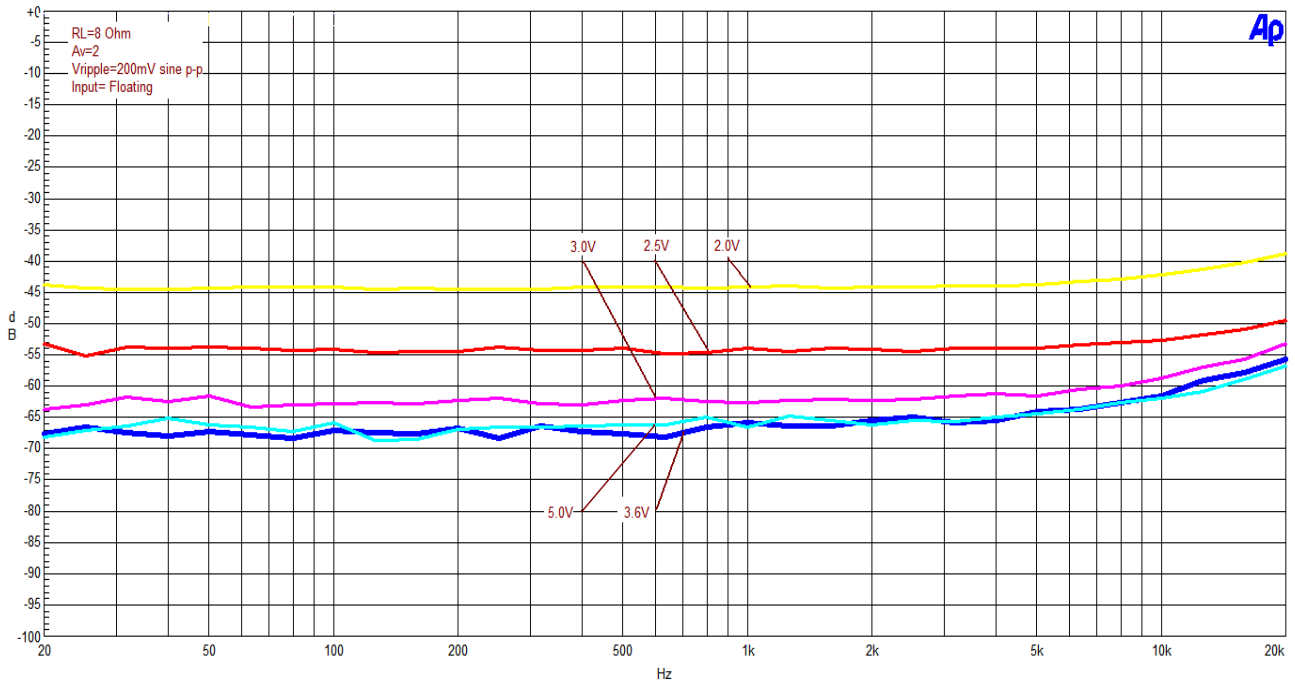


**Figure 6**  
THD+N vs Power Out (@  $RL=4\Omega$ ,  $f=1kHz$ ,  $Av=2$ )





**Figure 7**  
**Power Supply Rejection Ratio (PSRR)**  
**(@  $R_L=8\Omega$ ,  $A_v=2$ ,  $V_{ripple} = 200mV_{p-p}$ ,  $R_{IN} = Floating$ )**





## **APPLICATION INFORMATION**

### **BRIDGED CONFIGURATION EXPLANATION**

As shown in Figure 1, the LY8891 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of  $R_f$  to  $R_{IN}$  while the second amplifier's gain is fixed by the two internal 20k $\Omega$  resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$AVD = 2 \times (R_f / R_{IN}) \dots\dots\dots(1)$$

By driving the load differentially through outputs  $V_{o1}$  and  $V_{o2}$ , an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions.

This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

A bridge configuration, such as the one used in the LY8891, also creates a second advantage over single-ended amplifiers. Since the differential outputs,  $V_{o1}$  and  $V_{o2}$ , are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

### **INPUT CAPACITORS ( $C_i$ )**

The LY8891 input capacitors and input resistors form a high-pass filter with the corner frequency,  $f_c$ , determined in equation Equation 2.

$$f_c = \frac{1}{2\pi R_i C_i} \dots\dots\dots(2)$$

Equation 3 is reconfigured to solve for the input coupling capacitance.

$$C_i = \frac{1}{2\pi R_i f_c} \dots\dots\dots(3)$$

### **For example**

In the table 1 shows the external components.  $R_{in}$  in connect with  $C_{in}$  to create a high-pass filter.

**Table 1. Typical Component Values**

Reference	Description	Note
$R_i$	20K $\Omega$	1% tolerance resistors
$C_i$	0.39 $\mu$ F	80%/–20%

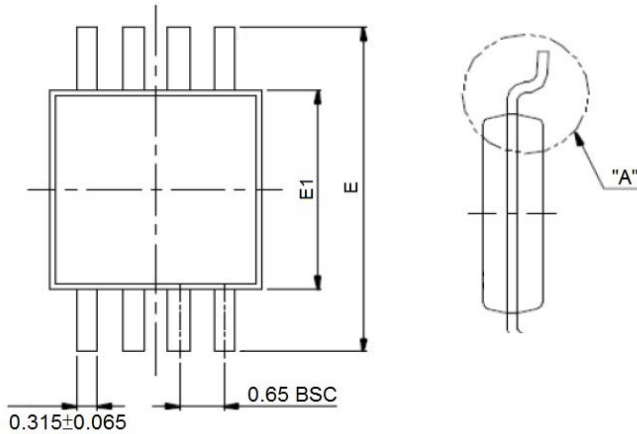


$$C_i = 1 / ( 2\pi R_i f_c )$$

$$C_i = 1 / ( 2\pi \times 20K\Omega \times 20Hz ) = 0.397\mu F \cdot \text{Use } 0.39\mu F$$

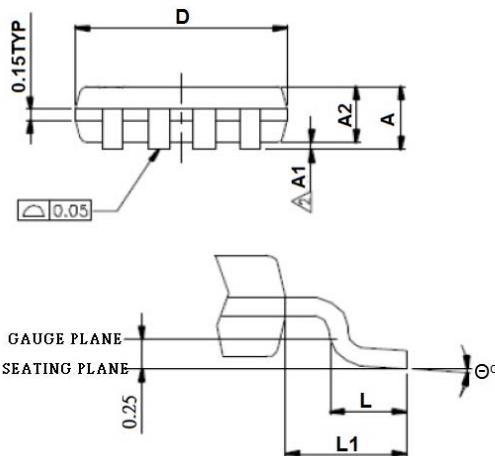
#### **POWER SUPPLY BYPASSING**

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible.

**PACKAGE OUTLINE DIMENSION**
**8 Pin MSOP Package Outline Dimension**


SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.10
A1	0.00	-	0.15
A2	0.75	0.85	0.95
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
θ°	0	-	8

UNIT : MM


**NOTES:**

1. JEDEC OUTLINE : MO-187 AA
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION '0.22' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE '0.22' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE  $\square$ .